SECOND ANNOUNCEMENT AND CALL FOR PAPERS

2025 SYMPOSIUM ON VLSI TECHNOLOGY AND CIRCUITS

~ Cultivating the VLSI Garden: From Seeds of Innovation to Thriving Growth ~

Rihga Royal Hotel Kyoto, Japan
Sunday–Thursday, June 8–12, 2025

June 8 Workshops
June 9 Short Courses
June 10–12 Technical Sessions

Paper Submission Deadline: 23:59 JST Monday, January 27, 2025
Details: www.vlsisymposium.org
New three-page Paper Format for Paper Submissions

Symposium Scope

The Symposium calls for papers in the following areas:

- **Advanced CMOS Platforms, Interconnect and Backside Power Delivery Network (BSPDN) Technologies**
- **Advanced packaging, Chiplet and Heterogeneous Integration Technologies Including 2.5D and 3D**
- **Analog and Mixed-Signal Circuits**
- **Beyond CMOS Devices That Utilize New Physics Including Spin, Optical and Quantum Computing**
- **Biomedical devices, circuits, and systems**
- **Data converters**
- **Device physics, Characterization, Modeling and Reliability**
- **Devices and Accelerators for ML/DL and New Compute**
- **Digital Circuits, Hardware Security, Signal Integrity, IOs**
- **DTCO and Design Enablement**
- **Frequency Generation and Clocking Circuits**
- **Memory Technologies, Devices, Circuits, and Architectures**
- **Power Management Devices and Circuits**
- **Processes and Materials for CMOS Scaling and New Devices**
- **Processors and SoCs**
- **Sensors, Imagers, IoT, MEMS, Display Circuits**
- **Wireless and RF Devices Circuits and Systems**
- **Wireline and Optical Transceivers, Optical Interconnects and Processors**

Paper Submission (New Format)

Prospective authors must submit paper abstracts with new Paper Format to the Symposium website www.vlsisymposium.org. Accepted papers will be published *as-submitted* with **no revisions permitted**. Authors must follow detailed instructions provided in the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. **Extended versions of outstanding papers will be invited for publication in the IEEE Transaction on Electron Devices, IEEE Journal of Solid-State Circuits, and IEEE Solid-State Circuits Letters.**

Highlights

The Symposium will be a fully in-person event with live sessions at the Rihga Royal hotel Kyoto to foster networking, with on-demand access to technical sessions available one week following the Symposium. The 5-day event will include : Plenary Sessions, Technical Sessions, Demo session for outstanding papers, Short Courses, Evening Panels and Workshop.

Short Courses

Symposium will offer Short Courses for Technology and Circuit.

1. Key VLSI Technologies in the AI era
2. Circuit and Systems for AI and Computing

Focus Sessions

In addition to the solicited topics, the Symposium will offer Focus Sessions on special areas of Technology and Circuits of joint interest, such as:

- **Advanced CMOS beyond 2nm** : CFET, 2D devices, BSPDN
- **Advanced Memory** : 3D DRAM, AI memory, embedded PCM
- **Circuit Design, DTCO, and Design Enablement**
- **3D Packaging and System Integration**
- **Design Automation** : AI for Automated Circuit Design
- **AI/ML Hardware** : Cloud Optics and AI

Call for Workshops

The Symposium provides valuable opportunities for volunteers to apply to organize and host short workshops at the Symposium. Call for Workshop | Symposium on VLSI Technology and Circuits

Best Student Paper Awards

Selection will be based on quality of the paper and presentation at the Symposium. The winning student will be presented with a certificate and monetary award at the 2026 VLSI Symposium opening session.

Demonstration Session

The popular in-person demonstration session will be part of Symposium program, providing participants an opportunity for in-depth interaction with authors of selected papers from both Tech and Circuit.

Contacts

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2025 VLSI SYMPOSIUM

Symposium Chairs:
Takaaki Tsunomura, Tokyo Electron Limited.
Mototsugu Hamada, The University of Tokyo

Symposium Co-Chairs:
Vijay Narayanan, IBM T.J. Watson Research Center
Ron Kapusta, Analog Devices

Program Chairs:
Kazuhiko Endo, Tohoku University
Sugako Otani, Renesas Electronics Corporation

Program Co-Chairs:
Benjamin Colombeau, Applied Materials
John Wuu, Advanced Micro Devices

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