Welcome to the 2020 Symposia on VLSI Technology and Circuits

The Next 40 Years of VLSI for Ubiquitous Intelligence

40th Anniversary

The 2020 Symposia on VLSI Technology & Circuits celebrates its 40th year with a virtual conference and the central theme of "The Next 40 Years of VLSI for Ubiquitous Intelligence". This week-long virtual conference features a fully overlapped program pushing the state-of-the-art in Technology and Circuits, packed with over 200 contributed technical presentations, technology and circuit demonstrations, 3 short courses, our “Friday” Forum and a “Luncheon Talk” that will be offered on-demand from the conference websites. These materials will be available for viewing at your convenience between June 14 to June 27 with the short courses and forum offering early access starting on June 8.

In addition to the on-demand sessions, the VLSI Symposia on Technology and Circuits will also feature an exciting program of live events. This includes 2 plenary sessions, 4 panel discussions, 3 workshops, and 25 Executive Sessions. The goal of Executive Sessions in the VLSI Symposia is to foster a discussion about the current state and future of the field. They will include 2-minute summaries of relevant papers that have been presented at VLSI Symposia 2020 on the topic, along with 35 minutes of discussion among the authors and session chairs on key challenges and opportunities. All conference participants are encouraged to join these meetings and contribute with insight and questions.

Thank you for your support of the Symposia, especially during this unprecedented pandemic time. We hope you enjoy the Symposia and wish you and your family continued good health.

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# VLSI Symposia in a Nutshell

## Live Streaming
*Watch at scheduled times*

- June 8 (Mon)
- June 9 (Tue)
- June 10 (Wed)
- June 11 (Thu)
- June 12 (Fri)
- June 13 (Sat)
- June 14 (Sun)

### June 15 (Mon)
- Plenary 1 Session
- Executive Sessions EA & EB

### June 16 (Tue)
- All Short Courses Summary & Q&A
- Executive Sessions EC & ED
- 3 Panels - Technology, Circuits, Diversity
- Workshop - Technology/Circuits for ML
- Workshop - Metrology

### June 17 (Wed)
- Plenary 2
- Forum Summary & Q&A
- Executive Sessions EE & EF
- Workshop - Quantum Computing

### June 18 (Thu)
- Executive Sessions EG & EH
- Young Professionals Mentoring

## On-Demand
*Watch pre-recorded videos at your convenience*

### Early Access for
- All 3 Short Courses
- Forum

### June 15 (Mon)
- All 3 Short Courses
- Forum
- Joint Focus Sessions
- Technology Sessions
- Circuits Sessions
- Joint Panel
- Demo Session
- Luncheon Talk
- All Workshops
- Full Recordings of All Live Events (available day after Live Event) except for Young Professionals Mentoring

## Papers & Slides Download
*See email sent to paid attendees*

- Papers & slides of Joint Focus, Technology & Circuits Session papers
- Slides of all 3 Short Courses
- Slides of Forum
- Slides of Workshops

Papers and slides also available in on-demand & executive sessions
On-Demand Technology, Circuits, and Joint Sessions are similar to typical paper sessions at previous Symposia on VLSI Technology and Circuits. The 2-page paper abstracts, presentation slides, and 20-minute video presentations are provided for your convenience “on-demand” anytime between June 14 (starting at 9:00am PDT) and June 27 (ending at 11:59pm PDT). Early on-demand access for short courses and the forum begins on June 8 at 9:00am PDT.

While viewing a recorded presentation, you can ask questions by typing your them in the "Q&A box", stating first the paper number and then your question. Your question will be directed to the session chairs and authors to respond.

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All live events (except Young Professionals event) will be available for on-demand access the day after event until June-27.

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**Live Streaming Content**

- **Traditional Sessions**
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**What is an Executive Session?**

**Live Content Page 6**
NEW!!! What is an Executive Session?

This year’s Virtual Symposia introduces new live Executive Sessions to foster live discussions and complement the On-Demand Sessions. The Executive Sessions feature 2-minute summaries of papers assigned to each executive session, along with 35 minutes of discussion among the authors and session chairs on key challenges and opportunities. All conference participants are encouraged to join these meetings and contribute with insights and questions.

There are a total of 25 live 50-minute executive sessions. Every On-Demand Technology, Circuits, and Joint Session paper as well as the Luncheon Talk is assigned to one Executive Session. Papers from each on-demand session may be mapped to several executive sessions.

Example mapping:
**PL1 - Plenary 1**

Session Chairs: Brian Ginsburg, Texas Instruments & Katsura Miyashita, Toshiba

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**PL1.1 Silicon is Greener: Why Innovation in Circuits is Needed for Sustainability**

Jennifer Lloyd, Analog Devices, USA

Sustainable development is one of the preeminent challenges facing humanity. The immediate and near-term identified challenge is carbon emissions, driven primarily from the energy sector. The integrated circuit industry has created an information and communications revolution which has transformed every sector of the economy from education to agriculture. Can the innovation and power of the industry transform sustainability? In this talk, we will show that by enabling electrification of the power sector (efficiency) and virtualization of physical processes (reducing energy demand), the integrated circuit industry will be a key enabler for solutions to sustainability issues.

Jennifer Lloyd received the S.B., S.M., and Ph.D. degrees in EECS from the Massachusetts Institute of Technology. She started her career as an analog designer at Analog Devices in the High-Speed Converter group, and has contributed to various ADC, DAC and SerDes products for which she holds 9 US patents and several papers and publications. She served on the technical program committee for both the IEEE Custom Integrated Circuits Conference and the IEEE Symposium on VLSI Circuits. Jen led ADI's core technology business in amplifiers and precision converters, along with the Instrumentation Market Group. For several years she was Vice President, Healthcare and Consumer Systems, where she led global engineering and business teams to build innovative solutions for those markets, which were discussed in a presentation at ISSCC in 2019. Dr. Lloyd is now Vice President for the Precision Technology and Platforms Group, in which she drives technology and market leadership across ADI’s precision franchises and related solutions in high-speed and precision amplifiers, precision converters, references, switches and

**PL1.2 5G Evolution and 6G**

Takehiro Nakamura, NTT Docomo, Japan

In this paper, 5G evolution, which is the enhancement of 5G, and the direction of the evolution of mobile communication technologies for 6G assuming the society and the worldview in the 2030s are examined, and requirements, use cases, and concepts pertaining to technical examination are described [1].

Takehiro Nakamura joined NTT Labs. in 1990. He is now SVP and General Manager of 5G Labs. in NTT DOCOMO, INC. Mr. Nakamura has been working for research and development of the W-CDMA, HSPA, LTE/LTE-Advanced, 5G and C-V2X/Connected Car technologies. He has been engaged in the standardization activities for W-CDMA, HSPA, LTE/LTE-Advanced and 5G at ARIB in Japan since 1997. He is currently the leader of 2020 and Beyond Ad Hoc (20B AH) in ARIB and Acting Chairman of the Strategy & Planning Committee in 5G Mobile Communication Promotion Forum (5GMPF) in Japan. He has been contributing to standardization activities in 3GPP since 1999. He contributed to 3GPP TSG-RAN as a vice chairman from March 2005 to March 2009 and as a chairman from April 2009 to March 2013. He is also very active in standardization of C-V2X/Connected Car in ARIB and ITS Info-communications Forum in Japan. He is now a leader of Cellular System Application Task Group of ITS Info-communications Forum.
PL2 - Plenary 2

Session Chairs: Tomas Palacios, MIT & Yusuke Oike, Sony Semiconductor Solutions

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PL2.1 The Future of Compute: How the Data Transformation is Reshaping VLSI
Michael Mayberry, Intel, USA

The digital transformation continues to gain momentum, as businesses offer consumers increasingly distributed services, and industry pursues improvements across the extent of the electronics ecosystem. This transformation is characterized by continued strong demand for compute at all points in the network – at the core, the edge, and at the endpoints. Data continues to grow at an exponential rate and not only drives the compute requirements, but also requires efficient solutions for movement and storage of data that is critical for overall performance. From device to cloud, new applications and use cases are continuously emerging. This transformation demands that we adapt our thinking and move from a hardware/program centric to a data/information centric approach, and to embrace new ways to compute. To keep pace in this dynamic environment, Moore’s Law and its impact have become more relevant than ever.

**Michael C. Mayberry** is the Chief Technology Officer at Intel Corporation. He is a Senior Vice-President, and General Manager of Technology Development where he is responsible for the research, development and deployment of next-generation silicon logic, packaging and test technologies that will produce future Intel products. Since joining Intel in 1984 as a process integration engineer, Mayberry has held a variety of positions. As part of the California Technology Development team, he developed EPROM, flash and logic wafer fabrication processes. In 1994, he moved to Sort Test Technology Development, responsible for road maps and development of test processes for Intel microprocessors. In 2005, he moved to Components Research and was responsible for research to enable future process options for Intel’s technology development organizations. In 2015, he moved to Intel Labs and became responsible for Intel’s product-driven research. In 2018, he moved to the Technology Development group at Intel. Dr. Mayberry received his bachelor’s degree in chemistry and mathematics from Midland College and his PhD in physical chemistry from the University of California, Berkeley.

PL2.2 Empowering Next-Generation Applications through FLASH Innovation
Shigeo (Jeff) Ohshima, Kioxia, Japan

The flash industry has continuously produced game-changing innovations in density, latency, and form factors resulting in large cost-performance benefits. To address the wide spectrum of storage demands coming from phone/IoT devices, mobile compute, up to data centers, new flash architectures are essential to handle these next generation applications. Future technology must include not only new architectures and more layers in flash chip designs, but also a roadmap for QLC flash and beyond, new memories, new classes of SSDs, and new software technologies. They must all come together to enable and accelerate the next wave of applications including the real-time analytics, AI (Artificial Intelligence)/ML (Machine Learning), high-performance computing, IoT, and virtual and augmented reality.

**Jeff Ohshima** is a member of the technology executive team at Kioxia, formerly Toshiba Memory Corporation, that started operation under its new corporate identity as of October 2019, where he currently focuses on SSD development and application engineering. He was previously VP Memory Technology Executive at Toshiba America Electronic Components, currently Kioxia America, Inc., focused on flash memory with an emphasis on SSDs. He was also Senior Manager R&D in the advanced NAND flash memory design department, responsible for 70 nm, 56 nm, 43 nm, and 32 nm design. He has been engaged with memory technology for over 30 years, including 20 years on DRAM where he acted as a design lead for application specific memories and did technical marketing. He has served as the keynote speaker for the Flash Memory Summit, held in every August in Santa Clara, CA for five consecutive years and has been back to back rated as the best keynote. Mr. Ohshima has served as a Visiting Research Scientist at Stanford University in 1992-93.
SC1 Technology Short Course - Future of Scaling for Logic and Memory

Session Chairs: Nirmal Ramaswamy (Micron), Vijay Narayanan (IBM), Kazuhiko Endo (AIST)

On-Demand Availability

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SC1.1 Nanosheet Transistor as a Replacement of FinFET for Future Nodes: Device Advantages & Specific Process Elements

Nicolas Loubet, IBM, USA

Horizontally stacked GAA Nanosheet structures can answer logic device needs for future technologies. They offer excellent electrostatics and short channel control, can be fabricated with minimal deviation from FinFET, with a significant reuse of legacy integration and manufacturing knowledge, and circumvent some of the patterning challenges associated with scaled technologies. Additionally, NS device architecture enable the best CMOS logic power and performance trade-off and provide additional area and gate length (Lg) scaling benefits at the 5nm node and beyond. The improved electrostatics of GAA devices and additional design flexiblity, which allow a continuous range of active widths (W_eff) in Nanosheet devices, open new opportunities in term of power/performance optimization. The benefits of using this technology for mobile and High Performance applications, including specific process and performance elements will be discussed. The challenges associated with the fabrication and the maturity of this technology for high volume manufacturing will be also discussed.

Nicolas Loubet received the B.S. and M.S. degrees in physics from Paul Sabatier University, Toulouse, France, in 2000 and 2001. In 2003, he received a high-level engineering degree in the field of physics and microelectronics from the National Institute of Applied Sciences in Toulouse, and the Ph.D. degree in 2006. From 2003 to 2008, he joined STMicroelectronics R&D group in front-end materials and epitaxy where he developed advanced epitaxy of Si and SiGe materials, and HCI vapor-phase etching of SiGe for the fabrication of silicon-on-nothing and dielectric isolation transistors. In 2008, he joined the Silicon Technology Research Alliance at IBM Research in Albany, NY and focused on junction and strain module engineering for the 20nm to 7nm CMOS device nodes using strained SOI and SGOI, SiGe relaxed buffer, and ultra-low resistivity SiGe:B and SiC:P for FDSOI and FinFET devices on bulk and SOI substrates. In 2015, he became a Senior Engineer and Technical Leader at IBM Research where his research focused on material, process, and device integration of Gate-All-Around devices for 5nm CMOS technology and beyond. He currently manages the Front-End Of Line (FEOL) Process Development team at IBM Research focusing on leading edge CMOS logic devices. He has published more than 100 papers and more than 250 patents.

SC1.2 On-Die Interconnect Challenges and Opportunities for Future Technology Nodes

Mauro Kobrinsky, Intel, USA

Interconnects advancements are critical to enabling Moore’s law. Each technology node demands: (1) pitch scaling at the lower metal layers to enable cell area reduction; (2) increasing number of interconnect layers; and (3) improvements in capacitance, line and via resistance on all layers (performance). In addition, 3D integration trends, including die and wafer stacking, create new challenges and open new opportunities. Future scaling research paths that include device stacking and novel power distribution schemes bring about need for additional interconnect advancements. In parallel, the impact of interconnects on overall part performance generates increased attention and visibility to interconnects. These ongoing trends have made Interconnect research one of the most dynamic and exciting areas in the Semiconductor Industry, abundant with exciting new ideas, challenges and opportunities. In this short course, we will first review the basic geometries, performance needs, and scaling trends of interconnects. We will also highlight a few of the most significant advances in the past 20 years. We will then discuss the most exciting leading options that Industry and Academia are exploring for future technology nodes. For scaling to 20 nm pitch and below, we will cover subtractive interconnects, new material options, and patterning challenges associated with scaled technologies. For mid-pitch intermediate layers, we will cover progress on three methods to improve performance: (i) barrier/liner thinning (standard and 2D options), (ii) graphene capping, and (iii) improvements on gap fill (e.g. Electroplating, Electroless plating, selective deposition) to enable higher aspect ratio interconnects. Finally, we will conclude by highlighting the opportunities and demands driven by novel 3D integration schemes, including die/wafer stacking mediated by Thru-Si Vias and Hybrid bonding, as well as monolithic device stacking.

Mauro J. Kobrinsky received his Ph.D. from the Massachusetts Institute of Technology in 2001. He has been with Intel's Components Research Division for 19 years; his current position is Director of Interconnects Structures and Architectures. He has contributed to all areas of interconnects research, including process integration, metallization, dielectrics, reliability, interconnects modelling, clock distribution, I/O, photonics, functional materials, 3D integration, and die-package interactions. He holds over 35 patents, and has more than 35 papers and conference presentations. Dr. Kobrinsky has served as a member of the Technical Advisory Board for the Interconnects and Packaging Science area of the Global Research Consortium (GRC), and as a member of the ITRS Interconnect roadmap section.
Modern IT technologies have been thriving owing to semiconductor technology progress following Moore’s Law which allows continuous improvements in key aspects of semiconductor chips such as power, performance, area, and cost. DRAM and Flash technologies have evolved successfully overcoming the apparently invincible technical barriers and been the key players in the semiconductor memory market. However, technical barriers are growing larger and larger and it is not easy to respond to all the requirements from various applications of IT era. There are growing concerns about whether such successful evolution will continue. On the other hand, there has been efforts to overcome the difficulties and limits of incumbent memories by developing new type of memories such as MRAM and PRAM. Such new type of memories have promising characteristics such as non-volatility, random access, high speed, and better endurance and attracted strong attention from early 2000s. Even though they have succeeded in starting mass production, they have been staying at niche market so far. In this presentation, challenges in technology scaling of memories such as DRAM, Flash, MRAM, and PRAM and approaches to overcome the technical barriers for future success.

Gwan-Hyeob Koh is currently a VP at Samsung Electronics and working on the development of STT-MRAM and PRAM. He joined Samsung Electronics in 1997 and was engaged in the development of 1Gb and 4Gb DRAM. Since 2002, he has been working on the development of next generation new memories including MRAM and PRAM. He was involved in the PRAM development from R&D to mass production stage, where his major work was related to process integration, memory device reliability, and yield enhancement. He has been working on the development of STT-MRAM since 2011. He received Ph.D. degree in physics from Seoul National University, Seoul, Korea in 1996. He authored or coauthored more than 60 papers in technical journals and international conferences. He has served as an editor of IEEE Transactions on Electron Devices’ (2013-2018), a subcommittee member of SSDM (2009-2015), IMW (2015-2019), and IEDM (2016-2017).

Lead-free HfO2 or ZrO2 based CMOS compatible ferroelectric layers even below 10 nm film thickness enable scalable devices like high aspect ratio ferroelectric capacitors (FeCap) and field-effect transistors (FeFET) in 2x nm technology nodes. This short course will cover these non-volatile memory array building blocks but also further applications like ferroelectric tunnel junctions, negative capacitance FETs (NC-FET), neuromorphic, piezo, and pyro electric devices are discussed. Ferroelectric properties are caused by a polar orthorhombic structure in polycrystalline films with a grain size of typically 20-30 nm. Transmission electron and piezo force microscopy studies are revealing single grain domain switching kinetics in the pristine case leading to larger (> 100 nm) domains after field cycling. By placing a doped HfO2 layer with a small number of grains within the gate-stack of a FeFET structure having a channel length of 30 nm, accumulative switching can be exploited to mimic the integrate-and-fire activity of biological neurons, which, together with FeFET-based synapses, might allow for building fundamental computing blocks of brain-inspired neural networks.

Anthony Yen is Vice President and Head of Technology Development Centers, ASML. He joined the company in 2017 with more than thirty years of experience in the field of nanolithography. Dr. Yen received his B.S.E.E degree from Purdue University and his S.M.E.E., Ph.D., and M.B.A. degrees from MIT. From 1991 to 1997, he was at Texas Instruments working on resolution enhancing techniques and an early investigator of optical proximity effects and their correction. From 1997 to 2003, he was with TSMC where he first led the development of its lithography processes, enabling TSMC to be the first company to adopt 193-nm lithography in the manufacturing of 0.13μm logic integrated circuits, and then co-led infrastructure development for next-generation-lithography technologies on assignment at SEMATECH. For three years at Cymer (now part of ASML) he was Senior Vice President responsible for marketing, he returned to TSMC in 2006. As head of Nanopatterning Technology Infrastructure Division, he led the development of EUV lithography, including its mask technology, for high-volume manufacturing which began at the 7 nm node in 2019. Dr. Yen has over 130 US patents and 100 publications. He is a Fellow of the IEEE and SPIE, and a recipient of the Outstanding ELECTRICAL AND COMPUTER ENGINEER AWARD from Purdue University.

Chang-Hong Shen is currently a VP at Samsung Electronics and working on the development of STT-MRAM and PRAM. He joined Samsung Electronics in 1997 and was engaged in the development of 1Gb and 4Gb DRAM. Since 2002, he has been working on the development of next generation new memories including MRAM and PRAM. He was involved in the PRAM development from R&D to mass production stage, where his major work was related to process integration, memory device reliability, and yield enhancement. He has been working on the development of STT-MRAM since 2011. He received Ph.D. degree in physics from Seoul National University, Seoul, Korea in 1996. He authored or coauthored more than 60 papers in technical journals and international conferences. He has served as an editor of IEEE Transactions on Electron Devices’ (2013-2018), a subcommittee member of SSDM (2009-2015), IMW (2015-2019), and IEDM (2016-2017).

Through-Silicon-Via (TSV) free monolithic three dimensional integrated circuits (3DIC) technologies have the advantages of (1) cost-effective manufacturing (2) compact chip small area, (3) low parasitic load for vertical signal transmissions, and (4) highly heterogeneous integration capability, including logic, memory, and sensors. The difficulties in fabricating TSV-free monolithic 3DIC involve the 3D hetero-integration process using stackable MOSFETS and memories based on low thermal-budget technology. In this short course, major TSV-free monolithic 3DIC technologies will be reviewed including 3D mono-Si/Ge MOSFETs and memories based on low thermal-budget technology. This short course presentation will cover the history of EUV lithography, basic imaging theory applied specifically to EUV lithography, the technology’s present status – its adoption in the production of 7- and 5-nm generations of logic integrated circuits; and how it can be extended to enable the manufacture of 3-nm logic node and beyond to future-generation DRAMs.

Anthony Yen is currently a VP at Samsung Electronics and working on the development of STT-MRAM and PRAM. He joined Samsung Electronics in 1997 and was engaged in the development of STT-MRAM and PRAM. He was involved in the PRAM development from R&D to mass production stage, where his major work was related to process integration, memory device reliability, and yield enhancement. He has been working on the development of STT-MRAM since 2011. He received Ph.D. degree in physics from Seoul National University, Seoul, Korea in 1996. He authored or coauthored more than 60 papers in technical journals and international conferences. He has served as an editor of IEEE Transactions on Electron Devices’ (2013-2018), a subcommittee member of SSDM (2009-2015), IMW (2015-2019), and IEDM (2016-2017).

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In situ BEOL Transistors and Oxide Electronics

Suman Datta, University of Notre Dame, USA

Amorphous oxide semiconductors have recently found commercial success in the form of thin film transistors for display applications. This short course will start with an overview of the fundamental advantage of amorphous oxide semiconductors as channel materials for low temperature processed transistors over their covalent semiconductor counterparts. We will identify the potential avenues for aggressive scaling of the oxide transistors and explore disruptive electronics, for example, three dimensional monolithic integrated circuits, enabled by oxide electronics embedded in the back-end-of-line (BEOL). We will evaluate the critical electrical characteristics, such as carrier transport, electrostatics, stability, endurance, extrinsic resistance associated with today's oxide semiconductor transistors fabricated at low temperatures, and their future improvement strategies. Finally, we will conclude with a benchmark study of the current and projected performance of oxide transistors with other semiconductor channel materials for BEOL transistor applications.

Suman Datta was with the Logic Technology Development group at Intel Corporation, Hillsboro, OR, USA, from 1999 to 2007, where he developed several generations of high-performance logic transistor technologies, including high-k/metal gate, tri-gate, and non-silicon channel CMOS transistors. He was a Professor of Electrical Engineering with Pennsylvania State University at University Park, University Park, PA, USA, from 2007 to 2011. He is currently the Stinson Chair Professor in Electrical Engineering with the University of Notre Dame, Notre Dame, IN, USA. He is the Director of a Multi-University Advanced Microelectronics Research Center, the ASCENT, funded by the Semiconductor Research Corporation and the Defense Advanced Research Projects Agency. He has published over 350 journals and refereed conference papers and holds 180 patents related to advanced semiconductors. He is a Fellow of the IEEE.

Layer Transfer Technology for Heterogeneous Material Integration

Tatsuro Maeda, National Institute of Advanced Industrial Science and Technology, Japan

The global semiconductor industry attempts to add values and extend functionalities within a single chip. Monolithic 3-D integration has emerged as a promising technological solution for high density, high performance, and multi-functional integrated circuits. Layer transfer technology of Ge and III-V semiconductors has attracted a lot of attention since these materials can be processed at low temperature and provide extended opportunity/functionality via heterogeneous material integration. Key challenges are how to manage material qualities of transferred layers, and how to fabricate high performance 3D devices under low-thermal budget process without performance degradation. In this talk, we discuss layer transfer technology for integrating Ge and III-V devices and its applicability to CMOS and photonics platforms for creating monolithic 3-D chip of the future.

Tatsuro Maeda is Research Manager in National Institute of Industrial Science and Technology (AIST), Ibaraki, Japan. His current research interests include heterogeneous integration of post-silicon devices such as SiGe, Ge, and III-V materials on Si platforms for future monolithic 3D application. He received the Ph.D. degree in material science from Tokyo Institute of Technology in Japan in 1996. In 1996, he joined the Electron Device Division, Electrotechnical Laboratory, Ibaraki, Japan where he has been engaged in the research on fabrication and characterization of ultra-small SOI-MOSFETs, nano-scaled Si-based devices, and single electron transistors for future CMOS components. In 2001, he joined AIST as a senior researcher. Now he belongs to Device Technology Research Institute in AIST. He has authored or co-authored over 100 publications and conference presentations related to nanoelectronics research.
SC2 Joint Short Course - Heterogeneous Integration - To Boldly Go Where No Moore Has Gone Before

Session Chairs: Alvin Loke (TSMC), Vijay Narayanan (IBM), Kazuhiro Endo (AIST), Makoto Nagata (Kobe University)

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SC2.1 Chiplet Meets the Real World: Benefits and Limits of Chiplet Designs
(SPC2)
Samuel Naffziger, AMD, USA

Chiplet architecture has been much discussed and debated, but today we are seeing real world architectural solutions based on chiplets in high volume production and mainstream markets. The benefits of these approaches in enabling lower costs from smaller die combined with modularity to scale performance and configuration will be covered, with examples taken from industry products. The costs of splitting and modularizing an SOC into chiplets will be discussed, which include the need to support high bandwidth and low latency communication between the die, overheads of testing and power managing what used to be individual SOC modules as standalone chips, and engineering the package substrate to provide routing and power delivery resources for the complex arrangement. Next will be an exploration of the fascinating optimization landscape these costs and benefits provide for finding the optimal application of chiplet architecture across product lines, both in the near term and looking into the next decade of innovation.

Samuel Naffziger is a Corporate Fellow at AMD responsible for technical strategy with a focus on power technology development. He has been the lead innovator behind many of AMD’s low power features and chiplet. He has over 30 years of industry experience with a background in microprocessors and circuit design, starting at Hewlett Packard, moving to Intel and then at AMD since 2006. He received the B.S.E.E. from the California Institute of Technology, Pasadena, CA, in 1988 and M.S.E.E. from Stanford University, Stanford, CA, in 1993 and holds over 130 US patents in the field. He has authored dozens of publications and presentations on processors, architecture and power management and is a Fellow of the IEEE.

SC2.2 Heterogeneous System Partitioning and the 3D Interconnect Technology Landscape
(SPC2)
Eric Beyne, imec, Belgium

High-density 2.5D and 3D integration technology will be used to realize “3D-SOC” heterogeneous systems to enable more complex, higher functionality, and higher performance systems than through traditional device scaling alone. This requires high bandwidth, low latency, and low energy chiplet-to-chiplet interconnect. With 3D integration being a very active field in the past decade, many technology directions have been proposed with a plethora of names and acronyms spawned to distinguish them apart. Unfortunately, this has created user confusion when comparing and selecting technologies for system applications. We propose a hierarchical view of the interconnect fabric, which we define as a 3D landscape, that extends from the die to the 3D interconnect level to span eight orders of magnitude in interconnect density. We will cover current technologies, as well as emerging ones in development, used to realize 2.5D systems, 3D stacked ICs, and 3D wafer-to-wafer stacking for 3D-SOCs. Technology elements such as Si interposers, through-silicon vias, solder microbumping, and hybrid wafer-to-wafer or die-to-wafer bonding will be discussed in detail.

Eric Beyne obtained a degree in electrical engineering in 1983 and the Ph.D. degree in applied sciences in 1990, both from the Katholieke Universiteit Leuven, Belgium. Since 1986, he has been with imec in Leuven, Belgium, where he has worked on advanced packaging and 3D interconnect technologies. Dr. Beyne is currently imec Fellow, VP R&D, and Program Director of imec’s 3D System Integration program.

SC2.3 Back-End Based Chiplet Integration Solutions & Roadmap
(SPC2)
Key Chung, SPIR R&D, Taiwan

With transistor scaling reaching both physical and economic barriers, transistor performance and cost have been increasingly lagging behind the historical Moore’s Law trajectory. However, demand for silicon remains incessant with the growth of internet traffic, artificial intelligence, autonomous driving, and big data. One solution to meet this demand is to integrate multiple dies into a package that is a so-called backend-based chiplet package. Chiplet packages are designed either heterogeneously or homogeneously with integrated devices. Over the years, electronic assembly houses have developed a plethora of chiplet technologies such as Flip Chip Multi Chip Module (FCMCM), 2.1D, 2.5D, 3D, Fan-Out MCM (FOMCM), and Fan-Out Embedded Bridge (FOEB). In this presentation, we review the advantages and disadvantages of chiplet-based designs, discuss their challenges and solutions, and offer chiplet trends.

C. Key Chung received his B.Sc. degree from Nanyang Technological University, Singapore, and Ph.D. degree from National Taiwan University, Taipei, both in materials science and engineering. He is currently the Senior Director of Advanced Package R&D at SPIR responsible for advanced chiplet packaging pathfinding, development, and initial ramp-ups across different business units. Dr. Chung and his team have successfully won several advanced packaging businesses in five years including ultra-thin FO-PoP, FOMCM, FOEB, 2.1D, 2.5D, and 3DIC packaging. He has been involved in electronic assembly for 26 years, focusing on packaging substrate and assembly material technology development, and having also worked at HP and Intel. He is a recognized expert in solder joint interconnection and a standing reviewer for the Journal of Alloys and Compounds from which he received the outstanding reviewer award. He has authored over 20 patents, over 30 journal and conference papers, and multiple invited talks at international conferences.
Heterogeneous Integration for AI Architectures
Arvind Kumar & Mukta Farooq, IBM Research, USA

The interest in AI has exploded over the past few years and the use of AI in applications is poised to increase dramatically for many years. However, AI already demands very large amounts of compute, memory, and bandwidth; to deliver these levels is becoming a pervasive challenge in computing system design. This explosive growth has provided a huge impetus to accelerate AI workloads by employing a mix of diverse components, including CPUs, GPUs, specialized accelerators, and memories. The requirement of high bandwidth interconnectivity between different components has been a major driver for heterogeneous integration. In addition, the diminishing node-to-node returns from scaling have propelled heterogeneous integration to the forefront of technology focus. This raises several questions. How does the current state-of-the-art in heterogeneous integration meet the ever-growing demands of AI? What novel integration schemes are needed to deliver continued gains in system performance? How can emerging memories and analog technologies, which show promise for accelerating AI workloads, be effectively integrated with conventional technologies? Finally, what is the path forward to deploy heterogeneous integration as a pervasive technology in this arena? We will examine both the architecture requirements for AI as well as the heterogeneous integration methods needed to enable an upward trajectory for system performance.

Arvind Kumar is a manager of AI Hardware Technologies at the IBM T.J. Watson Research Center. His research focuses on the requirements of AI systems and the heterogeneous integration innovations to accelerate them. He has presented a number of invited talks and been a panelist in this area. In addition, he has chaired and organized a number of future computing events, including the 2017 IEEE Rebooting Computing Conference. Prior to concentrating on AI, he worked extensively on device design, characterization, and simulation for several IBM SOI technologies. Dr. Kumar holds S.B., S.M., and Ph.D. degrees in electrical engineering and computer science, all from the Massachusetts Institute of Technology.

Mukta Ghate Farooq is a metallurgist and materials scientist with expertise in heterogeneous integration, CMOS BEOL, lead-free alloys, and chip-package interaction. She is currently the 3D Integration Leader for the Artificial Intelligence Center (AIC) at IBM Research. Mukta was the IBM technology leader who delivered the semiconductor industry’s first high-volume 3D logic wafer in 2013. Mukta is an IEEE Fellow, an IEEE EDS Distinguished Lecturer, and a Distinguished Alumna of IIT-Bombay. She has 216 granted US patents and is an IBM Lifetime Master Inventor and an IBM Academy of Technology member. She received her B.S. from the Indian Institute of Technology, Bombay, M.S. from Northwestern University, Evanston, IL, and Ph.D. from Rensselaer Polytechnic Institute, Troy, NY.

Heterogeneous Integration of Chiplets for Sensors
Marco Del Sarto, STMicroelectronics, Italy

System-in-Package (SiP), heterogeneous integration, and 3D interconnect are frequently coined as technologies that will disrupt Moore’s Law. Yet in the field of MEMS and sensors, these technologies have already been essential to successful product development for several years. Most MEMS sensors employ heterogeneous integration to co-package at least one die with dedicated micromachined technology and a standard IC that translates the electrical signals from the mechanical sensing element to a user-friendly signal. Here, 3D integration overcomes form factor challenges limited by conventional 2D interconnects. For example, caps or cans of various materials are used in environmental sensors for both protection and sensing ports while substrate passive components are commonly used in microphones. We will present state-of-the-art 3D integration techniques applied to MEMS and sensor packaging and offer an outlook on the convergence of the MEMS roadmap with advanced packaging solutions. We will cover the chiplet SiP approach for sensors; mechanical chiplets such as caps, cans, filters, and other mechanical parts that sense and transmit physical signals; novel usage of existing materials in a sensor assembly; and examples and future trends where sensors drive the package technology.

Marco Del Sarto received his M.D. in 2000 from the University of Pisa, Italy. His thesis work was on Lab-On-Chip developed at STMicroelectronics. He joined STMicroelectronics in 2001 as a MEMS designer in the area of testing, modeling, and simulation. From 2003 to 2006, he led the technical program management to industrialize the first MEMS accelerometers. From 2006 to 2016, he served a broad range of roles in the MEMS product quality department from customer quality assurance to department management. He concurrently managed the validation and characterization team working on MEMS sensors. Since 2016, he has been driving the package design R&D team for MEMS sensors.

Chiplet-to-Chiplet Communication Circuits for 2.5D/3D Integration Technologies
Kenny C. H. Hsieh, TSMC, Taiwan

More now than ever, conventional single-die package systems are facing both performance and cost challenges with continued CMOS scaling. As such, System-in-Package solutions, where multiple chiplets are integrated by various 2.5D/3D substrate technologies, have become lucrative alternatives. To be economically viable, they require carefully co-optimizing system design and package technology as well as the interconnects that enable communication between the chiplets. From a system perspective, the interface circuits need to be transparent to minimize power, area, and latency overhead. Here, we will briefly introduce prominent 2.5D/3D package technologies and outline opportunities and challenges presented by these technologies. We will explore circuit design and test considerations for these ultrashort-haul inter-chiplet links, covering topics such as clock schemes and synchronization, low-power design strategies, interconnect routing, and design for testability. We will also discuss recent design examples demonstrating high aggregate data bandwidth at high energy efficiency.

Kenny C. H. Hsieh received his B.S.E.E. degree from National Cheng Kung University, Tainan, Taiwan, and M.S.E.E. degree from National Chiao Tung University, Hsinchu, Taiwan, in 1985 and 1989 respectively. He designed SRAM and DRAM circuits at Winbond and Etron for 6 years prior to spending several years in PLL and Gm-C filter research at the University of California, Irvine. In 1997 to 2012, he designed high-speed SerDes at Ohm Technology, LSI/Avalog, and Xilinx in California. Mr. Hsieh joined TSMC in 2012 where he is currently a Deputy Director leading a mixed-signal design group. His current research interests include equalization theory for digital communication and design/technology co-optimization of advanced CMOS technologies.
SC2.7 Performance-Driven Design Methodology and Tools for 2.5D/3D Multi-Die Integration

Rajesh Gupta, Synopsys, USA

2.5D and 3D integrated circuits bring together complex logic and memory components, manufactured as multiple dies or chiplets, from the circuit board on to the same package. Modern 3DIC packaging technology is evolving rapidly and the 3DIC tools need to be versatile enough to handle a range of styles, across the space of 2.5D and 3D, including elements such as silicon interposers, silicon bridges, organic substrates, and their integrated combinations. The tools for design and verification of these chiplet/package combinations need to have high enough capacity to enable efficient co-optimization of the chiplets and the package. Design implementation tools need to enable the design of interconnect routes, microbumps on the chiplets, C4 bumps on the package, and through-silicon vias (TSVs) to be laid out with flexible layout styles to meet demanding electrical requirements including inductance effects. Signoff tools need to verify the power integrity, signal integrity and thermal integrity of the 3D system, with high enough accuracy to ensure the functioning and the performance, while enabling fast enough early feedback for optimization of the package design. DFT poses challenges because there is limited access to internal signals on the package and tools need to interoperate with new standards for addressing this. Special layout checks are needed to ensure proper connectivity of the chiplets via the package layout and to detect issues early. Above all, the 2.5D/3D IC tools should enable designers to explore the design space and efficiently converge on decisions to optimize the performance and power with minimal cost.

Rajesh Gupta is a Senior Director of Methodology at Synopsys, working on 3D IC tools and solutions. Previously, he worked at Samsung where he was responsible for CAD and design methodology for Samsung’s premium mobile processor designs. Before that he has held positions at Intel, on methodology development for the Atom processor designs, and at IBM, on EDA tool development for IBM’s very first Gigahertz Processor. Dr. Gupta has a B.Tech. from the Indian Institute of Technology, Madras and a Ph.D. from the University of Southern California, Los Angeles.

SC2.8 Generic Design Strategies and Considerations for 2.5D and 3D Stacked IC Designs

Ki Chul Chun, Samsung Electronics, Republic of Korea

2.5D/3D heterogeneous system integration is rapidly evolving to be the most promising solution to extend the celebrated historical Moore’s Law in the semiconductor industry. It has already been successfully deployed in various applications including high-performance computing, high-end graphics, and mobile computing. In this talk, we introduce state-of-the-art 2.5D/3D integration techniques such as chip partitioning, die-to-die interface, through-silicon-via (TSV) signaling, power delivery, and thermal considerations. Using 8-Hi/12-Hi 3D-stacked HBM2E as a practical example, we will present generic design strategies and considerations for 2.5D and 3D stacked IC ranging from power-efficient design techniques and performance optimization methods to stacked-die bit-cell reliability and design for testability.

Ki Chul Chun is a Principal Engineer and a Project Lead of HBM (High Bandwidth DRAM) chip design at Samsung Electronics. He received the B.S.E.E. degree from Yonsei University, Seoul, Korea, in 1998, the M.S.E.E. degree from KAIST, Daejeon, Korea, in 2000, and the Ph.D.E.E. degree from the University of Minnesota, Minneapolis in 2012. In 2000, he joined the Memory Division, Samsung Electronics, Hwasung, Korea, where he has been involved in low-power DRAM circuit design. After his Ph.D., he rejoined Samsung Electronics in 2012, where he has worked on low-power DRAM and HBM chip design. Dr. Chun received the ISLPED Low Power Design Contest Awards in 2009 with an embedded DRAM design and in 2012 with an embedded FLASH design. His research interests include 3D-DRAM circuit design and technology, low-power and high-speed DRAM design, and universal memory design such as STT-MRAM in scaled technologies.
### SC3.1 Topologies and Design Techniques of Switched-Capacitor Converters

**Wing-Hung Ki**, Hong Kong University of Science and Technology, Hong Kong

With the increasing demand of integrating voltage regulators completely on silicon, switched-capacitor (SC) converters that consist of only capacitors and switches are gaining popularity as substitutes or alternatives for inductor-based DC-DC converters. Step-up SC converters are also known as charge pumps, and handheld applications need mainly step-down charge pumps. This short course starts with charge balance law, followed by topological consideration, integrated circuit design technique and performance analysis. Step-up and step-down converters, 2-phase and multi-phase topologies and interleaving schemes for ripple reduction will be discussed.

Wing-Hung Ki received his B.Sc. degree (1984) from the University of California, San Diego, the M.Sc. degree (1985) from the California Institute of Technology, Pasadena, and the Ph.D. degree (1995) from the University of California, Los Angeles, all in electrical engineering. He first joined Micro Linear Corporation, San Jose, from 1992 to 1995, working on the design of power converter controllers. He then joined the Hong Kong University of Science and Technology in 1995. He is now a professor of the Department of Electronic and Computer Engineering. His research interests are integrated circuit techniques for power management circuits such as switched-inductor converters, switched-capacitor converters, low dropout regulators, wireless charging and implantable biomedical devices, and fundamental research in circuit analysis and design.

### SC3.2 The Noise-Shaping SAR ADC Technique: The Best of Both Worlds

**Michael Flynn**, University of Michigan, USA

The noise-shaping SAR technique, introduced in 2012, combines the efficiency of the SAR technique with noise-shaping. Noise-shaping extends the efficiency of SAR to higher resolution. Indeed, noise-shaping SAR ADCs have unrivaled energy and area efficiencies. Recently-published noise-shaping SAR ADCs demonstrate audio-level precision. This presentation explains the basics of noise-shaping SAR and discusses techniques to extend bandwidth and resolution.

Michael P. Flynn received the Ph.D. degree from Carnegie Mellon University in 1995. From 1995 to 1997, he was a Member of Technical Staff with Texas Instruments, Dallas, TX. During the four years from 1997 to 2001, he was with Parthus Technologies, Cork, Ireland. Since 2001, Dr. Flynn has been with the University of Michigan and is currently Professor. His technical interests are in RF circuits, data conversion, serial transceivers, and biomedical systems. He is a 2008 Guggenheim Fellow. He received the 2011 Education Excellence Award, 2010 College of Engineering Ted Kennedy Family Team Excellence Award, 2016 Faculty Achievement Award, and also the 2005-2006 Outstanding Achievement Award. He received the NSF Early Career Award in 2004. Dr. Flynn was Editor-in-Chief of the IEEE Journal of Solid-State Circuits from 2013 to 2016. He is a former Distinguished Lecturer of the IEEE Solid-State Circuits Society. He served as Associate Editor of the IEEE Journal of Solid-State Circuits (JSSC) and of the IEEE Transactions on Circuits and Systems. He is chair of the ISSCC Data Conversion Committee. He formerly served on the Technical Program Committees of ESSCIRC, A-SSCC, and the Symposium on VLSI Circuits.

### SC3.3 Next-Generation Readout of Resistor-Based Sensors

**Kofi Makinwa**, Delft University of Technology, Netherlands

This paper presents an overview of energy-efficient techniques intended for the readout of Wheatstone bridge sensors. Apart from energy-efficiency, such bridge-to-digital converters (BDCs) must achieve low input-referred offset, drift and noise; high gain accuracy, stability and linearity; as well as high immunity to power-supply and common-mode variations. Various BDC architectures will be discussed, beginning with classical ones in which an instrumentation amplifier is followed by an analog-to-digital converter (ADC), and moving on to more recent ones, which attempt to reduce complexity by eliminating the instrumentation amplifier and connecting an ADC directly to a bridge. The performance of these topologies, and in particular their energy-efficiency, will be compared and summarized.

Kofi Makinwa is a Professor at Delft University of Technology, Delft, The Netherlands. Before that he was a research scientist at Philips Research Laboratories in Eindhoven, The Netherlands (1989 to 1999). He holds B.Sc. and M.Sc. degrees (1985, 1988) from Obafemi Awolowo University, Ile, Nigeria, an M.E.E. degree (1989) from the Philips International Institute, Eindhoven, The Netherlands and a Ph.D. degree (2004) from Delft University of Technology, Delft, The Netherlands. His main research interests are the design of precision analog circuits and sensor interfaces. This has resulted in 16 books, over 250 technical papers and over 30 patents. He is the co-recipient of 16 best paper awards, from the JSSC, ISSCC, VLSI, ESSCIRC and Transducers, among others, and is an ISSCC top-10 contributor. Prof. Makinwa has been on the program committees of several IEEE conferences, and has served the Solid-State Circuits Society as a distinguished lecturer and as a member of the Adcom. He is currently the Analog Subcom chair of the ISSCC, a member of the editorial board of the Proceedings of the IEEE and a co-organizer of the Advances in Analog Circuit Design workshop and the Sensor Interfaces Meeting. He is an IEEE Fellow and a member of the Royal Netherlands Academy of Arts and Sciences.
**SC3.4  Time Reference and Frequency Generation**

Thomas Burd, IBM, USA

On-chip implementation of a timing reference has been gaining more attention as it offers great opportunities for miniaturized system and lower cost. Among various candidates for extracting controllable timing without bulky quartz-crystals, RC has been preferred over LC and ring-based ones in building integrated oscillators using CMOS technologies. However, challenges should still be taken in circuit design for widespread use of the RC oscillator as a wake-up timer in ultra-low-power sensor node or references for wireless and wired communications. Depending on application, power consumption, phase noise and jitter are specifically emphasized while commonly necessitating the long-term frequency stability. This talk reviews fundamentals of open-loop and closed-loop circuit implementations of the RC oscillator and performance-limiting trade-off factors. Recent trends of temperature compensation techniques will be also addressed with implementation examples.

Jae-Yoon Sim received the B.S., M.S., and Ph.D. degrees in electrical engineering from Pohang University of Science and Technology (POSTECH) in 1993, 1995, and 1999, respectively. From 1999 to 2005, he was a Senior Engineer with Samsung Electronics. In 2005, he joined POSTECH, where he is currently a Professor. From 2017 to 2019, he was the Director of the Joint Research Lab. nominated by the Korea Institute of Science and Technology. Since 2019, he has been the Director of the Scalable Quantum Computer Technology Center sponsored by the Ministry of Science and ICT of Korea. His research interests include frequency generation, sensor interface circuits, serial links, data converters and quantum computing. Dr. Sim was a co-recipient of the ISSCC Takuo Sugano Award in 2001. In 2020, he received the Science of the Month Award sponsored by Ministry of Science and ICT of Korea. He was an IEEE Distinguished Lecturer from 2018 to 2019. He served on the Technical Program Committees for the ISSCC, VLSI Symposium and A-SSCC.

**SC3.5  Low-Power and Digitally-Intensive RF Transceiver Design for IoT Applications**

Yao-Hong Liu, imec, Netherlands

This course will provide an in-depth discussion on the ultra-low power RF circuit transceiver and architecture design for Internet-of-Things (IoT) applications. By 2025, there will be up to 100 billion wireless sensor devices connected to IoT, and the cost of replacing or recharging the batteries will become one of the bottlenecks in the massive deployment of remote sensors. With such a strong demand on extending the battery lifetime of these IoT devices, ultra-low power RF transceivers are the key to achieving the final goal of autonomous operation for > 10 years. To address the challenges in IoT, the design requirements of one popular IoT protocol - Bluetooth Low Energy (BLE) - will be discussed. The design considerations and advancement of all-digital frequency synthesizers, one of the most critical building blocks in low-power RF transceivers, will also be addressed.

Yao-Hong Liu received his Ph.D. degree from National Taiwan University, Taiwan, in 2009. He was with Terax, Via Telecom (now Intel), and Mobile Devices, Taiwan, from 2002 to 2010, working on Bluetooth, WiFi and cellular wireless SoC products. Since 2010, he joined imec, the Netherlands. His current position is Principal Member of Technical Staff, and he is leading the development of the ultra-low power (ULP) RFIC design. His research focuses are energy-efficient wireless transceivers and radar for IoT and healthcare applications. He currently serves as a technical program committee of the IEEE ISSCC and RFC Symposium.

**SC3.6  Advances and Trends in High-Speed Serial Links for High-Density IO Applications**

Mounir Meghelli, IBM, USA

CMOS based high-speed serial electrical links continue to push the data rate forward with most recent realizations achieving over 100Gb/s at very good power efficiencies. Solutions for doubling the data rate of next generation serial links are however uncertain given the challenges of Moore’s Law and the fundamental Shannon capacity limit of the commonly used electrical channels. In this presentation, we will review the current state-of-the-art and discuss potential future options for high-density and low power wireline high-speed serial data communications, covering both electrical and optical links for server and networking applications.

Mounir Meghelli received the M.S. degree in electronics and automatics from the University of Paris Orsay in 1992 and the Engineering degree in telecommunication from the ENST-Paris, in 1994. He received his Ph.D. degree from the University of Paris VI after a 4 year research program with the CNET France Telecom Research Center, working on the design of high-speed ICs for optical communications in GaAs and InP HBT technologies. From 1998 to 2005, he joined the IBM T.J. Watson Research Center as a Research Staff Member working on the design of high frequency ICs in SiGe BiCMOS and CMOS technologies for wireline and wireless applications. From 2006 to 2011, he joined the IBM Server and Technology Group where he held a position of Senior Technical Staff Member position leading the design of advanced serial links for storage, networking and server applications. Since 2012, he has been managing the Mixed Signal Communication IC Design group at the IBM T.J. Watson Research Center.

**SC3.7  Adaptive Circuit & System Design Techniques**

Thomas Burd, AMD, USA

The last twenty years has seen an incredible explosion of adaptive circuit and system techniques, especially in the area of high-performance microprocessor design. While general purpose microprocessors continue to be essential components of any computing platform, their programmability and inherent flexibility cause them to have less performance, and less power efficiency, as compared to more structured designs such as GPUs, FPGAs, and ASICs. This deficiency has driven a significant amount of design effort to provide adaptive techniques in hardware to maximize the performance delivered, significantly improve power efficiency, and dramatically increase battery life. This talk will summarize the last twenty years of innovation, including topics such as voltage & frequency scaling, power gating, droop mitigation techniques, methods to mitigate process and environmental variation, as well as design and system-level mechanisms to enable reliability-aware performance optimizations. The talk will conclude by prognosticating what techniques we may see in future products.

Thomas Burd received the B.S, M.S, and Ph.D. degrees in electrical engineering and computer science from the University of California at Berkeley, in 1992, 1994, and 2001, respectively. He was a Consultant with multiple startups in Silicon Valley. In 2005, he joined Advanced Micro Devices, Santa Clara, CA, USA, where he has worked on multiple generations of high-performance x86 cores (including the Bulldozer and Zen families of cores) in physical design architecture, design for reliability, power delivery, and analysis methodology. He is currently a Senior Fellow Design Engineer and Physical Design Architect for the next-generation Zen core. He has authored over 25 conference and journal publications, in addition to the book Energy Efficient Microprocessor Design. He is an inventor of five U.S. patents. Dr. Burd has been serving on the ISSCC Technical Program Committee since 2017, where he is current the Digital Architectures and Systems Subcommittee Chair. He served on the Technical Program Committee for the Symposium on Very Large Scale Integration Circuits from 2012 to 2015, ICCAD from 2003 to 2005, and Hot Chips in 1996. He was a recipient of the 2001 ISSCC Lewis Winner Award for the Best Conference Paper and the 1998 Analog Devices Outstanding Student Award for recognition of excellence in IC design. He is a Senior Member of the IEEE.
Embedded memory continues to be the key defining component for modern SoC. As applications become more data centric, the performance of SoC for future abundant data computing is increasingly constrained by the bandwidth and energy of accessing data from memory. Alternative memory technologies and computing architectures are being actively explored to address these challenges, including the emerging memory technologies and in-memory computing. In this short course, the present status and key design considerations for various emerging memory technologies will be reviewed. The latest development and challenges for in-memory computing that exploit structural alignment of 2D SRAM or emerging memory arrays for energy-efficient matrix-vector multiplication will be discussed.

Yih Wang received his Ph.D. degree in electrical and computer engineering from University of Florida, Gainesville. He joined Intel’s logic technology development group in 2001 and was a Sr. Principal Engineer, leading the development of critical technologies for a variety of embedded memories, including embedded SRAM, DRAM, STT-MRAM and ReRAM. He received three Intel Achievement Awards for his contributions on development of embedded SRAM and DRAM technologies. He is currently a director in the design and technology platform group at TSMC. He has authored and co-authored more than 40 journal and conference publications and has more than 70 issued and pending U.S. patents.
**FF - "Friday" Forum - Technologies and Circuits for Edge Intelligence**

**Session Chairs:** Kamel Benaissa (Texas Instruments), Ron Kapusta (Analog Devices), Kazuyuki Tomida (Sony Semiconductor Solutions), Kouichi Kanda (Fujitsu Laboratories)

**On-Demand Availability**
June-08 09:00 PDT / June-08 18:00 CET / June-09 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

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**FF.1 Edge Intelligence – Technologies, Circuits, Architectures**

Ali Keshavarzi, Stanford University, USA

Edge Intelligence (EI) enables smart devices to sense, decide with, act on, and send information at the point of raw data collection rather than relying on the cloud. This archetype of Artificial Intelligence (AI) in small efficient systems is a key enabler for a wide range of applications, projected to reach a trillion Internet of Things (IoT) devices. Turning sensed data into actionable information locally allows for a careful balance of energy-efficient computing and communication demands, at the intersection of Moore’s Law and the Shannon-Hartley Theorem, resulting in minimized system energy consumption. Enabling devices to operate autonomously and sustainably in challenging and energy-constrained environments at a competitive SWaP-C metrics presents extraordinary technical challenges. Today, we will explore this interdisciplinary research field covering all scales - materials, devices, circuits, design, architectures, and implementations – to expand the vision of EI, defining the requirements of an engine for small-system AI and exploring the means to achieve them.

Ali Keshavarzi has been at the forefront of semiconductor technology innovation with a track record of successfully delivering critical technologies, devices, circuits, chips and modules for over 27 years. He has been at the leading edge of R&D in CMOS technology scaling, planar and FinFET devices, circuits and design for low-power, low-voltage electronics, and high-performance computing, low-power and programmable SoCs, wide I/O and high bandwidth memories, differentiated technology solutions by embedded non-volatile memory (eNVM), advanced multi-chip fan-out, Systems embedded in Package (SeP), and 2.5D packaging. Dr. Keshavarzi was the Vice President of R&D and a technical Fellow at Cypress Semiconductor. He has had various senior R&D roles at Intel, TSMC, and GlobalFoundries. Dr. Keshavarzi is the founder of Leading Edge Research (LER) company. Dr. Keshavarzi is an adjunct professor at Stanford University and was a visiting research scholar at UC Berkeley engaged in various research vectors in the field of low-power electronics and driving the vision of Edge Intelligence (EI) that enables smart devices to sense, decide with, act on, and send information at the point of raw data collection rather than relying on the cloud. He is also serving as an advisor to DARPA. Dr. Keshavarzi has over 65 granted patents and over 55 peer-reviewed papers.

**FF.2 Intelligent Edge – It’s Not Just Technology, it’s About Responsible Society**

Gowri Chindalare, NXP Semiconductors, USA

Global trend toward Edge Processing is not all about technology, not all about how many devices can we put on every person on the earth, and not at all about selling more technology. At the heart of this revolution is a paradigm shift that will propel us to build a responsible society that is more energy efficient, more productive, honoring individual safety and privacy. In this talk, we will discuss why it makes sense to embrace Edge Processing revolution, what technology companies like us are doing to drive its growth, challenges and opportunities ahead of all us.

Gowrishankar (Gowri) Chindalare is Head of Technology and Business Strategy for Industrial, IoT & Edge Processing with revenues of more than $1.5B at NXP Semiconductors, Inc. His team is responsible for studying global trends, identify growth opportunities, developing product strategy, competency gap assessments, and merger & acquisitions evaluations. Gowri has over 20 years of experience in the semiconductor field, spending his first fifteen years in R&D of innovative flash memory, radar and SoC technologies. He is the co-inventor of 75 issued patents and co-authored over 30 publications in the areas quantum mechanical effects, embedded flash memories, SoC integration and quality. Gowri obtained his Ph.D. in microelectronics from The University of Texas at Austin.

**FF.3 Heterogeneous Integration Technology Trends at the Edge**

Chih Hang Tung, TSMC, Taiwan

Edge computing and intelligence has gained momentum recently, made possible partially by novel in-package heterogeneous system integration. An overview on package-level heterogeneous integration platforms are discussed with focus on current products using state-of-the-art technologies. Close proximity at all levels, including chip-to-chip, and horizontal/vertical interconnection density is the underlying enabler for realizing edge device high performance computing using in-package multi-chip system integration technologies. Technology challenges and outlooks with future prospective are discussed as a summary.

Chih Hang Tung is Deputy Director of Exploratory 3D Program in TSMC R&D. He has worked in the Taiwan and Singapore semiconductor industry for over 30 years, covering areas including FEOL HKMG, silicid, to BEOL Cu low-k, and to far-back-end 3DIC and advanced packaging. Chih Hang has his M.S. degree from Illinois Institute of Technology (Chicago), has authored/co-authored for more than 250 peer reviewed papers, 30+ US patents, and a book “ULSI Semiconductor Technology Atlas” (Wiley 2003). He served as IEEE IFFA Chair in 2008, EDS Distinguished Lecturer (2007-2010), senior member since 2002, and received the IEEE EDS Paul Rappaport Award in 2008. He joined TSMC in 2008 and currently works in 3DIC and system integration.
Self Powered SOCs for the Intelligent Edge

Benton Calhoun, University of Virginia, USA

Self powered systems on chip harvest energy from their environment and remove the need for batteries, which is essential for allowing the Internet of Things to scale toward a trillion or more edge devices. This talk describes how self powered systems operate to meet application needs. Using an example industrial application, the application needs define requirements for the system on chip that support the harvesting context, the network needs, and computation at the edge. An example self powered system on chip shows how these capabilities are integrated into a device that intelligently operates without batteries.

Benton H. Calhoun received the M.S. degree and Ph.D. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, in 2002 and 2006, respectively. In 2006, he joined the faculty at the University of Virginia in the Electrical and Computer Engineering Department, where he is now a Professor. His research has emphasized energy efficient and sub-threshold integrated circuit design for self-powered, batteryless wireless sensing systems. Dr. Calhoun has over 200 peer reviewed publications and 22 issued US patents. He co-founded and is co-CTO at Everactive, Inc., which is selling self-powered, energy harvesting wireless sensing solutions in the industrial IoT market. He is a senior member of the IEEE.

CMOS and Beyond CMOS Technologies for Edge Intelligence

Myung Hee Na, imec, Belgium

The advent of modern smart phones transformed our lives and our daily routines profoundly. This has become even more evident during the current Covid-19 pandemic; it has been reported that the usage of edge devices has substantially increased. Mobile phones are no longer simple devices. They are nowadays vital to connect us to the outside world. CMOS technology has been crucial to advance the capabilities of these devices, and CMOS scaling has been essential to make these devices more affordable, faster, and more and more energy-efficient. Indeed, CMOS technology has been a remarkable success story of disruptive innovations spanning the fields of material sciences, device physics, and circuit design. During the last few years, the evolution from planar CMOS devices to FinFET has enabled a new era of scaled CMOS technologies. However, it cannot stop here. Disruptive innovations beyond these architectures are now required to maintain performance and power scaling for next-generation energy-efficient edge computing. In this talk, we would like to share our view of the evolving CMOS technology roadmap that needs to be followed to further advance the edge technology toward edge-computing.

Myung-Hee Na is a semiconductor technologist and currently work at imec as the Vice President of Technology Solutions and Enablement. She is currently responsible for CMOS and AI hardware technology research for new semiconductor era. Dr. Na received a Ph.D. in physics and started her career at IBM in 2001 where she held various technical, managerial and executive roles until early 2019. At IBM, she successfully led Research and Development for multiple generations of semiconductor technologies, including high-K metal gate, FinFET, and Nanosheet development. Moreover, she has co-authored numerous research papers and holds several U.S. and international patents.

Low Power Wireless Networking for the Edge

Thomas Watteyne, Analog Devices, USA

With standards such as 6TiSCH, IEEE802.15.4 TSCH and WirelessHART, the IoT has been going industrial for a number of years. Tens of thousands of such low-power wireless networks have been deployed in application domains as varied as Smart Factory, Smart Building, Smart Home and Environmental. Off-the-shelf products such as Analog Devices‘ SmartMesh IP offer >99.999% end-to-end reliability and over a decade of battery lifetime. Innovation in this domain also comes from vibrant open-source communities. We will first go through an overview of the key technology of the IIoT, and talk about what standards and products are available today. We will show numerous examples of where they are being used, all drawn from years of experience in real-world deployments. We will finish by discussing the research challenges ahead, both on dependable and technology-agile networking, and on crystal-free “Smart Dust” type architectures.

Thomas Watteyne is an insatiable enthusiast of low-power wireless mesh technologies. He is Senior Networking Design Engineer at Analog Devices, in the Dust Networks product group, the undisputed leader in supplying low power wireless mesh networks for demanding industrial process automation applications. He also holds a Research Director position at Inria in Paris, in the EVA research team, where he leads a team that designs, models and builds networking solutions based on a variety of Internet-of-Things (IoT) standards. Since 2013, he co-chairs the IETF 6TiSCH working group, which standardizes how to use IEEE802.15.4e TSCH in IPv6-enabled mesh networks. Prior to that, Thomas was a post-doctoral research lead in Prof. Kristofer Pister’s team at the University of California, Berkeley. He founded and co-leads Berkeley’s OpenWSN project, an open-source initiative to promote the use of fully standards-based protocol stacks for the IoT. Between 2005 and 2008, he was a research engineer at France Telecom, Orange Labs. He holds a Ph.D. in computer science (2008), an M.Sc. in Networking (2005) and an M.Eng. in telecommunications (2005) from INSA Lyon, France. He is an IEEE Senior Member.

Smart Vision Sensor

Hayato Wakabayashi, Sony Semiconductor Solutions, Japan

Today, the performance of image sensors exceeds the capabilities of the human eye and can provide more immersive experiences as a result. In addition, today’s image sensors can digitize various other kinds of information from typical 2 dimensional images where applications such as authentication, recognition, autonomous machine control, and wireless products further process this useful and efficient information. These latest sensors enhance the quality of services and the evolution of image sensing systems grow into a broader information conversion tool. In this talk, the requirements for smart vision sensors in high-speed and event-based processing systems for industrial automation and always-on sensing applications will be discussed. The performance requirements for these new application will be demonstrated. Finally, our vision of how the upcoming combination of Smart Vision Sensor and Artificial Intelligence technologies will profoundly influence our lifestyle, will be introduced.

Hayato Wakabayashi is a Deputy General Manager of the Research dVision at Sony Semiconductor Solutions Corporation. He received a B.S and M.S in engineering from Osaka University, Japan respectively and Ph. D. from Tohoku University, Japan. He served on the technical program committee of the Symposium on VLSI Circuits from 2014 to 2017 and has been engaged in a member of the technical program committee of International Solid-State Circuits Conference since 2017. He received the Walter Kosonocky Award for the paper on back-illuminated CMOS image sensor in 2011. He is currently working on the research and development of future imaging and sensing devices, circuits and systems.
As edge devices are becoming ubiquitous, it is increasingly important for them to be equipped with efficient hardware engines for intelligence. Such engines allow devices to respond to only meaningful events, thereby greatly reducing power consumption and data transfer. In addition, having inference engines on Edge devices allows for extracted features to be transferred to the cloud instead of raw data, providing a greater degree of security and privacy. In this presentation, we discuss possible approaches for making efficient neural engines for Edge devices. Since such inference engines are typically "always on", low power consumption is critical. We discuss possible on-chip memory hierarchies for making all-on-chip Wright storage more energy efficient as well as in-memory computation. We complete our presentation with a case study of a voice activity detection system which consumes < 200nW and measures less than 10 millimeters on a side.

David Blaauw received his B.S. in physics and computer science from Duke University in 1986 and his Ph.D. in computer science from the University of Illinois at Urbana-Champaign in 1991. Until August 2001, he worked for Motorola, Inc. in Austin, TX, where he was the manager of the High Performance Design Technology group and won the Motorola Innovation award. Since August 2001, he has been on the faculty of the University of Michigan, where he is the Kensall D. Wise Collegiate Professor of EECS. He has published over 600 papers, has received numerous best paper awards and holds 65 patents. He has performed extensive research in ultra-low-power computing using subthreshold operation and analog circuits for millimeter sensor systems, which was selected by the MIT Technology Review as one of the year's most significant innovations. For high-end servers, his research group introduced near-threshold computing, which has become common in semiconductor design. Most recently, he has pursued research in cognitive computing using analog, in-memory neural-networks for edge-devices and genomics acceleration for precision health. He was the ISLP general chair, the technical program chair for DAC, and serves on the ISSCC technical program committee. He is an IEEE Fellow and received the 2016 SIA-SRC faculty award for lifetime research contributions to the U.S. semiconductor industry.

Hannes Tschofenig is currently with Arm. Prior employers include the European Data Protection Supervisor, Nokia Networks, and Siemens. His work focused on developing global standards to make the Internet work better. He has been active in the Internet Engineering Task Force (IETF) for the past 18 years, contributing more than 80 RFCs on security, privacy, IoT, and emergency services. Hannes co-chaired various IETF groups, including the "Web Authorization Protocol" (OAAuth) working group and the "Authentication and Authorization for Constrained Environments (ace)" working group. From 2010 to 2014, Hannes was a member of the Internet Architecture Board (IAB), a committee of the IETF. He was also vice-chair of the FIDO Alliance Privacy and Public Policy Working Group. The FIDO (Fast IDentity Online) Alliance aims to change the nature of authentication on the Web by developing specifications that reduce the reliance on passwords. Recently, Hannes has been active in OMA SpecWorks, an organization working on the IoT device life-cycle management protocol LwM2M. Besides being a board member of OMA SpecWorks he also chairs the Device Management & Service Enablement working group.
JFS1 Joint Focus Session - Silicon Photonics

Session Chairs: Ted Letavic (GlobalFoundries), Bryan Casper (Intel), Mitsuro Takenaka (University of Tokyo), Hisakatsu Yamaguchi (Fujitsu Laboratories)

On-Demand Availability
June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Related Live Event(s)
Executive Sessions for Interactive Discussions, Paper Elevator-Pitch Summaries and Q&A
EG1 - Heterogeneous Integration (2) - June-18 08:00 PDT / June-18 17:00 CET / June-19 00:00 JST (1 hour)
EH6 - Si Photonics and DTCO - June-18 19:00 PDT / June-19 04:00 CET / June-19 11:00 JST (1 hour)

JFS1.1 TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s Optical I/O
Invited
Chen Sun, Ayar Labs, USA

We demonstrate an electro-optic platform enabling a direct optical I/O interface in an ASIC package. The 5.5x8.9mm² chiplet uses the Advanced Interface Bus (AIB), a parallel digital interface, to communicate to a host ASIC and integrates high-speed digital/analog circuits, optical modulators, photodetectors, and waveguides. Transmitters and receivers demonstrate data-rates up to 25Gbps at 4.9pJ/bit (Tx+Rx) and <10-12 BER error-free operation. We show a 32-channel, 512Gbps aggregate (across 4 Tx ports) wavelength-division multiplexed (WDM) transmit demonstration from a TeraPHY chiplet, running at 16Gbps per wavelength and 8 simultaneous wavelengths per port.

Chen Sun received a B.S. from UC Berkeley in 2009, and the S.M. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology in 2011 and 2015, respectively. Since 2015, he has been with Ayar Labs, Inc. where he is currently the Chief Scientist and VP of Silicon Engineering. His research interests include VLSI design and photonics I/O.

JFS1.2 High-Temperature Operation of Chip-Scale Silicon-Photonic Transceiver
Invited
Daisuke Okamoto, PETRA, Japan

A chip-scale optical transceiver was developed based on silicon photonics technology and optical/electrical assembly for 25-Gb/s × four-channel applications. Optical transmitters and receivers were integrated on a single silicon platform enabled by the hybrid integration of a quantum-dot laser diode, optical pins, and a 28-nm CMOS based electrical IC. Temperature compensation functions were implemented in a modulator driver and a transimpedance amplifier for high-temperature operations. The functions allowed us to successfully demonstrate error-free 25 Gb/s × four-channel data transmission at 85°C. The developed optical transceivers are suitable for embedded optical modules under high temperature environments for the realization of broadband interconnections between LSIs.

Daisuke Okamoto received the B.E. and M.E. degrees from Kyoto University, Japan, in 2003 and 2005, respectively, and a Ph.D. degree in engineering from Tohoku University, Japan, in 2019. He joined NEC Corporation in 2005, where he was involved in studies on plasmonics and silicon photonics. From 2008 to 2009, he was a Visiting Scholar at the Massachusetts Institute of Technology. He is currently a Senior Researcher for the Photonics and Electronics Technology Research Association, Tsukuba, Japan. His current research interests include silicon photonics and optical interconnects. He is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Japan Society of Applied Physics.

JFS1.3 A Monolithically Integrated Silicon Photonics 8×8 Switch in 90nm SOI CMOS
Invited
Jonathan Proesel, IBM T. J. Watson Research Center, USA

This work presents the first fully packaged silicon photonics 8×8 switch with monolithically integrated electrical control circuits in 90nm SOI CMOS. The switch is a strictly non-blocking network built from 2×2 and 2×2 Mach-Zehnder switches (MZSs). 180 DACs tune the MZSs and 112 ADCs measure optical power across the network for feedback control. Digital interfaces provide low-speed tuning/monitoring and high-speed switching controls. 5.6ns optical switching is achieved with thermooptically tuned crosstalk <−33.5dB.

Jonathan Proesel is a Research Staff Member at the IBM T.J. Watson Research Center, where he works on circuit design for high-speed optical and electrical communications. He received the Ph.D. degree in Electrical and Computer Engineering from Carnegie Mellon University in 2010. His research interests include high-speed wireline communications, silicon photonics, data converters, AI hardware, and design-technology co-optimization.

JFS1.4 III/V-on-Bulk-Si Technology for Commercially Viable Photonics-Integrated VLSI
Invited
Dongjae Shin, Samsung Advanced Institute of Technology, Republic of Korea

We have demonstrated a complete set of on-chip Si-photic components using our III/V-on-bulk-silicon (Si) technology. Our bulk-Si-based technology shows unrivaled CMOS compatibility and much improved thermal dissipation, leading to superior performance over the III/V-on-SOI technology at a fraction of cost. The components demonstrated on the bulk-Si platform include single & tunable wavelength laser diodes, semiconductor optical amplifiers, Ge & III/V photodiodes, modulators, waveguides, and couplers. Fabrication of Si-photonics components are all carried out on the same bulk wafers that will host CMOS ICs, and all the fabricated components show robust performance in experimental characterizations. Using these bulk-Si components, a solid-state beam scanner for the light detection and ranging (LiDAR) system is currently under development. The III/V-on-bulk-Si technology will open a new path for silicon photonics to share and enjoy the colossal infrastructure and remarkable commercial success of the CMOS technology in coming years.

Dongjae Shin is a principal researcher at Samsung Advanced Institute of Technology, and is currently working on silicon photonics to leverage the silicon infrastructure of Samsung for emerging applications. He has two decades of photonics research experiences with one book, 50+ papers, and 100+ patents on silicon photonics, WDM-PON, VLC, and near-field optics. Dr. Shin is an IEEE senior member.
O-Band GeSi Quantum-Confined Stark Effect Electro-Absorption Modulator Integrated in a 220nm Silicon Photonics Platform

Clement Porret, imec, Belgium

We report on a waveguide-coupled quantum-confined Stark effect (QCSE) electro-absorption modulator integrated in a 220nm Si photonics platform and operating in 1335-1365nm wavelength range. The device is based on a strain-balanced GeSi quantum well/barrier stack grown on an ultra-thin strain-relaxed buffer. The stack is only 450nm thick, facilitating optical coupling to sub-micron Si waveguides. An extinction ratio up to 8dB is achieved in a 40 µm long device for a 1Vpp drive voltage, demonstrating the potential of this modulator for low-power optical interconnect applications.

Clement Porret obtained his Ph.D. in materials science from the University of Grenoble in 2011 for his research on the growth of Mn-doped Ge nanostructures for spintronic applications. Between 2011 and 2015, he was an R&D and process engineer at Riber SA, where he worked on the engineering and passivation of III-V surfaces, using a SEMI-compatible 300 mm Molecular Beam Epitaxy system connected to a state-of-the-art III-V CMOS Metal Organic Vapor Phase Epitaxy production cluster. The project also included the deposition of high-K dielectric materials for future logic devices. In 2015, he joined imec as a SiGe epitaxy researcher, with the development of solutions for sub-14 nm technology nodes using Reduced-Pressure Chemical Vapor Deposition as a main task. Since then, Dr. Porret has been involved in various projects including, e.g., the formation of strained channels, the selective epitaxial growth of highly-doped source/drain materials for Si and Ge fin and gate-all-around field-effect transistors, the synthesis of graphene on Si compatible platforms and the fabrication of integrated electro-absorption modulators.
JFS2 Joint Focus Session - 5G/mm-Wave

Session Chairs: Kamel Benaissa (Texas Instruments), Amin Arbabian (Stanford University), Aaron Thean (National University of Singapore), Wei Deng (Tsinghua University)

On-Demand Availability: June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Related Live Event(s):
- EG5 - Devices and Circuits for Advanced Communications - June-18 10:00 PDT / June-18 19:00 CET / June-19 02:00 JST (1 hour)
- EH2 - High Speed Circuits, Systems, and Devices - June-18 17:00 PDT / June-19 02:00 CET / June-19 09:00 JST (1 hour)

JFS2.1 Hardware-Software Co-integration for Configurable 5G mmWave Systems
Invited
Alberto Valdes-Garcia, IBM, USA

Directional communication systems based on millimeter-wave phased arrays have reached a significant level of maturity and have entered the commercial space for 5G networks. In order to realize their full potential, Si-based phased arrays must be integrated efficiently at the system level with digital control electronics, firmware, and software. This paper describes key architecture approaches for such vertical integration from digital-RF co-integration in the IC to API definition in software. The important benefits of low-latency and versatile control of beamforming and radio functions from high-level APIs is illustrated with application examples at 28 GHz including directional channel sounding, spatio-temporal beamforming, and 3D imaging.

Demo
Alberto Valdes-Garcia is currently a Principal Research Staff Member and Manager of the RF Circuits and Systems Group at the IBM T. J. Watson Research Center. He received the Ph.D. degree in electrical engineering from Texas A&M University in 2006. From 2006 to 2009, Dr. Valdes-Garcia served in the IEEE 802.15.3c 60GHz standardization committee. From 2009-2012 he served as on the SRC Technical Advisory Board, where he was Chair of the Integrated Circuits and Systems Sciences Coordinating Committee in 2011 and 2012. In spring 2013, he was also an Adjunct Assistant Professor at Columbia University. He holds 65+ issued US patents, authored 100+ publications, and co-edited the book "60GHz Technology for Gbps WLAN and WPAN: From Theory to Practice". Dr. Valdes-Garcia is recipient of the 2005 Best Doctoral Thesis Award, the 2007 National Youth Award for Outstanding Academic Achievements in Mexico, the 2010 George Smith Award, and the 2017 ISSCC/JSSC Lewis Winner Award for Outstanding Paper. In 2013, he was selected twice by the National Academy of Engineering. Within IBM, he is a co-recipient of an IBM Corporate Outstanding Innovation Award and the Pat Goldberg Memorial Award. Dr. Valdes-Garcia is a Senior Member of IEEE, was inducted into the IBM Academy of Technology in 2015, and became an IBM Master Inventor in 2016.

JFS2.2 Beyond 5G & Technologies: A Cross-Domain Vision
Invited
Eric Mercier, Université Grenoble Alps, CEA-Leti, France

5G deployment is on-going and many challenges are arising. New Radio (NR) Frequency Range 2 (FR2) in the millimeter (mmW) frequency domain starts being considered. Wideband over extended spectrum is targeted, enlightening broadband capacity and even much higher throughput than current views. In addition, spatial coverage based on quite small short wave-length antenna-array beam-forming offers new use case scenarios. As a consequence, the induced bands to support are increasing as well as the complexity of Front-End Module (FEM). But for autonomy and economical attraction, massive deployment can only happen with energy efficiency improvement. This paper will propose optimization paths for mmW system architectures, and their actual implementation, PHY considerations, and associated technology advances, for an holistic approach of the entire communication chain, and will highlight some promising trends for the development of 5G and beyond transceivers.

Eric Mercier is with the CEA-Leti in Grenoble since 2006, now in charge of CEA-Leti's Connectivity Technology Line coordination, including 5G and IoT topics, and Deputy Head of the Wireless & Telecom Unit. He received his M.S.E.E. from ENSEEIH, Toulouse, France, in 1991. He had held positions with Schlumberger/Wavetek working on optical fiber link tests, as well as with STMicroelectronics and Atmel as an R&D Application & Characterization and Marketing engineer in the field of IoT RF. At CEA-Leti, he has led projects in the area of ULP RF, focusing on low-power RF transceiver design and embedded resources for low-power IoT solutions. Amongst these research contributions, the FOXY solution has been awarded "Électron D'Or – Golden Electron 2018" for "Connected Objects" in France. For 4 years, he was the Head Manager of the Laboratory for Architectures & Integrated RF design in the Architecture, IC Design and Embedded Software department that developed RF solutions for ULP, UWB, UNB, mmW, High-DATA Rate, RFID, PA & FEM systems, with a common target of addressing the lowest possible power consumption and using the most advanced CMOS technologies. He has co-authored some peer-reviewed conference papers and contributed to a book chapter on Wireless Sensor Network topic.

JFS2.3 A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring 7nm EUV Process Technology
Invited
Minjung Jin, Samsung Electronics, Republic of Korea

The product reliability of 7nm FinFET technology is demonstrated with 5G SoC platform, which support for both sub-6GHz and millimeter wave 5G networks. RO aging and other high-speed operating 5G IPs show an expected reliability model behavior, which has further improvement of frequency noise reduction through 3-plate MIIM integration and high thermal conductivity EMC featuring ultra-low alpha particle (<0.002cph/cm²) emitter for the encapsulation of 5G product. Radiation effects are extensively examined at both chip and transistor level, proving the excellent SER and SEL due to less charge collection in narrow fin and robust TID effect. Degradation of 6T SRAM cell stability and performance caused by BTI is comparable to previous 10nm technology. Product level reliability is further evaluated through 256Mb SRAM array and API/Modem for mmWave 5G connectivity. The current 7nm technology featuring EUV is being expanded to automotive, HPC and AI beyond high volume 5G system.

Minjung Jin received the B.S. in electrical engineering from the Pusan National University, South Korea, in 2006. Upon graduation, she joined Technology Quality & Reliability of Samsung Electronics, South Korea, where she was focused on device reliability ten of Samsung’s different technology generations. She worked at the IBM-led ISDA alliance for 20nm as a Samsung assignee (2011-2013). She earned her M.S. from Sungkyunkwan University in 2018 while working at Samsung Electronics and is currently focusing on studying process impact on device and circuit reliability in sub-7nm process technology.
Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture

Chen Sun, National University of Singapore, Singapore

For the first time, ion implant was used to partially relax the tensile strain by half in the fully-depleted (FD) strained SOI (SSOI) so that SiGe pFETs with a higher compressive strain can be realized at a fixed Ge composition. This enables the co-integration of highly tensile-strained Si nFETs and compressive-strained SiGe pFETs on the same substrate, achieving significant improvement in electrical performance over the unstrained counterpart verified by both experiment and simulation results. We also propose a Comb-like SSOI architecture to further boost RF performance, demonstrating peak $G_m$ improved by 47% over unstrained FinFET SSOI, as well as an improvement of 22% and 36% for $f_t$ and $f_{max}$, respectively, over n-type SSOI FinFETs.

Chen Sun graduated from University of Electronic Science and Technology of China in 2018 and is now a second-year Ph.D. student at the National University of Singapore.

FinFET with Contact Over Active-Gate for 5G Ultra-Wideband Applications

Ali Razavieh, GlobalFoundries, USA

FinFET with contact over active-gate (COAG) is implemented on 12nm node technology platform to optimize the Maximum Oscillation Frequency ($F_{MAX}$) and the Minimum Noise Figure (NF$_{MIN}$) for devices with large fin numbers. This study shows that proposed COAG design can reduce the gate resistance of the 40-fin device by ~10-fold, while improving the $F_{MAX}$ by ~180% with comparable reliability performance to traditional FinFETs. Excellent DC and RF performances with NF$_{MIN}$ of 0.6dB at 26GHz and 3dB improvement in NF with 50Ω source impedance (NF$_{50}$) over the 5-26GHz frequency range makes large fin number COAG FinFET an excellent candidate for variety of 5G sub-6GHz and mmWave applications in which high $F_{MAX}$ and low noise are critical.

Ali Razavieh is a senior member of IEEE who is interested in different transistor structures for advanced logic and analog/RF applications. Currently, he is a member of the RF development team at GlobalFoundries with the focus on development of RF transistors based on different technology platforms for 5G sub-6GHz and mmWave applications.

An RF Transceiver with Full Digital Interface Supporting 5G New Radio FR1 with 3.84Gbps DL/1.92Gbps UL and Dual-Band GNSS in 14nm FinFET CMOS

Sangwook Han, Samsung Electronics, Republic of Korea

This paper presents an RF CMOS transceiver supporting all cellular protocols such as 2G, 3G, 4G, and 5G Frequency Range (FR) 1 with eighteen receiver pipelines and two chains of transmitters. To support all combinations of cellular carrier aggregation (CA) and dual band quad-mode GNSS efficiently, a fully digital interface is implemented to transfer data between the RFIC and modem instead of conventional analog interface, resulting in enhanced routability and robustness. Digital intensive design in 14nm CMOS process allows digital-aided calibration in RF/analog circuits.

Sangwook Han received the B.S. degree in electrical engineering and computer science from Seoul National University in 2002, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 2008 and 2012 respectively. From 2002 to 2006, he worked with Macro Image Technology, Inc. and Samsung Electronics in Korea and developed digital circuits and image processing algorithm for flat panel display applications. Since 2012, he has been with Samsung Electronics, Hwasung in Korea, where he works on mixed-signal circuit design including ADPLL, polar modulation, and high-speed serial interface for RF integrated circuits and wireless communication.

A 1.96Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems

Chen-Chien Kao, National Taiwan University, Taiwan

This work presents a massive multi-user MIMO (MU-MIMO) detector for cellular systems that can support 256 base station (BS) antennas and 32 users with modulation of up to 256-QAM. The chip delivers a throughput of 1.96 Gb/s and dissipates 87 mW at 290 MHz. Compared to the state-of-the-art detectors, the chip achieves a 5.7 to 30.5x higher area efficiency with 9.2 to 31.2x lower normalized energy.

Chen-Chien Kao received his B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2019. He is working on his M.S. degree at the Graduate Institute of Electronics of National Taiwan University. His research topic is energy-efficient VLSI design for massive MIMO communication systems.
We explore six different PR (Power Rail) design options in the range of library cell heights from 100 nm to 130 nm for the 1nm design rules (i.e. CPP (Contacted Poly Soyoun Kim, Samsung Electronics, Republic of Korea)

Shairfe Salahuddin, imec, Belgium

The increased metal resistance degrades both the performance and write margin of SRAM circuits in sub-10nm nodes. This paper utilizes buried power distribution as SRAM performance and write ability booster in 3nm node. BPP-SRAM offers up to 34.5% read speed and 498.6mV write margin improvement over conventional SRAM. Gem5 simulator predicts up to 28.2% performance gain in server-processor having BPR-SRAM in L2 and L3 cache as compared to the baseline.

Shairfe Salahuddin is a senior R&D engineer at imec. His research interest includes embedded memory, 3D integration, design enablement in advanced technology nodes.

Soyoun Kim, Samsung Electronics, Republic of Korea

In this paper, key contributors to local variability of sub-7nm FinFET has been identified in various operating environments. Through a comprehensive analysis, different root-cause for high and low temperature region have been revealed and confirmed by advanced Si wafer for the first time. Moreover, a local variation-aware transistor was successfully demonstrated to reduce v/min distribution by 0.5x and 0.3x at cold temperature.

Soyoun Kim received a B.S. degree from Pukyung National University, Korea, and M.S. degree from Sungkyunkwan University, Korea, in 2009. Soyoun joined the Semiconductor Research Center of Samsung Electronics and is currently in the Foundry Business of Samsung Electronics. Since 2017, she has been pursuing her Ph.D. at Seoul National University, Korea.
JFS4 Joint Focus Session - Devices and Circuits for AI/ML

Session Chairs: Edith Beigne (Facebook), Vijay Narayanan (IBM), Nicky Lu (Etron Technology), Huaqiang Wu (Tsinghua University)

On-Demand Availability

June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Executive Sessions for Interactive Discussions, Paper Elevator-Pitch Summaries and Q&A

EG3 - AI/ML - June-18 09:00 PDT / June-18 18:00 CET / June-19 01:00 JST (1 hour)

EH1 - MRAM - June-18 17:00 PDT / June-19 02:00 CET / June-19 09:00 JST (1 hour)

JFS4.1 SOT-MRAM Based Analog in-Memory Computing for DNN Inference

Jonas Doevenspeck, imec, ESAT-Katholieke Universiteit Leuven, Belgium

Deep neural network (DNN) inference requires a massive amount of matrix-vector multiplications which can be computed efficiently in memory arrays in an analog fashion. This approach requires highly resistive (>MΩ) memory devices with low resistance variation to implement DNN weight memories. We propose an optimized Spin-Orbit Torque MRAM (SOT-MRAM) as weight memory in Analog in-Memory Computing (AIMC) systems for DNN inference. In SOT-MRAM the write and read path are decoupled. This allows changing the MTJ resistance to the high levels required for AIMC by tuning the tunnel barrier thickness without affecting writing. The target resistance level and variation are derived from an algorithm driven design-technology-co-optimization (DTCO) study. Resistance levels are obtained from IR-drop simulations of a convolutional neural network (CNN). Variation limits are obtained by testing two noise-resilient CNNs with conductance variation. Finally, it is experimentally demonstrated that the requirements for analog DNN inference are met by SOT-MRAM stack optimization.

Jonas Doevenspeck received a B.Sc in physics (2014) and M.Sc in nanotechnology & nanoscience (2016), both from KU Leuven. Currently, he is a Ph.D. researcher at KU Leuven and in the imec Machine Learning program. His Ph.D. research focuses on machine learning with emerging memories. In 2019, he was a visiting researcher at the IBM T.J. Watson Research Center in Yorktown Heights, NY, working on emerging memories for deep neural network training.

JFS4.2 Compact Probabilistic Poisson Neuron Based on Back-Hopping Oscillation in STT-MRAM for All-Spin Deep Spiking Neural Network

Ming-Hung Wu, National Chiao Tung University, Taiwan

A unique compact Poisson neuron that encodes information in the tunable duty cycle of probabilistic spike trains is presented as an enabling technology for cost-effective spiking neural network (SNN) hardware. The Poisson neuron exploits the back-hopping oscillation (BHO) in scalable spin-transfer torque (STT)-MRAM. The macrospin LLGS simulation confirms that the coupled local Joule heating and STT effects are responsible for the bias-dependent BHO. The complete neuron circuit design is at least 6x smaller than the state-of-the-art integrate-and-fire (IF) CMOS neuron. Hardware-friendly all-spin deep SNNs achieve equivalent accuracy to deep neural networks (DNN), 98.4% for MNIST, even when considering the probabilistic nature of neurons.

Ming-Hung Wu currently is a Ph.D. student in the Institute of Electronics at National Chiao Tung University, Taiwan. His research interests include novel magnetic memory and its applications to neuromorphic computing.

JFS4.3 An All-Weights-on-Chip DNN Accelerator in 22nm ULL Featuring 24×1 Mb eRRAM

Zhehong Wang, University of Michigan, USA

We present a DNN accelerator in 22nm ULL CMOS featuring 24×1 Mb embedded RRAM. The accelerator, composed of 4 PEs and 512 MACs, achieves 0.96 TOPS/W at 120 MHz with 0.8 V VDD. Each PE contains 6 RRAM macros, equipped with a dynamic clamping offset-canceling sense amplifier that offers sub-µA current input offset.

Zhehong Wang received his B.E. degree from Zhejiang University, Hangzhou, China, in 2016. He is currently pursuing the Ph.D. degree in electrical and computer engineering at the University of Michigan, Ann Arbor. His current research interests include application-oriented emerging memory and ASIC.

JFS4.4 PNPU: A 146.52TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping

Sangyeob Kim, Korea Advanced Institute of Science and Technology, Republic of Korea

An energy efficient Deep-Neural-Network (DNN) learning processor is proposed for on-chip learning and iterative weight pruning (WP). This work has three key features: 1) stochastic coarse-fine pruning reduced computation workload by 99.7% compared with previous WP algorithm while maintaining high weight sparsity, 2) adaptive input/output/weight skipping (AIOWS) achieved 30.1× higher throughput than previous DNN learning processor [1] for not only the inference but also learning, 3) weight memory shared pruning unit removed on-chip weight memory access for WP. As a result, this work shows 146.52 TOPS/W energy efficiency, which is 5.79× higher than the state-of-the-art [1].

Sangyeob Kim received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2018 and 2020, respectively, where he is currently pursuing the Ph.D. degree. His current research interests include energy-efficient system-on-chip design, especially focused on deep neural network accelerators and machine learning algorithms for deep learning. Sangyeob is a student member of the IEEE.
This work presents a low-cost mixed-signal time-domain accelerator for generative adversarial network (GAN). A significant reduction in hardware cost was achieved through delicate architecture optimization for 8-bit GAN training on edge devices. An area-efficient subthreshold time-domain multiplier was designed to eliminate excessive data conversion for mixed-signal computing enabling high throughput mixed-signal online training demonstrated in a 65nm CMOS test chip.

Zhengyu Chen received a B.S. degree from Southeast University, Nanjing, China in 2013 and an M.S. degree in computer engineering from Cornell University, Ithaca, in 2015. He is currently a Ph.D. candidate in computer engineering at Northwestern University, Chicago, IL. He is an aspiring engineer doing research in the area of ultra-low-power design/algorithm for VLSI and mixed-signal ICs and emerging devices. Now he is focusing on the low-power hardware/software codesign for machine learning related applications.
This paper presents a high-bandwidth capacitive accelerometer array that is fully integrated with reconfigurable readout circuits and on-chip distributed temperature converters, CMOS-MEMS sensors, and machine learning. He was a recipient of the Analog Device Outstanding Student Designer Award in 2018.

Daehoon Na
received his M.S. degree in microelectronics from Peking University, Beijing, China in 2015. He is currently pursuing the Ph.D. degree in electrical and computer engineering at Carnegie Mellon University, Pittsburgh, PA, USA. His current research interests include sensor interface circuits, mm-wave circuits, data converters, CMOS-MEMS sensors, and machine learning. He was a recipient of the Analog Device Outstanding Student Designer Award in 2018.
JFS5.4  A 3D-Stacked Cortex-M0 SoC with 20.3Gbps/mm² 7.1mW/mm² Simultaneous Wireless Inter-Tier Data and Power Transfer

Benjamin Fletcher, University of Southampton, United Kingdom

This paper presents a 2-tier 3D-stacked Cortex-M0 SoC, in 65nm CMOS technology, with wireless inter-tier power and data transfer through an inductively coupled bus. The proposed design is the first implementation of a wireless link as part of a standard SoC bus, and achieves 20.3Gbps/mm² data, and 7.1mW/mm² power transfer simultaneously through a 250µm channel. This also makes it the smallest ever reported inductive data and power link.

Benjamin J. Fletcher received the B.Eng. degree (honors) in electronic engineering from the University of Southampton, U.K., in 2016 where he is currently a Ph.D. candidate studying as part of the ARM-ECS research centre (a joint collaboration between the University of Southampton and Arm Ltd, based in Cambridge, UK). His research interests include analogue and mixed-signal circuit design, low-power VLSI and 3D integration. In 2018, he was the recipient of the Institute of Engineering Technology Postgraduate Prize for his research on low-cost 3D integration approaches, and in 2019 won the International Symposium on Low Power Electronic Design Best Paper award.

JFS5.5  Heterogeneous Power Delivery for 7nm High-Performance Chiplet-Based Processors Using Integrated Passive Device and In-Package Voltage Regulator

Alan Roth, TSMC, USA

We demonstrate two heterogeneous solutions to improve power delivery to High-Performance Computing (HPC) processors. The scalable HPC vehicle integrates two 7nm CMOS processor chiplets, each with four ARM® Cortex®-A72 cores, that are mounted on a Chip-on-Wafer-on-Substrate (CoWoS®) silicon interposer [1]. In the first solution, Integrated Passive Device (IPD) capacitors are placed directly beneath the interposer to provide more accessible and effective supply noise decoupling. The result is 3.9% higher maximum clock frequency at a core supply of 1.135V. In the second solution, the processor is powered by a laterally mounted in-Package Voltage Regulator (PVR) built in 28nm CMOS augmented with high-permeability on-die inductors. The processor performance provided by the buck converter-based PVR matches that by an off-package External Voltage Regulator (EVR). As processor power increases with higher core counts, PVRs with on-die inductors will be increasingly compelling for efficient system power delivery.

Alan Roth joined the Austin Design Center of Taiwan Semiconductor Manufacturing Company in 2007. He is currently a Senior Technical Manager managing a team that specializes in analog and mixed-signal CMOS designs, with emphasis on power management circuits. Mr. Roth earned his B.S.E.E. in 1989 from the University of Florida. Prior to joining TSMC, he has worked as an analog and digital design engineer for several start-up companies and started his career as a memory design engineer at Motorola.
The popular demonstration session will be an on-demand pre-recorded video session of a demo. All the accepted demonstration videos will be posted online in the DEMO session, and viewers can click through them, post comments and ask questions, thereby providing interaction between the authors and virtual attendees. Attendees will be able to vote for their favorite demos within the On-Demand session until Tuesday June-16 11:59 PM PST. A winner will be announced during the Join Plenary LIVE session on Wednesday, June 17.

VOTE FOR YOUR FAVORITE DEMO IN THE ON-DEMAND SESSION!!!

CB1.4 1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-Chip with Dynamic Incremental-SAR Acquisition
Jun Wang, University of California San Diego, USA

CB1.5 High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at 11.72μm Pitch for Neuronal Network Analysis
Invited Yun Kato, Sony Semiconductor Solutions, Japan

CB2.1 A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR
Invited Tuan Thanh Ta, Toshiba, Japan

CB3.4 A 0.72nW, 1Sample/s Fully Integrated pH Sensor with 65.8LSB/pH Sensitivity
Yihan Zhang, Columbia University, USA

CC2.3 Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting
Massimo Alioto, National University of Singapore, Singapore

CP3.6 A Domino Bootstrapping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 96% High Efficiency
Hsuan-Yu Chen, National Chiao Tung University, Taiwan

JFS1.4 III/V-on-Bulk-Si Technology for Commercially Viable Photonics-Integrated VLSI
Dongjae Shin, Samsung Advanced Institute of Technology, Republic of Korea

JFS2.1 Hardware-Software Co-integration for Configurable 5G mmWave Systems
Invited Alberto Valdes-Garcia, IBM, USA

JFS5.3 A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-g Measurement Capability and Low Bias Instability
Xiaoliang Li, Carnegie Mellon University, USA

TM2.2 A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing
Weier Wan, Stanford University, USA

TN1.3 Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFET for Advanced Hardware Security
Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China
THL.1 5G and AI Integrated High Performance Mobile SoC Process-Design Co-Development and Production with 7nm EUV FinFET Technology

Jie Deng, Qualcomm Technologies, USA

We report on Qualcomm® Snapdragon™ 765 mobile Platform and world’s first integrated 5G platform supporting both mmWave and sub-6 using industry-leading 7nm EUV FinFET technology. Snapdragon 765 unites 5G and AI to power select premium full-function experiences on a global scale. Snapdragon 765 exhibits 20% improvement in performance and 35% lower power consumption over its predecessor Snapdragon 730 (8nm FinFET) thanks to device performance boost with new technology integration feature (MBD), power/perf efficient design architecture enabled by dual poly pitch process, and low voltage logic/memory operation through process-design co-development. Further process-design co-optimization reduces CPU Vmin by 80mV, enabling premium-performance experience with integrated 5G and AI mobile SOC platform.

Jie Deng received his Ph.D from Stanford University, Electrical Engineering, in 2007. He has been working on leading-edge MOSFET process development, device characterization, and DTCO in the past >12 years. He has more than 30 peer-viewed publications. Dr. Deng is now a Principal Engineer in Qualcomm Technologies Inc.

THL.2 GaN and Si Transistors on 300mm Si(111) enabled by 3D Monolithic Heterogeneous Integration

Han Wui Then, Intel, USA

We expand on our work in [1] by demonstrating both Si P- and NMOS finfet transistors monolithically integrated with GaN transistors on 300mm Si(111) wafers using 3D integration. With the Si finfet architecture, we are able to take advantage of the fin orientations of the transferred Si(100) crystal to fabricate both high performance Si P- and NMOS transistors. Furthermore, we demonstrate a variety of GaN transistor innovations, including enhancement (e-mode) and depletion mode (d-mode) GaN MOS transistor with high I_D=1.8mA/µm; GaN Schottky gate transistor producing high saturated power of 20dBm with peak PAE=57% at 28GHz; high performing, low leakage cascode and multi-gate GaN transistors; and GaN Schottky diodes with ultra-low C_OFF for ESD protection, all integrated on 300mm Si(111) wafer.

Han Wui Then received his B.S. (1999) and Ph.D. (2009) degrees in electrical and computer engineering from the University of Illinois at Urbana-Champaign (UIUC). He held an M.S. degree (2000) in electrical engineering from California Institute of Technology, Pasadena, and MS (2006) in physics from the National University of Singapore. He is currently at Components Research, Technology Development Group of Intel Corporation, working on novel advanced transistor technologies for system-on-chip (SoC), RF, power electronics, and logic. He has published over 35 journal and conference papers, and holds over 80 U.S. patents.

THL.3 An Optically Sampled ADC in 3D Integrated Silicon-Photonics/65nm CMOS

Nandish Mehta, University of California, Berkeley, USA

The accuracy of conventional ADCs for high-frequency input signals is mainly limited by the sampling clock jitter. To address this issue, this paper demonstrates an ADC that uses low-jitter (<26 fs rms) optical pulses to sample the input signal. A prototype two-channel ADC is realized in a 3D integrated platform with 65 nm CMOS and silicon-photonics connected using high-density TOVs. With optical pulses spaced at 250 ps (4 GS/s effective sampling rate), the ADC achieves SNDR of 40 dB near DC and 37 dB at 45 GHz input.

Nandish Mehta received the M.Sc. degree in microelectronics from Delft University of Technology in 2013, and Ph.D. in electrical engineering from the University of California, Berkeley, in 2019. He is currently working with Nvidia Inc, Santa Clara. Prior to that, he worked with Apple Inc in Cupertino, Broadcom Ltd. in the Netherlands, and the Indian space organization in Bangalore, India. His research interests includes application of integrated silicon-photonics to enable optical I/Os and analog-to-digital converters. Nandish is a recipient of IEEE SSCS pre-doctoral achievement award in 2019, ADI outstanding designer award in 2018, NXP scholarship in 2013, and Intel scholarship in 2008.

THL.4 A Monolithic 3D Integration of RRAM Array with Oxide Semiconductor FET for In-Memory Computing in Quantized Neural Network AI Applications

Jixuan Wu, University of Tokyo, Japan

We have monolithically integrated RRAM array with oxide semiconductor channel access transistor in 3D stack, achieved uniform memory characteristics of 1T1R cells at each layer, and demonstrated basic functionality of XNOR operation in a memory computing for binary neural network AI applications, for the first time. The impact of RRAM bit error rate on neural network is also investigated. 3D neural network built by this architecture has high potential to enable area-efficient, low-power and low-latency computing.

Jixuan Wu graduated from Shandong University (China) with a Ph.D. degree in 2019. His main doctoral research was 3D NAND flash memory reliability, 2D materials, and TFET devices simulation based on first principle calculations. He has been a post-doctorate researcher at the University of Tokyo since September 2019. His main research now includes reliability of ferroelectric-HfO2 devices based on first-principle calculation, HfO2-based RRAM devices characteristic.
Improved Air Spacer Co-Integrated with Self-Aligned Contact (SAC) and Contact Over Active Gate (COAG) for Highly Scaled CMOS Technology

Kangguo Cheng, IBM, USA

We report an improved air spacer that is successfully co-integrated on FinFET transistors along with Self-Aligned Contacts (SAC) and Contacts Over Active Gate (COAG). The new integration scheme presented enables air spacer formation agnostic to the underlying transistor architecture, thus paving the way for its adoption in FinFET and Gate-All-Around (GAA) transistors. A reduction in effective capacitance ($C_{\text{eff}}$) by 15% is experimentally demonstrated. The power/performance benefits achieved by the new air spacer exceeds the benefits of scaling FinFET from 7nm node to 5nm node.

Kangguo Cheng is currently a Senior Technical Staff Member and Master Inventor of IBM. He has over 18 years hands-on experience in CMOS technology research and development, ranging from planar bulk, partially depleted SOI (PDSOI), fully depleted SOI (FDSOI), FinFET, to emerging 3D device architectures such as FinFET and Gate-All-Around (GAA) devices. He also contributed to early development of vertical transistor DRAM, embedded DRAM (eDRAM) technologies. His technical expertise lies in advanced semiconductor devices and process integration. He has presented multiple papers related to FDSOI and FinFET at prestigious conferences such as IEDM and VLSI Symposia. Several of those papers have been selected as highlighted papers by IEDM and VLSI Symposia committees. Dr. Cheng is one of the most prolific inventors in the world with near 2,000 issued US patents. Dr. Cheng is an IEEE Fellow and a Member of IBM Academy of Technology (AoT). He received a B.Eng. degree and a M.Eng. Degree from Tsinghua University, China, in 1995 and 1997 respectively, and a Ph.D. degree from University of Illinois at Urbana-Champaign in 2001.

Buried Power Rail Integration with Si FinFETs for CMOS Scaling Beyond the 5nm Node

Anshul Gupta, imec, Belgium

Buried power rail (BPR) is a key scaling booster for CMOS extension beyond the 5 nm node. This paper demonstrates, for the first time, the integration of tungsten (W) BPR lines with Si FinFETs. The characteristics of CMOS in close proximity to floating BPR are found to be similar to the characteristics of CMOS without BPR. Moreover, W-BPR interface with Ru via contact can withstand more than 320 h of electromigration (EM) stress at 4 MA/cm² and 330 °C, making Ru a candidate for via metallization to achieve low resistance contact strategy to BPR.

Anshul Gupta works in the BEOL Process Integration Group of imec's Logic Device Integration and Pathfinding department involved in research and development of CMOS technology scaling enablers like buried power rail, alternative metals, and low-k interconnect stacks.
**TC1 Technology Session - Advanced Si CMOS Devices**

**Session Chairs: Paul Grudowski (NXP Semiconductors), Yuri Masuoka (Samsung Electronics)**

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**TC1.1 Enabling Multiple-Vt Device Scaling for CMOS Technology Beyond 7nm Node**

**Vincent Chang**, TSMC, Taiwan

For the first time, multiple-$V_t$ (multi-$V_t$) device options with $V_t$ range $>250$ mV are achieved in standard cells at dimensions beyond 7nm technology node. To overcome the common scaling challenges of potential device options such as FinFET and gate all-around (GAA) nanosheet transistor – gate length and cell height scaling, key enablers are identified, including novel, thin, and conformal work function metal (WFM) with enhanced patterning efficiency, high-k (HK) engineering, and precise WFM patterning boundary control. This work enables design flexibility for advanced CMOS technology beyond 7nm node with critical differentiators.

Vincent S. Chang received the B.S. degree from National Taiwan University, Taipei, Taiwan in 1991 and Ph.D. degree from Texas A&M University, College Station, TX, USA in 1999, both in chemical engineering. He was with Applied Materials, Hsinchu, Taiwan from 2000 to 2002, and has been with TSMC, Hsinchu, Taiwan since 2002. He also worked at imec, Leuven, Belgium as a TSMC assignee from 2006 to 2007. He has been working on advanced technology development in TSMC.

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**TC1.2 7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing**

**Sylvain Barraud**, CEA-Leti-MINATEC, France

In this paper, we experimentally demonstrate, for the first time, gate-all-around (GAA) nanosheet transistors with a record number of stacked channels. Seven levels stacked nanosheet (NS) GAA transistors fabricated using a replacement metal gate process, inner spacer and self-aligned contacts show an excellent gate controllability with extremely high current drivability (3 mA/µm at $V_{DD}=1V$) and a 3× improvement in drain current over usual 2 levels stacked-NS GAA transistors.

Sylvain Barraud received the Ph.D. degree from the Paris-Sud University, Orsay, France, in 2001. From 1998 to 2001, he worked at Institut d’Electronique Fondamentale (IEF), Orsay, France, on modeling and simulation of electron transport in field-effect transistors using Monte-Carlo method. He joined the French Atomic Energy Commission Laboratory (CEA-LETI), Grenoble, as a research staff member in 2001. From 2001 to 2009, he was engaged in the physics and modeling of transport in advanced MOSFET devices. Since 2010, his research activity is focused on innovative device integration. He has been involved in several industrial, European and national projects. His current research interests include the device physics, fabrication, and characterization of nanowire-based devices including tri-gate, omega-gate, and stacked-gate-all-around nanowire MOSFETs. In 2014, he received the IEEE Electron Devices Society’s Paul Rappaport Award. He has authored or co-authored about 200 papers published in international journals and conferences.

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**TC1.3 Cold CMOS as a Power-Performance-Reliability Booster for Advanced FinFETs**

**H. L. Chiang**, TSMC, Taiwan

We present advanced FinFET characterization and circuit analysis at reduced temperatures down to 77 K. Steepened subthreshold slope enables threshold voltage ($V_{th}$) and supply voltage ($V_{DD}$) scaling for ~0.27x power reduction without sacrificing logic switching speed. With simultaneous $V_{th}$ scaling, SRAM can operate at the same low $V_{DD}=0.4V$. Improved gate dielectric reliability raises maximum $V_{DD}$ for >70% speed boost when single thread performance is needed. Taking advantage of lower Cu wire resistance at 77 K, the repeaters for global signal propagation can be redesigned for 80% energy reduction. Increased thermal conductivity of silicon at low temperature reduces self-heating and further improves power efficiency. When refrigeration power is included, net power reduction can be achieved when cooling efficiency exceeds ~50% of Carnot limit. We present effective $V_{th}$ reduction methods for both nFET and pFET, critical for attaining high performance for cold CMOS.

Hung-Li Chiang received the B.S. degree in electrical engineering and the M.S. degree from the Graduate Institute of Photonics and Optoelectronics of National Taiwan University in 2007 and 2009, respectively. Since 2010, he joined Corporate Research at TSMC, Hsinchu, Taiwan. He has been working on the research of advanced logic devices and memory devices for 10 years. He holds 28 US patents in these areas. As a working engineer, he is concurrently pursuing a Ph.D degree at National Chiao-Tung University.

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**TC1.4 All-Operation-Regime Characterization and Modeling of Drain Current Variability in Junctionless and Inversion-Mode FDSOI Transistors**

**Daphnée Bosch**, CEA-Leti-MINATEC, France

We evidence a unique feature of junctionless Fully-Depleted Silicon-On-Insulator (JL FDSOI) transistors: the presence of both bulk and accumulation conduction renders standard $V_{t}$-variability studies incomplete. For JL transistors, we rather propose an original analysis of the (local and global) variability in all-operation-regimes, from subthreshold to accumulation. We evidence that the current variability around $V_{t}$ is highly sensitive to back-bias $V_{B}$ and film thickness ($t_{si}$) uniformity. We demonstrate experimentally for the first time up to 70% lower drain current ($I_D$) range >250 mV(583,670),(759,705) are achieved in standard cells at dimensions beyond 7nm technology node. To overcome the common scaling challenges of potential device options such as FinFET and gate all-around (GAA) nanosheet transistor – gate length and cell height scaling, key enablers are identified, including novel, thin, and conformal work function metal (WFM) with enhanced patterning efficiency, high-k (HK) engineering, and precise WFM patterning boundary control. This work enables design flexibility for advanced CMOS technology beyond 7nm node with critical differentiators.

Daphnée Bosch received a master degree in nano and micro technologies from PHELMA Grenoble-Inp, Politecnico di Torino and Ecole Polytechnique Lausanne. Her fields of interest as a Ph.D. student are 3D monolithic, junctionless transistors, and in-memory computing.
Haiwen Xu, National University of Singapore, Singapore

For the first time, we have achieved contact resistivity ($\rho_c$) less than $10^{-9} \Omega\cdot cm^2$ for p-type metal/Si$_{0.5}$Ge$_{0.5}$ contacts with in-situ doping-only technique. This is enabled by an optimized surface Gallium (Ga)-boosted Boron (B)-doped Si$_{0.5}$Ge$_{0.5}$ having active doping concentration ($N_a$) of $1.1 \times 10^{21} \text{cm}^{-3}$ grown using reduced pressure chemical vapour deposition (RPCVD). Compared with B-only doped sample with $N_a$ of $9 \times 10^{20} \text{cm}^{-3}$, B and Ga co-doping enhances $N_a$ by $2 \times 10^{20} \text{cm}^{-3}$, reducing $\rho_c$ from $1.5 \times 10^{-8} \Omega\cdot cm^2$ to $5.7 \times 10^{-10} \Omega\cdot cm^2$. $\rho_c$ was extracted using advanced ladder transmission line model (LTLM) structures. It was also found that sub-$10^{-9} \Omega\cdot cm^2$ $\rho_c$ of our Ti/In$_{0.5}$Ge$_{0.5}$ contact can be maintained with thermal budget up to 450 °C.

Haiwen Xu earned a bachelor degree in Jilin University in 2018 and is now a second-year Ph.D. student at the National University of Singapore.

Yu-Shiang Huang, National Taiwan University, Taiwan

The undoped stacked GeSn channels without parasitic Ge channels are realized by a radical-based highly selective isotropic dry etching. Heavily doped Ge sacrificial layers can reduce S/D resistance and the undoped GeSn channels can increase the channel mobility. SS=89mV/dec and $I_{ON}=42\mu A$ per stack ($10.5\mu A$ per sheet) at $V_{DS}=V_{DS}=-0.5V$ are achieved for the undoped 4-stacked 12nm-thick nanosheets with 120nm gate length and the width larger than 50nm. The etching selectivity and the channel uniformity are highly improved by the dry etching as compared to H$_2$O$_2$ wet etching. Both dry etching and undoped channel are essential to obtain stacked wide nanosheets with high performance.

Yu-Shiang Huang received the B.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2014. He is currently pursuing the Ph.D. degree in the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan. His current research interests focus on process integration and electrical characterization of high performance GeSn/Ga planar MOSFETs and stacked channel gate-all-around transistors, including epi design, patterning, channel release, gate stack, S/D contact, strain response, temperature dependent measurement, and low frequency noise. He achieved the record high mobility of CVD-grown GeSn p-MOSFETs in 2016 IEDM and performed the first vertically stacked GeSn channel pGAAFETs on Si by GeSn/Ga CVD epitaxial growth and optimum selective etching in 2017 IEDM. In addition, he fabricated the first stacked-triangular GeSn pGAAFETs with [111] facets, small dangling bond density, and roughness by orientation dependent etching in 2019 VLSI. Recently, he demonstrated the first Stacked GeSn pGAAFETs with Cap and record high IQN and Gm among all GeSn 3D transistors in 2019 IEDM. He has first-authored two journal papers and seven conference papers, including three IEDM and one VLSI papers.
Vertical Heterojunction Ge$_{0.92}$Sn$_{0.08}$/Ge GAA Nanowire pMOSFETs: Low SS of 67 mV/dec, Small DIBL of 24 mV/V and Highest \( G_{m,ext} \) of 870 \( \mu \)S/\( \mu \)m

Mingshan Liu, Forschungszentrum Juelich, Germany

We demonstrate high performance vertical heterojunction Ge$_{0.92}$Sn$_{0.08}$/Ge gate-all-around (GAA) nanowire (NW) pMOSFETs enabled by a top-down approach, a self-limiting digital etching and NiGeSn metallization. Thanks to the GAA NW geometry and EOT scaling, low SS of 67 mV/dec, small DIBL of 24 mV/V, and a high \( I_{ON}/I_{OFF} \) ratio of \( \sim 10^6 \) are achieved in the smallest NW device with a diameter down to 25 nm. Furthermore, record high \( G_{m,ext} \) of \( \sim 870 \) \( \mu \)S/\( \mu \)m and the best quality factor \( Q = G_{m,ext}/SS_{sat} \) of 9.1 are obtained for all reported GeSn-based pFETs.

Mingshan Liu is currently a Ph.D. student in electrical engineering at RWTH Aachen University. He received the B.Sc. and M.Sc. degrees from Chongqing University in 2014 and 2016 respectively and spent first-year of his Ph.D. at the University of California at Los Angeles. He has published several patents and presented at the International Electron Device Meeting (IEDM), IEEE Symposium on Very Large Scale Integration (VLSI), VLSI-TSA, EMN Photovoltaics, and ICAMPE. He has published papers in the Journal of IEEE Transactions on Electronic Devices, IEEE Electronic Device Letter, Solid-State Electronics, Nano Electronics and Optoelectronics, and Semiconductor Science and Technology. His current research topics are device modeling, novel semiconductor devices design, fabrication, and characterization.

Structural and Electrical Demonstration of SiGe Cladded Channel for PMOS Stacked Nanosheet Gate-All-Around Devices

Shogo Mochizuki, IBM Research, USA

In this paper, horizontal gate-all-around (hGAA) devices with a SiGe cladded nanosheet (NS) channel have been explored for their potential benefits of Vt modulation and improved NBTI. The SiGe cladded NS channel was formed through trimming of the Si NS channel followed by selective SiGe epitaxial growth. Selective Si NS channel trimming of 1 – 2 nm per side with low roughness and conformal SiGe cladding epitaxial growth of 2 – 3 nm with good crystallinity were demonstrated. It is shown that a SiGe cladding NS channel provides a reduction of threshold voltage (Vt) and improved reliability. It is also shown that a conformal Si cap grown on the SiGe cladded NS channel suppresses the interface trap density (Dit).

Shogo Mochizuki received the B.S., and M.S. degrees in engineering from Nagoya University, Nagoya, Japan, in 2004, and 2006, respectively, and the Ph.D. degree in engineering from Osaka University, Osaka, Japan, in 2019. In 2006, he joined the Process Technology Division of NEC Electronics Corporation, Sagamihara, Japan. He joined IBM Research in 2013 and has been engaged in the research and development for front-end process technology of next generation logic CMOS devices, particularly the research of advanced epitaxial growth-related process and integration technologies, and local crystallinity characterization in advanced scaled CMOS devices.
Materials Technology Co-Optimization of Self-Aligned Gate Contact for Advanced CMOS Technology Nodes

Ashish Pal, Applied Materials, USA

Materials technology co-optimization (MTCO) modeling is used for the first time to simulate Performance-Power-Area (PPA) benefits of self-aligned gate contact (SAGC) technology. We also demonstrate a process flow to integrate novel CMOS compatible materials and processes to enable SAGC at the 3nm node and below.

Ashish Pal completed his doctorate degree in electrical engineering from Stanford University in 2015 and since then, he has been a part of different development and modeling teams in companies like Intermolecular and Applied Materials. Ashish has worked on advanced logic nodes for FinFET, Gate-All-Around, 3D-NAND, DRAM, ferroelectric, NCFET, ReRAM and different other technologies.

Selective Enablement of Dual Dipoles for Near Bandedge Multi-Vt Solution in High Performance FinFET and Nanosheet Technologies

Ruqiang Bao, IBM Research, USA

We report that n-dipole and p-dipole (dual dipoles) can be co-integrated to provide a more flexible volumeless multiple threshold voltage (multi-Vt) solution in FinFET and Nanosheet (NS) technologies. The p-dipole process for dual dipoles co-integration is identified. When the Vt shift is less than 100mV, the mobility is slightly degraded, but other properties are not clearly affected. The improved pFET performance is from the Vt reduction. The dual dipole co-integration also provides a novel method for Vt definition via dipole Vt compensation. Our selective dipole enablement approach can implement near bandedge (BE) multi-Vt for high performance application.

Ruqiang Bao received the B.S. and M.S. degrees in materials science and engineering from the University of Science and Technology Beijing, Beijing, China, in 2001 and 2004, respectively, and the Ph.D. degree in materials engineering from Rensselaer Polytechnic Institute, Troy, NY, in 2010. After joining IBM in 2011, he has worked on advanced interconnect for back-end-of-line technology strategy and worked on front-end-of-line, particularly high-k metal gate, for 22nm, 14nm, 10nm, 7nm and 5nm technology and beyond. Currently, he is an IBM senior engineer and working on the new device architecture definition.

Composite Interconnects for High-Performance Computing Beyond the 7nm Node

Suketu Parikh, Applied Materials, USA

We demonstrate a design-technology co-optimization (DTCO) solution for enabling novel composite interconnects in next-generation high-performance computing (HPC) applications. Minimum-pitch signal line optimization with aggressively shrunk feature size potentially requires a non-Cu conductor while relaxed-pitch signal and power line optimization require traditional Cu metallization, along with properly tuned power tap spacing, activity factor and standard cell size. We discuss significant process innovation required to co-optimize signal and power line resistances. Our composite metallization scheme also reduces via resistance by 50%, which results in a net performance uplift of between 2%-10% depending on via density and power requirements. We believe this is an optimal approach for HPC applications that have implemented alternate, higher-resistivity conductor metals at the 1x levels.

Suketu Parikh is currently a Senior Director at Applied Materials, working on developing interconnect solutions for sub-5nm nodes. He has 25 years of experience in the semiconductor industry, working on integrating Cu-low K solution, yield enhancement analytics, and new technology introduction at Applied Materials. Prior to this, he worked on scaling Flash memory at Spansion, and integration at Texas Instruments. Suketu holds a Ph.D. in materials science from Arizona State University and B.Tech from IIT Mumbai.

Record Low Contact Resistivity to Ge:B (8.1x10⁻¹⁰ Ω-cm²) and GeSn:B (4.1x10⁻¹⁰ Ω-cm²) with Optimized [B] and [Sn] by In-situ CVD Doping

Fang-Liang Lu, National Taiwan University, Taiwan

The record low contact resistivity (ρc) of Ti contact to Ge:B (8.1x10⁻¹⁰ Ω-cm²) is achieved by in-situ doped CVD using the high-order Ge precursor (Ge₂H₆). The best achievable [B] for 7.1x10²⁰cm⁻³ and extended epitaxial process window are obtained using Ge₂H₆. By optimizing the [B] and [Sn], 2% Sn addition into Ge epitaxy reaches the lowest ρc of 4.1x10⁻¹⁰Ω-cm². Further Sn addition (4.7% and 13.2%) increases ρc due to reduced [B], and degrades the thermal stability. The record low resistivity (2x10⁻¹⁰Ω-cm) among epitaxial p-type Ge and GeSn is also demonstrated. Optimized metal etching processes (Cl₂+BCl₃ for metal on GeSn:B, while Cl₂ for metal on Ge:B) are necessary to minimize etching of GeSn:B and Ge:B, and to fabricate the test structure. A two-sheet-resistance model is used to correctly extract the ρc. B segregation (>1x10²⁷cm⁻³) at the metal/semiconductor interface enables the record low ρc.

Fang-Liang Lu received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2014. He is currently pursuing the Ph.D. degree at the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan. His current research interests include chemical vapor deposition, heavily doped epitaxy (Si/SiGe/Ge/GeSn) on Si with low metal/semiconductor contact resistivity, channel layer epitaxy for stacked nanosheet device applications.
TC3.5 High Quality N+/P Junction of Ge Substrate Prepared by Initiated CVD Doping Process
Jaehwan Kim, Korea Advanced Institute of Science and Technology, Republic of Korea
For the first time, a novel co-doping scheme of P and Sn into Ge substrate using an initiated CVD (iCVD) dopant-containing polymer film is successfully developed. This optimized doping process provides high carrier concentration n-type doping of 3 x 10^{20} cm^{-3} with a shallow junction depth of 50 nm. The enhancement of the P carrier concentration is attributed to less point defect generation during dopant injection and the strain relief effect induced by Sn co-doping with P into the Ge substrate. The Ge nMOSFETs with co-iCVD doping at the source/drain regions show lower off-state leakage current, higher on-current values, and lower contact resistivity compared to the Ge nMOSFETs with conventional ion implantation.

Jae Hwan Kim received the B.S. and M.S. degrees in electronic engineering from KwangWoon University and KAIST, in 2015 and 2017, respectively. He is currently pursuing the Ph.D degree in electronic engineering at KAIST, Daejeon, Republic of Korea. His current research interests are nanoelectronic devices, materials, and process developments for advanced CMOS device applications.

TC3.6 Ultra-low $\rho_c$ Extraction for Recessed and Non-Recessed Contacts: Generalized Transmission Line Model
Jishen Zhang, National University of Singapore, Singapore
A universal transmission line model (TLM) is developed to provide an accurate extraction of specific contact resistivity $\rho_c$ for both recessed and non-recessed contacts. This new model eliminates the need for the assumption that semiconductor sheet resistance under the contact $R_{shc}$ is equal to that in the contact gap region $R_{sh}$ which has been used for decades and expands the application of TLM-based methods for alloyed contacts for the first time. The model was verified experimentally by applying it to directly extract $\rho_c$, $R_{shc}$, and metal sheet resistance $R_m$ of alloyed p⁺-GeSn contact. The change of $R_{shc}$ due to alloying or recess-etching is well captured and ultra-low $\rho_c$ values of $1.0 \times 10^{-9}$ Ω-cm² are extracted. In contrast, conventional TLM-based methods lead to a large variation in $\rho_c$ extraction and miscalculate $\rho_c$ by neglecting the deviation of $R_{shc}$ from $R_{sh}$.

Jishen Zhang graduated from University of Electronic Science and Technology of China in 2018 and now is a second-year Ph.D. student at the National University of Singapore.
### TF1 Technology Session - FeFETs

**Session Chairs:** Suman Datta (University of Notre Dame), Byoung-Hun Lee (Gwangju Institute of Science and Technology)

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#### TF1.1 FeFET Memory Featuring Large Memory Window and Robust Endurance of Long-Pulse Cycling by Interface Engineering Using High-k AlION

**Chi-Yu Chan,** National Tsing Hua University, Taiwan

Without destabilizing the ferroelectric (FE) phase, high-k AlION with ~13% [N] was proposed as the interfacial layer (IL) between FE HfZrO$_x$ (HZO) and Si substrate for FeFET memory to enhance the memory window (MW) while improving reliability compared to SiO$_2$ IL. The AlION-based memory shows promising performance in terms of a large MW of 3.1 V by ±4 V operation, long retention up to 10 years, and robust endurance up to $10^5$ cycles with a long pulse width ($10^4$ s), outstanding other FeFET memory. It is ascribed to the high k-value and larger $\Delta E_v$ that respectively allow a lower voltage drop across the IL and suppress hole trapping. [N] in the IL also enhances the thermal stability that inhibits sub-IL formation by restraining the reaction of residual OH groups with Si substrate. Besides, the AlION and FE-HZO can be integrated in a single ALD step to simplify the process.

**Chi-Yu Chan** received his B.S. degree from the Department of Electrical Engineering, National University of Tainan, Taiwan, in 2018. Currently, he is pursuing his master's degree with a thesis focusing on the development of high-performance memory based on VLSI-compatible ferroelectric material.

#### TF1.2 Re-Examination of $V_{th}$ Window and Reliability in HfO$_2$ FeFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation

**Reika Ichihara,** Kioxia, Japan

We re-examine the dominant factors of the memory window (MW) and reliability of HfO$_2$ FeFET using a new technique to extract both spontaneous polarization ($P_s$) and interface trap charges ($Q_t$) by one-time current measurement of an FeFET during the memory operation. FeFET characteristics are strongly affected by unstable $Q_t$ (unrelated to ferroelectric) which causes $V_{th}$ instability just after programming, and stable $Q_s$ which compensates most of electric (E)-field generated by $P_s$. Stable $Q_s$ is coupled to $P_s$ with constant ratio (~90%), and reduce MW to the value much lower than the coercive voltage ($V_c$) limitation. Unlike the conventional model, $P_s$ increase and stabilization are still effective to improve MW and retention, respectively. During cycling, MW is degraded by $\Delta P_s$ reduction as well as the increase of the compensation ratio ($\Delta Q_t/\Delta P_s$) which can be mitigated by suppressing charge injection/ejection via interfacial SiO$_2$.

**Reika Ichihara** received the B.E. (2002) in applied chemistry and M.S. (2004) in advanced materials from University of Tokyo, Tokyo, Japan. In 2004, she joined the Advanced LSI Technology Laboratory, the Research and Development Center, Toshiba Corporation, Japan. In 2018, she joined Future Memory Development Dept., Device Technology Research & Development Center, Kioxia Corporation, Japan. She has been engaged in the research on the non-volatile memory devices.

#### TF1.3 Hot Electrons as the Dominant Source of Degradation for Sub-5nm HZO FeFETs

**Ava Tan,** University of California, Berkeley, USA

In this work, we demonstrate FDSOI ferroelectric FETs (FeFETs) incorporating 4.5 nm hafnium zirconium oxide, which show a ~0.5V memory window at ±3.3V and a program/erase speed of 1 µs. In typical FeFETs where ≥ 9 nm thick ferroelectric (FE) gate oxides have been used, bulk charge trapping has been identified as the main mechanism for endurance degradation and shrinkage of the memory window (MW). By contrast, we find that the role of bulk trapping in our devices with a much thinner FE layer is minimal. Through a combination of cryogenic temperature-dependent electrical measurements and simulations using the Ginestra™ modeling platform, we identify and prove that hot electron-induced hole damage during the application of negative gate biases is the primary source of endurance degradation and MW closure in FeFETs with scaled oxide layers.

**Ava J. Tan** is a Ph.D. student in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley, advised by Professor Sayeef Salahuddin. She received her B.S. in electrical and computer engineering from Cornell University in 2016. Her current research focuses on the realization of ferroelectric hafnium oxide-based nonvolatile memories for novel computing schemes, which encompasses materials development/optimization, device processing, and electrical characterization.
In this work, we developed a comprehensive model for ferroelectric FET (FeFET), which can capture all the essential ferroelectric behaviors. Unlike previous models, which can describe only a subset but not all the reported ferroelectric behaviors, the proposed model can: i) predict device performance with geometry scaling; ii) quantify the device-to-device variation with device scaling; iii) exhibit stochasticity during a single domain switching; and iv) capture the accumulation of domain switching probability with applied pulse trains. This comprehensive model would enable researchers to explore a wide range of FeFET applications and guide device development, optimization and benchmarking.

Kai Ni received the B.S. degree in electrical engineering from University of Science and Technology of China, Hefei, China in 2011, and Ph.D. degree of electrical engineering from Vanderbilt University, Nashville, TN, USA in 2016, working on characterization, modeling, and reliability of III-V MOSFETs. Since then, he became a post-doctoral associate at University of Notre Dame, working on ferroelectric devices for nonvolatile memory and novel computing paradigms. He is now an assistant professor in Microsystems Engineering at Rochester Institute of Technology. He has around 60 publications in top journals and conference proceedings, including Nature Electronics, IEDM, VLSI Symposium, IRPS, and EDL. His current interests lie in nanoelectronic devices empowering unconventional computing, AI accelerator, security and 3D memory technology.

Kasidit Toprasertpong received the B.E., M.E. and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 2013, 2015, and 2018, respectively. During 2015–2018, he was a Research Fellow of the Japan Society for the Promotion of Science. He is currently an Assistant Professor with the Department of Electrical Engineering and Information Systems, Graduate School of Engineering, the University of Tokyo.
### TF2.1 SoC Compatible 1T1C FeRAM Memory Array Based on Ferroelectric Hf$_{0.5}$Zr$_{0.5}$O$_2$

**Jun Okuno**, Sony Semiconductor Solutions, Japan

This paper experimentally demonstrates fundamental memory array operation of a ferroelectric HfO$_2$-based 1T1C FeRAM. Metal/ferroelectric/metal (MFM) capacitors consisting of a TiN/Hf$_{0.5}$Zr$_{0.5}$O$_2$(HZO)/TiN stack were optimized for a sub 500 °C process. Structures revealed excellent performance such as remanant polarization $2P_r>40$ μC/cm$^2$, endurance $>10^{11}$ cycles, and 10 years data retention at 85 °C. Furthermore, the MFM capacitors were successfully integrated into a 64 kbit 1T1C FeRAM array including our dedicated circuit for array operation. Back-end-of-line (BEOL) wiring showed no degradation of the underlying CMOS logic. Program and read operation were properly controlled resulting in 100% bit functionality at an operation voltage of 2.5 V and operating speed at 14 ns. This technology matches requirements of fast level cash (LLC) and embedded non-volatile-memory (NVM) in low power System-on-a-Chip (SoC) for IoT applications.

**Jun Okuno** was born in Osaka, Japan in 1982. He received the B.S. degree in engineering science in 2005 and M.S. degree in material physics from Osaka University. He has been with Sony Semiconductor Solutions since 2007 as a device engineer in research and development field. He has contributed to production of emerging CMOS image sensors and development of emerging memories such as ReRAM and FeRAM. His current research interest is an emerging memory of FeRAM based on ferroelectric hafnium oxide. He oversees a material engineering and a process integration for the device. He is specialized in material science, physics and technology of semiconductor device, product engineering and device characterization.

### TF2.2 A Novel Dual Ferroelectric Layer Based MFMFIS FeFET with Optimal Stack Tuning Toward Low Power and High-Speed NVM for Neuromorphic Applications

**Tarek Ali**, Fraunhofer IPMS Center Nanoelectronic Technologies, Germany

A novel MFMFIS FeFET based on dual MFM/MFIS integration in a single gate stack is reported. The external top and bottom contacts, dual ferroelectric (FE) layers, and tailored MFM/MFIS area ratio ($A_{FE}$) shows flexible stack tuning for improved FeFET performance. A tradeoff between maximized MFM voltage and weaker FET channel inversion is notable in the $I_{DSS}$ as $A_{FE}$ decreases. A dual FE layer enables maximized MW and fine control of its size when MFM/MFIS switching contribution is tuned through $A_{FE}$. Tuning extends to low voltage switching with maximized MW size and extremely linear current change over a wide dynamic range at high symmetry of synaptic potentiation/depression. Reliability in terms of variability, temperature effects, endurance, and retention is reported. The MFMFIS concept is thoroughly discussed with insight on optimal stack tuning for improved FeFET characteristics.

**Tarek Ali** received the B. E. in electronics and communication engineering from Minya University, Minya, Egypt in 2011, the diploma in nanoelectronics engineering from the information technology institute (ITI), Cairo, Egypt in 2013, and the joint Erasmus Mundus M.Sc. in nanoscience and nanotechnology from the Catholic University of Leuven and the Technical University of Dresden in 2016. Since 2017, He is pursuing a Ph.D. degree in the area of ferroelectric memory development with the Fraunhofer Institute for Photonic Microsystems (IPMS), Center nanoelectronic Technologies (CNT), Dresden, Germany. His current research activities cover the integration, and electrical evaluation of ferroelectric memories based on binary oxide ferroelectric materials. His research interests include the theory, design, and physics of semiconductor and memory devices.

### TF2.3 Improved State Stability of HfO$_2$ Ferroelectric Tunnel Junction by Template-Induced Crystallization and Remote Scavenging for Efficient In-Memory Reinforcement Learning

**Shosuke Fujii**, Kioxia, Japan

We investigated the effects of read current instabilities originated from depolarization field and charge trapping in HfO$_2$ ferroelectric tunnel junctions (FTJs) on the performance of in-memory reinforcement learning. We utilized, for the first time, remote scavenging to control interfacial layer thickness, combined with template-induced crystallization to stabilize the ferroelectric phase. These are found to improve both short-term and long-term stability of memory state. Pole-car simulation results reveal that these improvements significantly increase the efficiency and stability of reinforcement learning with the FTJ cross-point array, suggesting that in-memory reinforcement learning with the improved FTJ is a promising candidate for future compact and efficient reinforcement learning systems.

**Shosuke Fujii** received the B.S. (2005) and M.S. (2007) in materials science and engineering from Kyoto University, Kyoto, Japan. He joined Advanced LSI Technology Lab, Toshiba Corp., Yokohama, Japan, in 2007, where he was engaged in the research on reliability physics of MONOS memories. From 2009 to 2016, he was engaged in the research of emerging memory cell technology. From 2016 to 2018, he was a visiting scholar at Stanford University, where he studied scaling effects of resistive switching memories. He is currently with Kioxia Corporation (renamed from Toshiba Memory Corporation), where he is engaged in research and development of emerging memory devices for high-density applications. He served as vice chair of the memory reliability session in the IEEE International Reliability Physics Symposium in 2014 and 2015 and a tutorial lecturer in IEEE International Reliability Physics Symposium in 2016.
TF2.4 Nanosecond Laser Anneal (NLA) for Si-Implanted HfO2 Ferroelectric Memories Integrated in Back-End Of Line (BEOL)
Laurent Grenouillet, CEA-Leti-MINATEC, France

10nm Si-implanted HfO2 is demonstrated to be ferroelectric for the first time when integrated in a Back-End-Of-Line (BEOL) 130nm CMOS. Scaled 0.28μm² capacitors demonstrate excellent endurance (10^12 cycles measured at 4V, extrapolated to be 10^17 at 3V), with low coercive field distributions at wafer scale and excellent data retention at 85°C. To extend the ferroelectric BEOL compatibility of 10nm or thinner HfO2-based films, but also to understand their crystallization dynamics, nanosecond laser anneal is demonstrated to be very appealing, even for undoped HfO2.

Laurent Grenouillet received the Engineer degree in physics in 1998 from the National Institute of Applied Sciences (INSA) in Lyon, France, and the Ph.D. degree in electronic devices in 2001 for his work on the optical spectroscopy of diluted nitrides grown on GaAs substrates. After a post-doctoral position in the field of molecular beam epitaxy, he joined CEA-Leti in 2002 and worked on GaAs-based VCSELs emitting in the 1.1-1.3μm range and single photon sources with quantum dots. In 2006, he joined the Silicon Photonics group where he developed CMOS compatible hybrid III-V on silicon lasers. In 2009, he joined IBM Alliance in Albany as a Leti assignee to contribute to the development of FDSOI technology. Within Albany state-of-the-art facilities, he worked on device integration to improve performance of FDSOI devices (28nm and 14nm node). Back in France at CEA-Leti in 2013, he focused on the performance boosters for the 10nm node FDSOI technology, and took part to the FDSOI technology transfer to GlobalFoundries (22FDX) in 2015. During that period, he joined the Memory Component Laboratory at CEA-Leti. His current research interests include resistive switching memory devices and selectors, and ferroelectric memories. Dr. Grenouillet authored over 80 papers and has filed over 40 patents. He serves as a SSDM committee member.

TF2.5 Fast Thermal Quenching on the Ferroelectric Al: HfO2 Thin Film with Record Polarization Density and Flash Memory Application
Changhwan Choi, Hanyang University, Republic of Korea

We have investigated the effects of post cooling process with chamber cooling, air cooling and fast quenching in DI water on the ferroelectric (FE) characteristics of Al-doped HfO2 (Al:HfO2) thin films and demonstrated their potential flash memory applications. Compared with other cooling processes, using fast quenching after annealing we achieved the drastic increase of remnant polarization (P_r) and coercive electric field (E_c). The highest 2P_r and 2E_c are ~100 μC/cm² and ~9.5 MV/cm, respectively, the highest records among HfO2-based FE reported so far. These improvements are attributed to induce higher stress/strain within Al:HfO2 thin film, leading to stable orthorhombic phase (o-phase). Program/erase up to 10^10 cycles and 10 years retention characteristics are also evaluated for the potential flash memory application. Our simulation with experimental data indicates that P_r and E_c significantly can influence on the memory window and multi-bit states, which can be tuned by our proposed quenching process.

Changhwan Choi is a Professor of Materials Science and Engineering at Hanyang University, Seoul, Republic of Korea. He received the B.S. degree from Hanyang University, M.S. and Ph.D. degrees from the University of Texas at Austin, USA in 2000, 2002, and 2006 respectively. 2016-2017, Visiting Research Professor, Korea Institute of Science and Technology, Seoul, Republic of Korea. In 2006-2010, he was a Research Staff Member at the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA. His research interests are in nanoelectronic devices, materials and process development of Si-based device fabrication and characterization, advanced logic and memory technology (ReRAM, CBRAM, FeRAM), tunneling transistor, ferroelectric transistor, 3D device Integration (monolithic 3D, TSV), non-Si substrate device, post-Si devices, neuromorphic computing device, ALD oxide and metal process.

TF2.6 Multi-Probe Characterization of Ferroelectric/Dielectric Interface by C-V, P-V and Conductance Methods
Junkang Li, Purdue University, USA

In this work, we report on the multi-probe characterization of interfacial charges at the ferroelectric/dielectric (FE/DE) interface in response to both large-signal measurement associated with polarization switching and small-signal measurement without polarization switching. Charge densities at the FE/DE interface are extracted from temperature dependent C-V, P-V, conductance methods. It is found that the charge injection and accumulation at the FE/DE interface play a key role in the operation of FE/DE stack. These enormous trapped charges of 10^12-10^13 cm² at the FE/DE interface are supplied from the leakage current through the ultrathin DE layer. The proposed multi-probe measurement techniques provide a comprehensive understanding of FE/DE stack. The demonstrated leakage-assist polarization switching provides the new insights on the understanding of negative-capacitance (NC) effect and ferroelectric device performance.

Junkang Li received the B.S. degree in communication engineering from the Zhejiang University of Technology, Zhejiang, China, in 2013. He is currently pursuing the Ph.D. degree with Zhejiang University, Hangzhou, China and a visiting scholar at Purdue University, West Lafayette, IN, USA.

TF2.7 Probing the Evolution of Electrically Active Defects in Doped Ferroelectric HfO2 During Wake-Up and Fatigue
Umberto Celano, imec, Belgium

We correlate the concentration and configuration of electrical defects in ferroelectric Si-doped HfO2 (FE-HfO2) with the electrical device performance during wake-up and fatigue regimes. To this end, we combine time-to-breakdown (TDBB), Kelvin probe force microscopy (KPFM), conductive atomic force microscopy (C-AFM) and Scalpel SPM, probing for the first time, the nanoscopic material variations as a function of device’s field cycling behavior.

Umberto Celano is a Senior Scientist at imec (Belgium), with expertise in materials analysis for semiconductor technology, device physics and nanoscale functional materials. He received his Ph.D. in physics from the University of Leuven - KU Leuven (Belgium) in 2015. His research established a novel three-dimensional nanoscale imaging technique that combines sensing with sub-nm material removal to study materials in confined volumes. Currently, Dr. Celano’s research interests encompass nanoelectronics, nanophotonic, functional materials and VLSI metrology. In these areas, he conducted research in various institutions including KU Leuven, Osaka University and Stanford University. Umberto is the recipient of the Rogen A. Haken Best Paper Award at IEDM (2013) and has authored or co-authored 60+ papers in international journals and conference proceedings. He is part of the metrology working group for the International Roadmap for Devices and Systems (IRDOS) and has acted as member of the early carrier editorial board of Nano Letters. Previously, Umberto received his B.Eng. in electronic engineering and a M.Sc. degree in nanoelectronics with honors from the University of Rome Sapienza, Italy.
Direct, atomic-scale visualization of polarization switching in a functional, polycrystalline, binary oxide via in-situ high-resolution transmission electron microscopy (HRTEM) biasing is reported for the first time. Antiferroelectric (AFE) ZrO$_2$ was used as the model system, which is important for commercial DRAMs and as emerging NVMs (through work-function engineering). We observed (1) clear shifting and coalescing of domains within a single grain, and (2) dramatic changes of the atomic arrangements and crystalline phases—both at voltages above the critical voltage measured for AFE switching. Similar synergistic, in-situ structural-electrical characterization can pave the way to understand and engineer microscopic mechanisms for retention, fatigue, variability, sub-coercive switching and analog states in ferroelectric and AFE-based memory devices.

Sarah Lombardo is a doctoral student at the Georgia Institute of Technology in the Department of Materials Science and Engineering. Her work focuses on structural characterization of materials via transmission electron microscopy techniques. She received her B.S. degree in nanoscale engineering from the University at Albany's Colleges of Nanoscale Science and Engineering in 2016. She entered Georgia Tech's MSE department in Fall 2016.
TH1 Technology Session - 3D Packaging

Session Chairs: Michael DeLaus (Analog Devices), Tetsu Tanaka (Tohoku University)

On-Demand Availability: June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Related Live Event(s):
- ED3 - 3D Packaging - June-16 19:00 PDT / June-17 04:00 CET / June-17 11:00 JST (1 hour)
- EG1 - Heterogeneous Integration (2) - June-18 08:00 PDT / June-18 17:00 CET / June-19 00:00 JST (1 hour)

TH1.1 Low Temperature SoIC Bonding and Stacking Technology for 12/16-Hi High Bandwidth Memory (HBM)
(C. H. Tsai, TSMC, Taiwan)

A 12-high (12-Hi) die stack using low temperature SoIC bonding and stacking technology is presented and demonstrated for the application of HBM. The daisy chains in the 12-Hi structure incorporating over ten thousand TSVs and bonds are tested. Liner I-V curves are obtained to demonstrate the good bonding and stacking quality. The electrical link from a base logic die to top DRAM is built up to study the bandwidth and power consumption. Compared to μbump technology, the bandwidth for 12-Hi and 16-Hi structures using the SoIC technology shows the improvement of 18% and 20%, respectively and the power efficiency demonstrates the improvement of 8% and 15%, respectively. Also, the thermal performance for the 12-Hi and 16-Hi SoIC-bond structures are improved by 7% and 8%, respectively. Based on the proposed technology, the scalability of bond pitch to sub-ten μm and die thickness to be thinner is prospected.

Chung-Hao Tsai received the Ph.D. degree in communication engineering from National Taiwan University, Taiwan, in 2012. He is currently a technical manager with TSMC, Taiwan, in charge of SiP/RF design and modeling of 3DIC package and WLSI technology. In 2016, he received the Young Scientist Award of IEEE APEMC for outstanding contribution in the development of SiP technology for 5G mobile and high speed system application. He has over 40 US patents and published over 20 papers in the field.

TH1.2 3D Heterogeneous Package Integration of Air/Magnetic Core Inductor: 89%-Efficiency Buck Converter with Backside Power Delivery Network
(Xiao Sun, imec, Belgium)

We demonstrate a novel concept of integrating 110-µm-thick low-resistance high-Q magnetic core inductors in fan-out wafer level packaging (FOWLP). Unlike thin-film magnetic core inductors [1], this solution offers the possibility to embed thick cores to meet power density requirements, allowing for 89% efficiency at 1.2 W/mm² power density for 2:1 power conversion with a backside power delivery network (BSPDN) using circular-shaped magnetic inductors.

Xiao Sun received a Ph.D. degree in electrical engineering in 2001 from Université Grenoble Alpes, Grenoble, France. Since then, she has been a senior scientist at imec, Belgium. Her research interests include RF design, modeling and characterization for 3D interconnects and their impact on 3D ICs. She is also actively involved in heterogeneous integration and packaging for RF and 5G applications. She has (co)authored over 70 peer-reviewed journals and conference papers and one book chapter. She was the recipient of the prestigious outstanding session paper award from ECTC 2015.

TH1.3 Bumpless Build Cube (BBCube): High-Parallelism, High-Heat-Dissipation and Low- Power Stacked Memory Using Wafer-Level 3D Integration Process
(Norio Chujo, Tokyo Institute of Technology, IIR, WOW Alliance / Hitachi, Japan)

The superiority electrical performance of 3D integration (3DI) with bumpless wafer-on-wafer (WOW) was clarified by 3D electromagnetic (EM) field analysis. We propose a high parallelism stacked memory, named “BBCube” using WOW. In comparison with conventional high-bandwidth memory (HBM), BBCube can achieve a bandwidth four-times higher, at 1.4 TB/s, with only 13 % I/O power consumption, at 0.29W. Furthermore, it should have sufficient potential to realize 32-times higher bandwidth and four-times more stacking levels.

Norio Chujo has been in production engineering with the Center for Technology Innovation, Hitachi, Ltd. Resarch & Development Group, Center since 1989. His area of work is in SiP/RF design and modeling for high-speed and high-density PCB and LSI package technology.

TH1.4 ExaNoDe: Combined Integration of Chiplets on Active Interposer with Bare Dice in a Multi-Chip-Module for Heterogeneous and Scalable High Performance Compute Nodes
(Pierre-Yves Martinez, Université Grenoble Alpes, CEA-LIST, France)

In the context of high performance computing (HPC), energy efficiency and computing density are key for targeting exascale architectures. Close integration of chiplets, active interposer and field programmable gate arrays (FPGA) paves the way for dense, efficient and modular compute nodes. In this paper, we detail the ExaNoDe multi-chip-module (MCM) combining the integration of a substrate, an active interposer, some chiplets and bare dice. The reported MCM demonstrates that the multi-level integration flow enables tight integration of hardware accelerators in a heterogenous HPC compute node.

Pierre Yves Martinez is Project Leader at CEA-LETI, Grenoble, France. He received his engineering degree from the Chemistry Physic Electronic institute of Lyon (CPE Lyon) in 1993. He spent 17 years (1997 to 2014) at STMicroelectronics, mainly in the STB and mobile area, as designer, SoC integrator and design manager. After 4 years in Tunisia where he started a design activity and taught electronic within superior schools, he came back to Grenoble where he became CPU/GPU design team manager. He joined LETI in the digital design lab in 2014, working now as SoC project leader on diverse power efficient multi core architectures. He led the work package “Compute Node Design and Manufacture” of the ExaNoDe European project.
**TH1.5 Immersion in Memory Compute (ImMC) Technology**

*C.T. Wang, TSMC, Taiwan*

Immersion in Memory Compute (ImMC) technology with multiple chips and functions in multi-layer stacking integrated using System on Integrated Chips (SoIC™) technology is presented. The technology provides multiple compute and memory chips to interconnect each other to gain computing power and memory bandwidth. The interconnect parasitics, bandwidth density and power efficiency are analyzed using N7 light I/O transceiver. The ImMC compared with 3DIC with bridge and with shared die, respectively, using bump and TSV, is studied. The ImMC is 16x, 14x, and 224x better than the 3DIC with bridge in bump density, data rate, and bandwidth density. The transceiver power and size for the ImMC is only 1% of those for the 3DIC.

*Chuei-Tang Wang* received the B.S. and M.S. degrees in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1983 and 1985, respectively, and the Ph.D. degree from Stanford University, Stanford, CA, USA, in 1997. In 2011, he joined TSMC Integrated Interconnect and Packaging (IIP) RD team as a Technical Director for system architectures and their SI, PI and RF performance exploratory study. He had received a National Award of Industrial Technology Advancement (ITA), Taiwan, for the leadership of connectivity SiP module development in industry in 2007. He holds 60 US patents and publishes papers in IEDM, VLSI, ECTC, etc.

**TH1.6 Low Temperature Cu/SiO₂ Hybrid Bonding with Metal Passivation**

*Demin Liu, National Chiao Tung University, Taiwan*

Cu/SiO₂ hybrid bonding process with short duration (1 minute) has been successfully performed at low temperature (120°C) under the atmosphere with metal passivation material. Electrical performance (over 15K daisy chain and 10⁻⁸ Ω-cm² specific contact resistance), mechanical strength (>15 kgf), and reliability have been conducted to verify its excellent bonding quality. This method of hybrid bonding therefore provides a wide range of applications and a new solution for 3D integration.

*Demin Liu* received his bachelor’s degree in microelectronics engineering from Jiangnan University in 2015. He is currently a Ph.D. candidate of Department of Electronics Engineering in National Chiao Tung University, Hsinchu, Taiwan. He has been working in the field of 3D packaging, 3D integration, and hybrid bonding in Professor Kuan-Neng Chen’s group since 2015.
TH2 Technology Session - Semiconducting Oxides for 3D Integration

Session Chairs: Willy Rachmady (Intel), Yoshitaka Sasago (Hitachi)

On-Demand Availability

June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Executive Sessions for Interactive Discussions, Paper Elevator-Pitch Summaries and Q&A

ED1 - Heterogeneous Integration (1) - June-16 18:00 PDT / June-17 03:00 CET / June-17 10:00 JST (1 hour)

EG1 - Heterogeneous Integration (2) - June-18 08:00 PDT / June-18 17:00 CET / June-19 00:00 JST (1 hour)

Related Live Event(s)

TH2.1

BEOL Compatible Dual-Gate Ultra Thin-Body W-Doped Indium-Oxide Transistor with $I_{on}=370\mu A/\mu m$, $SS=73mV/dec$ and $I_{on}/I_{off}$ ratio $> 4\times 10^9$ (EG1)

Wriddhi Chakraborty, University of Notre Dame, USA

We experimentally demonstrate BEOL compatible (<250°C thermal budget) 1% W-doped amorphous In$_2$O$_3$ (IWO) back-gate (BGFET) and dual-gate (DGFET) field-effect transistors with 7nm channel thickness. The 100nm channel length IWO DGFET exhibits excellent subthreshold slope (SS) of 73mV/dec, record $V_{SAT}$ of 370µA/µm, and on-off ratio $> 4\times 10^9$ at $V_{DS}=1V$ and $V_{GS-VT}=2V$. We provide insight into the electrostatic gate control efficiency through temperature and frequency dependent admittance measurement. We identify fundamental transport mechanisms that limit electron mobility inamorphous IWO as a function of gate-bias ($V_{GS}$) and temperature. Benchmarking shows that IWO DGFET is a promising BEOL transistor for enabling high-performance monolithic three-dimensional (M3D) integrated circuits.

Wriddhi Chakraborty received his Bachelors' degree in electronics and telecommunication engineering from the Indian Institute of Engineering Science and Technology, Shibpur, India, in 2018. He is currently pursuing his Ph.D. degree in electrical engineering from University of Notre Dame, Indiana, USA, under Dr. Suman Datta. His current research focuses on cryogenic response of MOSFETs for quantum computing and high-performance computing applications, which involves experimental characterization and device modelling at cryogenic temperature. His research interest also includes investigation of higher-K oxide materials for gate-stack in advanced MOSFET technologies and Ferroelectric Field-effect transistor (FeFET) based neuromorphic hardware. He also received the DAAD-WISE scholarship (2017) for working on a summer research project for developing quantum-circuit synthesis algorithm at Universitat Bremen, Germany.

TH2.2

Surrounding Gate Vertical-Channel FET with Gate Length of 40nm Using BEOL Compatible High-Thermal-Tolerance In-Al-Zn Oxide Channel (ED1)

Hirokazu Fujiwara, Kioxia, Japan

We have demonstrated, for the first time, a surrounding gate vertical-channel FET with gate length of 40 nm by introducing back-end-of-line (BEOL) process compatible novel oxide semiconductor (OS) In-Al-Zn-O as a channel material. Fabricated FETs exhibited high scalability by excellent thermal stability (~ 420 °C) compared to conventional In-Ga-Zn-O-channel FETs, with high mobility (12.7 cm$^2$/V·s) characteristics. Furthermore, the vertical-channel FET also exhibited excellent reliability and stable operation without floating body effect. Endurance of over $10^{11}$ cycles was also demonstrated. Our work opens a pathway to realization of high-performance BEOL transistor for 3D-LSI applications.

Hirokazu Fujiwara received M.S. and Ph.D degrees in physics at the Graduate School of Natural Science and Technology, Okayama University. He started working for Toshiba Memory Corporation (currently Kioxia Corporation) in 2019. He has been continuously studied oxide materials.

TH2.3

Amorphous IGZO TFTs featuring Extremely-Scaled Channel Thickness and 38nm Channel Length: Achieving Record High $G_{m,\text{max}}$ of 125 µS/µm at $V_{DS}$ of 1V and $I_{ON}$ of 350µA/µm (ED1)

Subhranu Samanta, National University of Singapore, Singapore

We demonstrated amorphous indium-gallium-zinc-oxide thin film transistors (a-IGZO TFTs) with extremely scaled channel thickness ta-IGZO of 3.6 nm, achieving low SS of 74.4 mV/decade and the highest μeff of 34 cm²/V·s at carrier density $N_{carrier}$ of $\sim 5 \times 10^{12}$ cm$^{-2}$ for a-IGZO TFTs having sub-10 nm ta-IGZO. We found that there is no obvious degradation of mobility as ta-IGZO changes from 6 nm to 3.6 nm. By scaling down the channel length LCH to 38 nm, the devices have shown the highest extrinsic transconductance (Gm) of 125 $\mu S/\mu m$ (at VDS of 1V) and the highest on-state current $I_{ON}$ of 350$\mu A$/µm at $V_{GS} - VT$ of 3.0 V and VDS of 2.5 V for any kind of a-IGZO TFTs.

Subhranu Samanta received his Ph.D. in electrical engineering from Chang Gung University, Taiwan in 2018. Currently, he is working as a research fellow in ECE dept. of National University of Singapore. Dr. Samanta's research topic is amorphous semiconductor oxide based TFTs.
First Monolithic Integration of 3D Complementary FET (CFET) on 300mm Wafers

Sujith Subramanian, imec, Belgium

We report the first monolithic integration of 3D Complementary Field Effect Transistor (CFET) on 300mm wafers using IMEC’s N14 platform. A monolithic CFET process is cost effective compared to a sequential CFET process. The small N/P separation in a monolithic CFET results in lower parasitics and higher performance gains. In this paper, using a CFET fabrication process flow, we demonstrate functional PMOS FinFET bottom devices and NMOS nanosheet FET top devices. Process development of all the critical modules to enable these devices are presented. Monolithic CFET integration scheme could enable the ultimate device footprint scaling required in future technology nodes.

Sujith Subramanian received his Ph.D. in electrical engineering from the National University of Singapore. He is currently a Researcher and Development Engineer at imec, Belgium working on FEOL process integration for 14nm and below CMOS technology nodes.

3D Sequential Low Temperature Top Tier Devices Using Dopant Activation with Excimer Laser Anneal and Strained Silicon as Performance Boosters

Anne Vandooren, imec, Belgium

Top tier devices in a 3D sequential integration are optimized using a low temperature process flow (<525°C). Bi-axial tensile strained silicon is transferred without strain relaxation to boost the top tier nmos device performance by 40-50% over the unstrained silicon devices, recovering the performance loss from the low temperature processing when using extension-less device integration. Excimer laser anneal is also shown to effectively activate both n-type and p-type dopants in the extension of thin silicon film devices using optimized, CMOS compatible, laser exposure conditions. Laser anneal is fully compatible with a replacement metal gate (RMG) process flow and with selective source/drain (SD) epitaxy. The dopant activation level is preserved during the entire process flow which results in similar Ion-Ioff device performance for devices with laser and spike anneals. Excimer laser anneal benefits also from improved control short channel effects over spike annealing due to low dopant diffusion.

Anne Vandooren received her M.S. degree in electrical engineering from the Université Catholique de Louvain, Belgium in 1996 and her Ph.D. degree in electrical engineering from the University of California, Davis in 2000. She is currently working as a member of the technical staff at imec on advanced CMOS device integration.

28nm FDSOI CMOS Technology (FEOL and BEOL) Thermal Stability for 3D Sequential Integration: Yield and Reliability Analysis

Camila Cavalcante, CEA-Leti, France

For the first time, the thermal stability of a 28nm FDSOI CMOS technology is evaluated with yield measurements (5Mbit dense SRAM and 1 Million Flip flop). It is shown that 500°C 2h thermal budget can be applied on a digital 28nm circuit including State-Of-The-Art CuULK BEOL without yield nor reliability degradation. These results paves the way to the introduction of BEOL between tiers in 3D sequential integration while the thermal budget allowed for the top tier is sufficient to lead to high performance device.

Camila Cavalcante was born in 1989. She received her master's degree in nanoscale engineering from ECL (Ecole Centrale de Lyon), Lyon-Rhône-Alpes, France.

First Demonstration of Low Temperature (≤500°C) CMOS Devices Featuring Functional RO and SRAM Bitcells toward 3D VLSI Integration

Claire Fenouillet-Beranger, CEA-Leti-MINATEC, France

For the first time FDSOI CMOS transistors with Si-monocrystalline channel have been fabricated at a temperature below 500°C. High performance PMOS ($I_{ON}=450\mu A/\mu m$ ($V_{dd}=0.9V$) @ $I_{OFF}=2nA/\mu m$ $L_{g}=35nm$) with low overlap capacitance (0.46F/µm per device), low gate resistance (10Ω), enables to achieve good RF Figure-Of-Merit (FOM) with $f_{MAX}$ values up to 170GHz. In addition, we demonstrate for the first time the full functionality of Ring Oscillators (RO) and SRAM bitcells processed at 500°C, paving the way for a high-performance 3D sequential CMOS integration.

Claire Fenouillet-Beranger received the postgraduate diploma in microelectronics and Ph.D. degree from the Institut National Polytechnique de Grenoble, France, in 1998 and 2001, respectively. In 1998, she joined LETI, Grenoble, where she carried out her Ph.D. work on the integration and characterization of SOI devices. From 2001 to 2013, she worked as a CEA/Leti assignee in advanced R&D STMicroelectronics center, Crolles, France on FDSOI (Fully-depleted SOI) technology platform development and characterization. Since 2013, she is a senior scientist and works as the project leader of the low-temperature MOSFETs development for 3D sequential integration. In parallel, she is now a scientific delegate in her LETI department. In the frame of these activities, she received the Best Paper Awards at ESSDERC 2009 in Athens, and the best student paper at IEEE VLSI-TSA 2010 in Taiwan. She was also the co-recipient of the Grand Prix du Général Ferrié in 2012 for her work on FDSOI.
Flexible and Transparent BEOL Monolithic 3DIC Technology for Human Skin Adaptable Internet of Things Chips

Ming-Hsuan Kao, Taiwan Semiconductor Research Institute, Taiwan

For the first time, below 400°C-fabricated poly-Si MOSFETs and 6T-SRAM fabrication process was demonstrated on polyimide (PI) substrate for flexible and transparent monolithic 3DIC. Key enablers are 400-900 nm transparent laser-stop layer (LsL), laser-crystallized/CMP-thinned poly Si channel and pulse UV-laser S/D activation. These advanced low thermal budget fabrication technologies enable stackable poly-Si MOSFETs on flexible 6"-wafer-scale PI substrate with high device uniformity (V\text{th}/SS~16.2%/16.6%) and bending stability (V\text{th}/SS~4.2%/9.8%) after cycle-bending at radius of 10mm. Such CMOS compatible technologies envision flexible 3D heterogeneous integration of circuits/optical sensors for human-skin adaptable Internet of Things (IoT) chips.

Ming-Hsuan Kao was born in Pingtung, Taiwan, in 1986. She received the Ph.D. degrees from the Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2017. She is currently an Assistant Researcher with the Taiwan Semiconductor Research Institute (TSRI), Hsinchu, Taiwan. Her current research focuses on development and integration of flexible electronics.
An Extremely Scaled Hemi-Cylindrical (HC) 3D NAND Device with Large V<sub>e</sub> Memory Window (>10V) and Excellent 100K Endurance

**Pei-Ying Du**, Macronix International, Taiwan

We report an extremely scaled HC 3D NAND device with large memory window. The proposed cell area is only ~32% of the standard GAA 3D NAND cell area, while it can produce very large >10V memory window with excellent 100K endurance. We also study the size effect of HC device. It is found that the larger HC device may easily suffer parasitic edge leakage effect that causes programming saturation. A "wake-up" effect by strong –FN erasing can introduce gate injected electrons that electrically suppress the parasitic edge and in turn "wake-up" the device to produce larger programming window. On the other hand, the smaller HC device already shows excellent memory window without the need of wake-up. Good post-cycled retention and RTN performance are demonstrated for an extremely scaled HC device. Our results suggest a promising path of 3D NAND device to enjoy both aggressive dimension scaling and large memory window.

Pei-Ying Du received her B.S. degree in engineering and system science from National Tsing-Hua University (NTHU), Hsinchu, Taiwan, in 2004, and Ph.D. degree in electrical engineering from National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 2009. She joined the Emerging Central Lab. (ECL) in Macronix International, Hsinchu, Taiwan, in 2006, where she engaged in the theoretical modeling and reliability physics of nitride trapping Flash memory. From 2010 to 2012, she was assigned to IBM/Macronix Phase Change Memory (PCM) Joint Project in IBM T.J. Watson Research Center, NY, and engaged in PCM reliability. She currently is the deputy department manager of nano-technology R&D department developing 3D nitride trapping NAND Flash memory. Dr. Du has published more than 50 papers in premier conferences and journals including IEDM, Symposium on VLSI Technology, IRPS, IMW, T-ED, and etc. She is well-recognized in memory reliability, in particular on nitride trapping memories. Dr. Du served in the program committee of International Memory Workshop (IMW) from 2012 to 2016, and was the Local Chair and the Short Course Chair of IMW, in 2014 and 2015, respectively. She also served in the IEDM Memory Technology (MT) sub-committee from 2017 to 2018. She has been serving as Associate Editor of IEEE-TED since 2018.

An Approach to Embedding Traditional Non-Volatile Memories into a Deep Sub-Micron CMOS

**Chia-Sheng Lin**, TSMC, Taiwan

This work presents an example of 16nm FinFET CMOS with an embedded flash 40nm memory employing Wafer-on-Wafer (WoW) technology. Our results show comparable embedded flash performance, CMOS logic speed and power consumption comparing corresponding circuits before and after the 3D assembly. WoW integration can provide embedded flash solution for advanced CMOS nodes where no solutions currently exist. The method is also applicable for embedding other functionalities into the advanced CMOS.

Chia-Sheng Lin was born in Taiwan in 1982. He received the Ph.D. degree in electrical engineering in 2011 from National Sun Yat-Sen University, Taiwan. In 2011, he joined Taiwan Semiconductor Manufacturing Company (TSMC), where he is currently an embedded technology integration engineer in the R&D department. His research interests include new non-volatile memory device development and solutions for integration with advanced CMOS nodes.

A Vertical 2T NOR (V2T) Architecture to Enable Scaling and Low-Power Solutions for NOR Flash Technology

**Hang-Ting Lue**, Macronix International, Taiwan

In this work, we developed a new vertical 2T (V2T) NOR Flash architecture that provides not only scaling capability but also low-power solutions for NOR Flash technology. We leveraged the process of standard 3D NAND to develop a vertical 2T NOR that produces even smaller cell size than conventional planar 1T NOR. Advanced high-K metal-gate (HKMG) integration is developed to provide high-performance BE-MANOS charge-trapping device with excellent 1M endurance and retention reliability. The 2T NOR architecture provides low-voltage read (~1V) that is compatible with advanced CMOS circuits without charge pumping to save power. We also suggest future technology extensions of the V2T NOR by adopting the ferroelectric memory devices (FeFET) and the 3DIC chiplets integration to broaden the applications fields of NOR technology in embedded Flash and computing in memory (CIM).

Hang-Ting Lue is currently a project director in Macronix, leading an advanced research team in various innovative 3D memory architectures to pursue high-performance and functional memory devices. He is currently a technical committee member in the VLSI Symposia since 2011. He has published over 130 IEEE papers in various prestigious semiconductor conferences and journals, and owns >100 US granted patents.
Understanding of Tunable Selector Performance in Si-Ge-As-Se OTS Devices by Extended Percolation Cluster Model Considering Operation Scheme and Material Design

Shoichi Kabuyanagi, Kioxia, imec, Japan

Switching mechanism and its controllability in Ovonic Threshold Switching (OTS) devices are systematically investigated by using Si-Ge-As-Se quaternary system known as promising OTS materials, considering the impacts of switching pulse waveform and OTS material composition. We newly demonstrate that selector device performance is flexibly tunable by controlling fall time of switching pulse as well as operation current. Meanwhile, As- and Si-incorporation are found to be beneficial in terms of stable operation and faster recovery. All results are consistently understandable by extended percolation cluster model, supported by ab-initio molecular dynamics and Monte-Carlo simulations. These findings are of utmost practical importance for controlling and designing actual circuits operation with high-density and energy efficient cross-point array.

Shoichi Kabuyanagi received the B.S. (2011), M.S. (2013) and Ph.D. (2016) degrees in materials science and engineering from The University of Tokyo, Tokyo, Japan, investigating the semiconductor device physics of germanium metal-oxide-semiconductor gate stack. He joined the Advanced LSI Technology Lab, Toshiba Corp., Kawasaki, Japan, in 2016, where he started his work on the research and development of emerging memory device technology. He is currently with Kioxia Corporation (renamed from Toshiba Memory Corporation) and has been assigned at Interuniversity Microelectronics Centre (IMEC), Leuven, Belgium, as a device researcher, since 2018. His main activities have been related to the electrical and reliability characterization of emerging memories such as ferroelectric memory, phase change memory and ovonic threshold switching devices.

A No-Verification Multi-Level-Cell (MLC) Operation in Cross-Point OTS-PCM

Nanbo Gong, IBM T. J. Watson Research Center, USA

We present the first MLC operation for OTS-PCM with comprehensive operation algorithm study. An ADM chip with fast write speed (<300ns) and robust operation (>10^9 cycles) are shown indicating the potential for high performance MLC OTS-PCM. A desirable 2-bits/cell operation up to 10^8 cycles without further read verification is achieved based on 100 cells data from 1Mbit crosspoint array. Systematic discussions of MLC operation under “1/2V” scheme is further presented, and threshold voltage (Vt) drift is evaluated accordingly.

Nanbo Gong received his B.S. degree in physics from Yuanpei College, Peking University, China, in 2013, M.S. and Ph.D. degrees in electrical engineering from Yale University, US, in 2015, and 2018, respectively. He became a Research Staff Member in IBM T.J. Watson Research Center in 2018 and his research interests include phase change memory and selector for 3D crosspoint memory, analog computing, and HfO2-based ferroelectric memory.

Si Incorporation Into AsSeGe Chalcogenides for High Thermal Stability, High Endurance and Extremely Low Vth Drift 3D Stackable Cross-Point Memory

Huai-Yu Cheng, Macronix International, Taiwan

By incorporating Si into AsSeGe system, we demonstrate a 3D stackable OTS+PCM memory in a 1k by 1k cross-point memory array with extremely low Vth drift (~0V after 3 days from programming), wide Vd/Vr window (>2V main distribution memory window), high endurance (>2E11 cycles), excellent Ioff and thermal stability. So far, attempts to improve the thermal stability of AsSeGe system sacrifice Ioff and cycling endurance. We show that Si incorporation relaxes this trade-off and can greatly improve the thermal stability and cycling endurance while also achieving good Ioff. In particular the Ioff of AsSeGeSi selector is improved over the AsSeGe system for films of 20 nm.

Huai-Yu Cheng received her B.S., M.S., and Ph.D. degrees in materials science and engineering from National Tsing Hua University, Taiwan, in 2001, 2003, and 2007, respectively. She joined Macronix International Co., LTD in 2007 and is currently a Senior Researcher based in Yorktown Heights, New York. Her research interests include phase change materials and selector materials for 3D crosspoint memory. She has published two review articles, one book chapter, and more than 70 conference and journal papers including 12 invited papers. Dr. Cheng has over 18 granted US patents.
Weier Wan, Chang-Feng Yang, The energy efficiency of RRAM-based in-memory matrix-vector multiplication (MVM) depends largely on the output sensing mechanism. We design a novel voltage-mode sensing scheme with differential-row weight mapping for energy-efficient RRAM-based in-memory computing.

Irene Munoz-Martin, Politecnico di Milano, Italy
Biological systems autonomously evolve to maximize their efficiency in a continually changing world. On the other hand, artificial neural networks (ANNs) outperform the human ability of object recognition but cannot acquire new information without forgetting trained tasks. To introduce resilience in ANNs, we present a SiO$_2$-RRAM-based inference hardware capable of merging the efficiency of convolutional ANNs and the plasticity of spiking networks. We validate the accuracy of the system with MNIST (99.3%), noisy N-MNIST (96%), Fashion-MNIST (93%) and CIFAR-10 (91%) datasets. We demonstrate that the circuit plastically adapts its operative frequency for power saving and enables continual learning of up to 50% non-trained classes. This optimizes the classification and enables the re-training of the filters, thus overcoming the catastrophic forgetting of standard ANNs.

Weier Wan, Stanford University, USA
The energy efficiency of RRAM-based in-memory matrix-vector multiplication (MVM) depends largely on the output sensing mechanism. We design a novel voltage-mode sensing configuration with differential-row weight mapping that achieves a 3.6× improvement in energy per multiply-accumulate (MAC) at the same read voltage compared to current-mode sensing, and avoids the nonlinear source-line dynamics issue that occurs in conventional voltage-mode sensing. We verify the MVM performance of our scheme by performing measurements using a RRAM array monolithically integrated with CMOS voltage-mode neurons. We compare the effects of weight normalization on MVM accuracy under two different weight mapping schemes, and find that scheme 1 achieves higher accuracy when weights are sparse and the L-1 weight norm is consistent across the columns.

Chang-Feng Yang, TSMC, Taiwan
The read disturb performance and industrially applicable model of mega-bit embedded RRAM with standard 28 nm select transistor are demonstrated in this study. At first, 100k endurance test on 0.5 Mb RRAM 1T1R array is implemented and non-degraded memory window with high read disturb immunity results are acquired. Contrary to conventional analysis on major bits, the read disturb model is especially investigated on tail bits in this work. Furthermore, the read disturb performance for chip user condition with nano-second level pulse width is well emulated by long pulse, which provides a time-efficient way to evaluate read disturb performance at product level. As a consequence, the mega-bit 28 nm RRAM array in this work is able to sustain larger than 1E18 read counts at a rigorous fail criteria.
TM3 Technology Session - Memory - STT MRAM

Session Chairs: Klaus Knobloch (Infineon), Masahiko Kanda (Toshiba Electronic Devices & Storage)

On-Demand Availability

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Related Live Event(s)

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TM3.1 Scalability of Quad Interface p-MTJ for 1X nm STT-MRAM with 10ns Low Power Write Operation, 10 years Retention and Endurance > 10^11

Sadahiko Miura, Tohoku University, Japan

We have fabricated quad-interface perpendicular MTJ (Quad-MTJ) down to 33nm with our developed PVD, RIE and damage control integration process technologies under 300nm process. We demonstrated scalability merit as well as high speed writing of Quad-MTJ compared with double-interface p-MTJ (Double-MTJ) as follows; a) two times larger thermal stability factor (1Xnm Quad-MTJ is extrapolated to achieve 10 years retention.), b) lower write voltage at short write pulse regions at less than 30ns, c) in scaled MTJ, effective suppression of write current increase for higher write speed, d) more than 2 times higher write efficiency at 10ns write operation down to 33nm MTJ. We revealed that our developed 33nm Quad-MTJ achieve excellent endurance of more than 10^11 thanks to higher write efficiency and low damage integration process technology. These results show that the Quad-MTJ technology is one of promising way for low power, high speed and enough reliable STT-MRAM with excellent scalability down to 1Xnm node.

Sadahiko Miura received the M. S. degree in applied physics and the D. E. degree from Waseda university, Tokyo, Japan, in 1986 and 2000, respectively. His doctoral research focused on superconducting materials and devices. His research interests included MRAM devices, integration, and characterization. He joined NEC Corporation, Tsukuba, Japan, in 1986. From 2011 to 2014, his research group which investigated MRAM devices and circuits collaborated with Tohoku university. Since 2014, he has been at the Center for Innovative Integrated Electronic Systems, Tohoku University and researched in MRAM electrical characterization.

TM3.2 Reliability Demonstration of Reflow Qualified 22nm STT-MRAM for Embedded Memory Applications

Chia-Yu Wang, TSMC, Taiwan

We demonstrate the reliability of reflow qualified embedded STT-MRAM integrated on 22nm. STT-MRAM is capable of 1E5 endurance cycles across temperature (-40/25/125°C) with extremely low BER (mean 0.04 ppm, -40°C) and can pass 1M cycles by an enhanced process. BERs post three cycles of 260°C solder reflow are below 1 ppm for AP/P states. Due to high energy barrier for flipping states, chips can meet the retention lifetime spec (>200°C at 10yrs, BER 1 ppm) with a large margin. The balance of retention between AP and P can be adjusted in an optimized process. In addition, we investigate the impact of magnetic field applied at tilted angles and report standby immunity can reach 600 Oe at 125°C for 10 years for fields tilted 60 degrees from parallel to the die surface. Magnetic shields are demonstrated to sustain data exposed to perpendicular fields up to 3.5k Oe at 25°C, 100 hours.

Chia-Yu Wang is currently a Senior Engineer with Quality and Reliability, TSMC, Taiwan, where he is involved in reliability test methodologies and environment development for MRAM.

TM3.3 Fast Switching of STT-MRAM to Realize High Speed Applications

Tae Young Lee, GlobalFoundries, Singapore

We demonstrate less than 10 ns write speed and read access for 40Mb embedded MRAM (eMRAM) macro covering high temperature up to 125°C. The macro shows unpowered data retention of 10 second at 125°C and the capability of achieving 10^12 cycles endurance and 5 ns read time. Our study indicates that MTJ stack engineering and MTJ CD optimization are the two critical factors to achieve the suppression of bit error rate (BER) ballooning and 0.5x ic scaling for fast switching.

Tae Young Lee, Ph.D., is a Member of Technical Staff at TD-MRAM of GLOBALFOUNDRIES (Singapore), where he leads STT-MRAM device technology and develops new MTJ stacks including both eFlash and and SRAM type eMRAM together with Kazutaka Yamane (MTJ PVD module Leader, PMTS). In particular, Dr. Lee demonstrated magnetic immunity guideline to realize mass production for the first time and has a deep study to understand for fast switching of STT-MRAM. He really enjoys thinking and like discussion about MRAM's future.

TM3.4 A Reliable TDDB Lifetime Projection Model Verified Using 40Mb STT-MRAM Macro at Sub-ppm Failure Rate to Realize Unlimited Endurance for Cache Applications

Vinayak Bharat Naik, GlobalFoundries, Singapore

We report a reliable TDDB lifetime projection model using power law verified from 40Mb STT-MRAM macro data at sub-ppm failure rate to realize nearly unlimited endurance for cache applications. A specially designed macro, having internal temperature control systems and capable of applying accelerated voltage at 40Mb array level with wide operating temperature range: -40 to +125 °C and varying pulse widths: 200~10 ns, is used for the study. We demonstrate superior endurance performance of >1E12 cycles at 1 ppm failure rate using 40Mb macro combined with SRAM-like MTJ stack with lower operating voltage at BER ~ 1 ppm at 10 ns write pulse.

Vinayak Bharat Naik received the Ph.D. degree in physics from the National University of Singapore in 2011. He is currently a MRAM Device lead at GlobalFoundries (2014 to present), Singapore. Prior to joining GlobalFoundries, he was working as a Scientist at Agency for Science, Technology and Research (A*STAR), Singapore (2011-2014) on conventional and voltage-controlled STT-MRAM development. He has published close to 50 technical papers in international journals/conferences, and holds more than 15+ U.S. patents in the field of Non-volatile memory technologies.
TMFS Technology Memory Focus Session -
MRAM Future - Opportunities Beyond STT

Session Chairs: Franck Arnaud (STMicroelectronics), Hang-Ting Lue (Macronix International)

On-Demand Availability

June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Related Live Event(s)

Executive Sessions for Interactive Discussions, Paper Elevator-Pitch Summaries and Q&A

EC1 - Memory (2) - June-16 09:00 PDT / June-16 18:00 CET / June-17 01:00 JST (1 hour)

EH1 - MRAM - June-18 17:00 PDT / June-19 02:00 CET / June-19 09:00 JST (1 hour)

TMFS.1 Recent Progresses in STT-MRAM and SOT-MRAM for Next Generation MRAM

Invited
Tetsuo Endoh, Tohoku University, Japan

In last decade, since high performance MTJ using CoFeB/MgO-based interfacial perpendicular magnetic anisotropy (IPMA) is utilized, STT-MRAM technology has rapidly progressed and mass-production of STT-MRAM has already started in the semiconductor companies. However, for further expansion of MRAM applications and markets, higher reliability, larger capacity or speed are required. In this invited paper, we describe our recent progresses in STT-SOT-MRAM fabricated under developed 300mm integration process (PVD, RIE, etc.) [4] with advanced spintronics device technologies, such as quadrant-interface MTJ [10] and canted SOT device [12].

Tetsuo Endoh joined the ULSI Research Center Toshiba Co. in 1987 and was engaged in the R&D of NAND Memory. He became a lecturer at the Research Institute of Electrical Communication, Tohoku University in 1995. He is a professor at the Department of Electrical Engineering, the Graduate School of Engineering, Tohoku University and Director of the Center for Innovative Integrated Electronic Systems (CIES). His current interests are novel 3D structured device technology, such as vertical MOSFETs; high-density memory, such as SRAM, DRAM, 3D-NAND memory and STT-MRAM; and beyond-CMOS technology, such as spintronics-based non-volatile logic for ultralow power systems such as mobile systems, AI systems and IoT systems. He is also interested in power-management technology, such as GaN on Si based power devices and power integrated circuits with high efficiency and high power consumption for automotive applications. He received the 14th Prime Minister's Award for contribution to Industry-Academia-Government-Colaboration in 2016. He received 2017 National Invention Award for "the 21st century Encouragement of Invention Prize".

TMFS.2 Magnetic Random Access Memories (MRAM) Beyond Information Storage

Invited
Ricardo Sousa, Université Grenoble Alpes / CEA / CNRS, SpinTec, France

Magnetic random access memory (MRAM) is now available as embedded memory from major CMOS foundries. In this study, we demonstrated that slightly modified magnetic tunnel junctions than those used in conventional STT-MRAM can be used for multifunctional purposes, namely magnetic field sensing and RF oscillators. For that, the FeCoB storage layer thickness in the perpendicular anisotropy magnetic stack was adjusted to 1.3-1.4 nm, closer to the transition region from perpendicular to in-plane anisotropy. Two possible configurations of magnetic field sensing using the same stack can be used, achieving high sensitivity in small field range or lower sensitivity in large field range. Additionally, RF oscillator GHz detection and generation were also demonstrated. Further applications of this multifunctional stack can be envisioned including non-volatile and reprogrammable logic, special functions such as random number generator and memristors.

Ricardo Sousa is Research Engineer at CEA-Grenoble in France working in the field of MRAM for over 20 years. He received his Ph.D. degree (2003) in applied physics from the Instituto Superior Técnico in Lisbon and his Habilitation (2017) from Université Grenoble Alpes for his work on MRAM. He has been leading the MRAM group at SpinTec since 2008 to develop MRAM concepts like thermally assisted-MRAM with Crocus Technology and shape anisotropy MRAM cells scaling below 10nm. In 2017, his patents and MRAM test know-how led to the creation of the start-up company Hprobe. He worked recently (2017-2018) as a CEA assignee at GlobalFoundries on 22FDX technology for mmWave RF devices. He currently contributes to projects targeting MRAM hybrid circuits and spintronics-photonics integration.

TMFS.3 CMOS Compatible Process Integration of SOT-MRAM with Heavy-Metal Bi-Layer Bottom Electrode and 10ns Field-Free SOT Switching with STT Assist

Invited
Noriyuki Sato, Intel, USA

This paper demonstrates a CMOS compatible process integration of spin-orbit torque (SOT) device with a unique bi-layer SOT bottom electrode. An effective spin-Hall angle of 0.27, a median tunneling magnetoresistance ratio of 127% at electrical CD of 57 nm, and a 96% resistance-based MTJ yield on 300 mm scale were achieved. We experimentally validated the two-pulse field-free SOT switching scheme with spin-transfer torque assist at 10 ns. Unlike conventional field-free SOT switching schemes, the demonstrated scheme adds no complexity to process integration.

Noriyuki Sato is currently a component research engineer at Intel Corporation. Noriyuki received his B.Sc. and M.Sc. degrees from Tohoku University in 2010, 2012 and Ph.D. degree from Stanford University in 2017.

TMFS.4 Deterministic and Field-Free Voltage-Controlled MRAM for High Performance and Low Power Applications

Invited
Yueh Chang Wu, imec, Belgium

We propose a deterministic VCMA writing concept that allows exclusion of the pre-read which is required in conventional VCMA write scheme. We apply it on 400°C compatible PMTJ devices with high TMR 246% and retention Δ = 54 and demonstrate a genuine ns-scale write speed. Furthermore, we realize reliable 1.1GHz external field-free VCMA switching with 20fJ write energy by integrating a magnetic hard mask as the in-plane magnetic field generator. An endurance of more than 10^{10} cycles is achieved. Our results address the fundamental write operation challenges of the voltage-controlled MRAM technologies.

Yueh Chang Wu received the M.S. degree in nanoscience, nanotechnology and nanoeengineering from Katholieke Universiteit Leuven (KU Leuven), Belgium, in 2016. He is currently a Ph.D. student working with the Memory Device Design, imec, Belgium, and the Department of Electrical Engineering (ESAT), KU Leuven, Belgium. His research interests focus on characterization of MRAM devices for high-speed and low-power applications.
We demonstrated a novel true random number generator (TRNG) utilizing stochastic short-term recovery of Charge-Trapping (CT) FinFET devices. The true random number generator is designed and evaluated. All the generated random numbers pass the National Institute of Standards and Technology (NIST) tests and exhibit negligible bias and correlation free random bits; iii) the proposed oscillator phase TRNG is a generic design, independent of the oscillator platform. Thus, a CMOS ring oscillator based TRNG is also designed and evaluated. All the generated random numbers pass the National Institute of Standards and Technology (NIST) tests and exhibit negligible bias and correlation from statistical analysis. Therefore, the proposed solution provides a competitive alternative to the existing on-chip TRNG design toolbox.

Chia-Che Chung was born in Taiwan in 1995. He received the B.S. and M.S. degrees in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2017 and 2019 respectively, where he is currently pursuing the Ph.D. degree. His current research interest lies in ion sensors and CMOS photodetectors.

Chien-Ping Wang was born in Taiwan in 1995. He received the B.S. and M.S. degrees in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2017 and 2019 respectively, where he is currently pursuing the Ph.D. degree with the Graduate Institute of Electronics Engineering. His current research interests include the device- and circuit-level self-heating modeling and electrical simulation of 3-D transistors.

Jianguo Yang is an associate professor in the Key Laboratory of Microelectronics Devices and Integrated Technology at Institute of Microelectronics of the Chinese Academy of Sciences. His research interests include circuit designs for volatile and nonvolatile memory, hardware security, memory-centric computing, and memristor logics. He has authored or co-authored several technical papers such as JSSC, Symposium on VLSI, TVLSI, TCAS-II, ASSCC, ISCAS, ESSCIRC and ESSDERC. Some of his recognitions include two Best Paper Awards from the IEEE International Conference on ASIC on high-performance memory circuit design. He has participated in several large industry and government-sponsored center-level projects. He earned a Ph.D. degree from Fudan University, Shanghai, China.

Kai Ni received the B.S. degree in electrical engineering from University of Science and Technology of China, Hefei, China in 2011, and Ph.D. degree of electrical engineering from Vanderbilt University, Nashville, TN, USA in 2016, working on characterization, modeling, and reliability of III-V MOSFETs. Since then, he became a post-doctoral associate at University of Notre Dame, working on ferroelectric devices for nonvolatile memory and novel computing paradigms. He is now an assistant professor in Microsystems Engineering at Rochester Institute of Technology. He has around 60 publications in top journals and conference proceedings, including Nature Electronics, IEDM, VLSI Symposium, IRPS, and EDL. His current interests lie in nanoelectronic devices empowering unconventional computing, AI accelerator, security and 3D memory technology.
1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy

Xu Bai, NEC, Japan
1.5x energy-efficient and 1.4x operation-speed, nonvolatile via-switch (VS) FPGA with atom switch and a-Si/Si/N/Si varistor is demonstrated in a 65nm-node for various basic applications. For rapid and low-cost migration from VS-FPGA to ASIC, “hard-via” to replace VS with “ON”, named VS-copy (VSC), is newly proposed. The VSC-ASIC is fabricated by sharing all the photo masks with VS-FPGA excepting one via mask revise and three VS masks skip, realizing an exact design copy with minimum NRE cost and TAT. The VS-FPGA equipped with the VSC gives energy-efficient edge device, e.g., for up-to-date AI inference algorithms, covering a wide range of chip volume with extremely low cost.

Xu Bai is a senior researcher at NEC’s System Platform Research Laboratories. He has a Ph.D. degree in information sciences from Tohoku University. His research interests include reconfigurable computing, nonvolatile memory, new concept VLSI including multiple-valued VLSI computing. He received the IEEE Student Award in 2010, the Excellent Student Poster Award at 22nd International Workshop on Post-Binary ULSI Systems in 2013, and the SSDM Young Researcher Award in 2016. He is a senior member of the IEEE and a member of the IEICE.

Proposal and Experimental Demonstration of Reservoir Computing Using Hf\textsubscript{0.5}Zr\textsubscript{0.5}O\textsubscript{2}/Si FeFETs for Neuromorphic Applications

Eishin Nako, University of Tokyo, Japan
We propose a new AI calculation scheme by reservoir computing utilizing the memory effect and non-linearity of ferroelectric gate MOSFETs (FeFETs) for neuromorphic applications. Reservoir computing is promising owing to its unique characteristics such as low-power consumption, real-time machine learning and high potential capability of information processing with time-series data. The proposed reservoir computing system utilizes the drain current of a FeFET reservoir in response to time-series input data applied to the gate as gate voltage and the drain current sampled at a constant time is used as virtual nodes. The operations of short terms memory and parity check tasks, inherent to polarization, are experimentally demonstrated by using Hf\textsubscript{0.5}Zr\textsubscript{0.5}O\textsubscript{2}/Si FeFETs. The memory capacity, an index of reservoir computing performance, is dependent on gate voltage swing to control polarization. A high ability to classify input data is also experimentally verified by t-SNE (t-distributed Stochastic Neighbor Embedding) analyses.

Eishin Nako is currently studying in the Electrical Engineering Department of the University of Tokyo.

High On-Current 2D nFET of 390 μA/μm at V\textsubscript{DS} = 1V using Monolayer CVD MoS\textsubscript{2} without Intentional Doping

Ang-Sheng Chou, TSMC, Taiwan
We demonstrate the highest nFET current of 390 μA/μm at V\textsubscript{DS} = 1V based on CVD MoS\textsubscript{2} monolayers without intentional doping. The transistor exhibits good subthreshold swing of 109 mV/decade, large I\textsubscript{ON}/I\textsubscript{OFF} ratio of 4 \times 10\textsuperscript{8}, and nearly zero DIBL. The high on-current achieved in monolayer MoS\textsubscript{2} nFET is mainly attributed to the thin EOT ~2 nm of HfO\textsubscript{2} gate oxide, short gate length of 100 nm, and low contact resistance ~1.1 kΩ-μm.

Ang-Sheng Chou received the B.S. degree in the department of photonics from National Cheng-Kung University (NCKU), Tainan, Taiwan in 2014. He is currently pursuing his Ph.D. degree in the Graduate Institute of Photonics and Optoelectronics at National Taiwan University (NTU), Taipei, Taiwan. He is also a research intern at Taiwan Semiconductor Manufacturing Company (TSMC) responsible for the studies of low-dimensional material devices. His research interests include the growth of high-quality and large-area carbon nanotube and graphene materials, the fabrication and measurement of small-scaled two-dimensional (2D) material transistors by e-beam and helium-ion-beam lithography, and the surface and interface analyses of metal contact on 2D materials by photoemission spectroscopy (PES).

Ultrahigh Responsivity and Tunable Photogain BEOL Compatible MoS\textsubscript{2} Phototransistor Array for Monolithic 3D Image Sensor with Block-Level Sensing Circuits

Chih-Chao Yang, Taiwan Semiconductor Research Institute, Taiwan
A large-area and scalable monolayer TMD is feasible to employ in monolithic 3D image sensor scheme. For the first time, we represents a prototype MoS\textsubscript{2} phototransistor array with ultrahigh responsivity (>10\textsuperscript{5} A/W) and tunable photogain (10\textsuperscript{2}~10\textsuperscript{5}) which can be directly implemented on a CMOS circuit connected with BEOL fine-pitch vertical interconnects. Electric gate pulse modulation mitigates photogating (PG) and persistent photocurrent (PPC) effects from layered semiconductor interface. Both three-order-of-magnitude improvements of response speed and fine-pitch vertical interconnects empower block-level compressive sensing circuits and global image-signal processing for gain control and data compression.

Chih-Chao Yang received his Ph.D. degree from the Institute of Electronics Engineering at National Tsing Hua University, Hsinchu, Taiwan. He is currently an associate researcher of chip integration technology division in Taiwan Semiconductor Research Institute (TSRI). His research interests include the development of monolithic 3D device and advanced integrated circuit for artificial intelligence and internet of things. He is now integrating various functional devices, including advance monolayer TMD phototransistor, for heterogeneous integration system.

GaN PMIC Opportunities: Characterization of Analog and Digital Building Blocks in a 650V GaN-on-Si Platform

Wan Lin Jiang, University of Toronto, Canada
This paper reports the performance of GaN based building blocks for monolithic integration. An integrated gate driver, low-voltage analog and synchronous digital circuits are fabricated in a 650-V GaN-on-Si process and measured. Calibrated GaN models are compared against simulated silicon designs to identify optimal integration criteria.

Wan Lin Jiang received the B.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, Canada in 2018. She is currently working toward the M.A.Sc. degree in electrical engineering at the University of Toronto. Her research interests include GaN applications in power electronics and design of mixed-signal integrated power converters.
Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures Down to 100mK for Quantum Computing

(卒業生)
Bruna Paz, CEA-Leti-MINATEC, France

Variability of 28nm FD-SOI transistors is evaluated for the first time down to ultra low temperatures (ULT), at T=100mK. High performance is achieved at ULT for short channel transistors, with $I_{ON}>1mA/µm$ and $I_{OFF}$ below the equipment accuracy $<1$fA, in particular by keeping advantage of forward back biasing (FBB), with the same efficiency from room temperature (RT) down to 100mK. The physical origins of MOSFET mismatch at ULT are studied, highlighting the impact of the charge fluctuations increase on both threshold voltage ($V_{TH}$) and current gain factor ($β$) variabilities. Besides that, we demonstrated that the increase of $V_{TH}$ and $β$ variabilities at low temperature remains reasonably low in comparison to RT values and other CMOS technologies, so that it should not be detrimental to circuit operation in this range of temperatures.

Bruna Paz received her Ph.D. in electrical engineering in 2018 from FEI University, Brazil. She is currently a post-doctoral researcher at CEA-LETI, Grenoble, France, acting on the following subjects: quantum computer, cryogenic CMOS, ultra low temperature, electrical characterization, FD-SOI, and advanced MOSFETs. Dr. Paz has authored and co-authored 11 articles and 18 papers published in international conferences.

Toward Long-Coherence-Time Si Spin Qubit: The Origin of Low-Frequency Noise in Cryo-CMOS

(卒業生)
Hiroshi Oka, National Institute of Advanced Industrial Science and Technology, Japan

We have experimentally clarified the origin of low-frequency noise, which limits the coherence-time in Si quantum bit (qubit), utilizing cryo-CMOS. At cryogenic temperature (2.5 K), significantly enhanced 1/f noise is observed in Si MOSFETs, while it is not seen at room temperature. Interface trap density dependence of noise in Si MOSFETs, changing the surface orientation, revealed that the cryogenic 1/f noise is governed by carrier number fluctuation and we identified that the origin of the 1/f noise is interface trap at cryogenic temperature, for the first time. The present study demonstrates that the experiments using well-investigated MOSFETs can provide new knowledge on Si qubits, which it is hardly possible to investigate using Si qubit as itself.

Hiroshi Oka received the M.S. and Ph.D. degrees from Osaka University, Japan, in 2014 and 2017, respectively. He is currently with the National Institute of Advanced Industrial Science and Technology (AIST), Japan. His research interests include the cryogenic Si electronics for quantum computer hardware, high-mobility channel for advanced CMOS, and optoelectronic integrated circuits.
**CA1.1**

**A 3.0 TFLOPS 0.62V Scalable Processor Core for High Compute Utilization AI Training and Inference**

*Sae Kyu Lee, IBM T. J. Watson Research Center, USA*

A processor core is presented for AI training and inference products. Leading-edge compute efficiency is achieved for robust fp16 training via efficient heterogeneous 2-D systolic array-SIMD compute engines leveraging compact DLFloat16 FPPUs. Architectural flexibility is maintained for very high compute utilization across neural network topologies. A modular dual-corelet architecture with a shared scratchpad and a software-controlled network/memory interface enables scalability to many-core SoCs and large-scale systems. The 14nm AI core achieves fp16 peak performance of 3.0 TFLOPS at 0.62V and 1.4 TFLOPS/W at 0.54V.

*Sae Kyu Lee* received his B.S. degree in electrical engineering from Seoul National University, Seoul, Republic of Korea, the M.S. degree in electrical and computer engineering from The University of Texas at Austin, Austin, TX, USA, and the Ph.D. degree from Harvard University, Cambridge, MA, USA. He was previously with Intel Corporation, Austin, TX, USA, and Advanced Micro Devices, Boxborough, MA, USA, where he worked on mobile microprocessor design. He is currently with IBM T.J. Watson Research Center, Yorktown Heights, NY, USA. His research interests include energy-efficient accelerator design for machine learning applications and VLSI design for efficient on-chip power delivery solutions.

**CA1.2**

**A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS**

*Phil Knag, Intel, USA*

A 10nm digital Binary Neural Network (BNN) chip implements 1b activations and weights for compute density of 418TOPS/mm² and memory density of 414kB/mm². The chip achieves an energy efficiency of 617TOPS/W by leveraging Compute Near Memory (CNM), parallel inner product compute, and Near-Threshold Voltage (NTV) operation. The digital BNN design approaches the energy efficiency of analog in-memory techniques while also ensuring deterministic, scalable, and precise operation.

*Phil C. Knag* received the B.S. degree in computer engineering and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2010, 2012, and 2015, respectively. He is a research scientist at Intel, Circuit Research Lab, Hillsboro, OR, USA. His research interests include machine learning, compute in/near-memory, and energy efficient circuits.

**CA1.3**


*Chieh-Fang Teng, National Taiwan University, Taiwan*

To meet with the stringent requirements of ultra-low latency communication in 5G, this work presents a polar decoder fabricated in TSMC 40nm CMOS featuring: 1) World’s first neural network-assisted decoder chip with 8x improvement of convergence rate. 2) Fully reconfigurable architecture to support multi-code length operations with a 2-to-8x hardware utilization rate. 3) Optimized fixed-point design of processing element (PE) to reduce 73% area and 67% power consumption.

*Chieh-Fang Teng* received his B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2017. He is currently pursuing a Ph.D. degree in the Graduate Institute of Electronics Engineering, National Taiwan University. His research interests are in the areas of Internet-of-things, VLSI architecture for DSP, and machine learning assisted wireless communication systems design.

**CA1.4**

**A 4.45ms Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices**

*Dongseok Im, Korea Advanced Institute of Science and Technology, Republic of Korea*

A 3D point-cloud-based neural network (PNN) processor is proposed for the low-latency hand pose estimation (HPE) system. The processor adopts the heterogeneous core architecture to accelerate both convolution layers (CLs) and sampling-grouping layers (SGFs). The proposed window-based sampling-grouping (WSG) directly samples and groups the 3D points from the streaming depth image to boost up the throughput by ×2.34. Furthermore, the max pooling prediction (MPP) predicts the 64- and 128-to-1 max pooling outputs with ×1.31 throughput enhancement. In addition, the tiled data based MPP (TMPP) performs the MPP with the tiled input data to hide the latency of the MPP. As a result, the processor achieves 4.45 ms latency on the HPE system.

*Dongseok Im* received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2018, and the M.S. degree in electrical engineering at the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2020, where, he is currently pursuing the Ph.D. degree. His current research interests include energy-efficient deep learning SoC design & intelligent vision system.
A 3mm\(^2\) Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception Using Parallel Gibbs Sampling in 16nm

Glenn G. Ko, Harvard University, USA

This paper describes a 16nm programmable accelerator for unsupervised probabilistic machine perception tasks that performs Bayesian inference on probabilistic models mapped onto a 2D Markov Random Field, using MCMC. Exploiting two degrees of parallelism, it performs Gibbs sampling inference at up to 1380x faster with 1965x less energy than an Arm Cortex-A53 on the same SoC, and 1.5x faster with 6.3x less energy than an embedded FPGA in the same technology. At 0.8V, it runs at 450MHz, producing 44.6 MSamples/s at 0.88 nJ/sample.

Glenn Gihyun Ko is a postdoctoral researcher at Harvard University working with Professor Gu-Yeon Wei and Professor David Brooks. He received B.S. and M.S. in electrical and computer engineering, both from the University of Illinois at Urbana-Champaign in 2004 and 2006 respectively. He then joined Samsung Electronics and engaged in research and development of Exynos application processor SoCs. He returned to Illinois and received Ph.D. in electrical and computer engineering in 2017 prior to joining Harvard University in 2018. He has also spent summers at Qualcomm Research and IBM Research on machine learning and architecture research. His current research interests are machine learning, algorithm-hardware co-design and scalable accelerator architectures on the cloud and edge devices.
CA2 Circuits Session - Visual Processing & AI

Session Chairs: Brian Zimmer (Nvidia), Yasuki Tanabe (Toshiba Electronic Devices & Storage)

On-Demand Availability
June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST → June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Related Live Event(s)
Executive Sessions for Interactive Discussions, Paper Elevator-Pitch Summaries and Q&A
EA2 - Sensor Systems - June-15 10:00 PDT / June-15 19:00 CET / June-16 02:00 JST (1 hour)
EB2 - Intelligent Computing - June-15 19:00 PDT / June-16 04:00 CET / June-16 11:00 JST (1 hour)

CA2.1 A 0.05pJ/Pixel 70fps FHD 1Meps Event-Driven Visual Data Processing Unit
Steven Hsu, Intel, USA

An Event-casting accelerator in 10nm CMOS simultaneously casts multiple rays in spatial proximity to exploit voxel data-locality, featuring a near-memory search for voxel address overlaps and opportunistic approximate trilinear interpolation for energy savings. Measurements demonstrate ray-casting of 320x240 depth images with an average latency of 23.2ms/frame, while consuming 32.7pJ energy per ray-step and achieving a maximum energy-efficiency of 115.3 giga ray-steps/W.
A SoC-FPGA-based motion-planning accelerator operating on a graph with >10^6 edges is presented for the first time for dual-arm-robot manipulation systems. The proposed modified A* algorithm with minimized memory access time, is further accelerated by extensive parallel computation and dynamic reconfigurations. The proposed accelerator has been verified by measurement result showing overall motion-planning time of 0.5 seconds, which is only 1/100 of the one by conventional algorithm on embedded CPU, while preserving accuracy.

Takashi Oshima received the B.S., M.S. and Ph.D. degrees in physics from University of Tokyo, Tokyo, Japan in 1996, 1998 and 2001, respectively. He joined the Central Research Laboratory of Hitachi Ltd., Tokyo in 2001, where he is a researcher of analog and digital circuits. From 2005 to 2006, he was a visiting researcher at University of California at Berkeley, USA. Dr. Oshima served as a secretary of the IEEE SSCS Japan Chapter and a Technical Program Committee member of ESSCIRC (IEEE European Solid-State Circuits Conference). He is currently a Technical Program Committee member of ISSCC (IEEE International Solid-State Circuits Conference). He received several awards including 2010 Best Invited Paper Award of IEICE Electronics Society and ISSCC2016 Outstanding Evening Session Award.
Managing Chip Design Complexity in the Domain-Specific SoC Era

Yunsup Lee, SiFive, USA

Chip designers can no longer rely on Moore’s Law and Dennard scaling to make inefficient general-purpose processors faster, cheaper, and lower-power. The industry has instead been forced toward building specialized domain-specific systems on chip (SoCs) to meet next-generation product requirements. Balancing the complexity of these specialized chips with the need to improve time to market is a great challenge of the domain-specific SoC era. We argue that reuse and rapid validation are key to bringing these specialized SoCs to market faster. In this paper, we share our observations of industrial and academic attempts to vault this hurdle, and describe how SiFive, in its early days, quickly designed the Freedom Unleashed 540 SoC with a small team and a tight budget.

Yunsup Lee is SiFive’s Chief Technology Officer and co-founder. Yunsup received his Ph.D. from UC Berkeley, where he co-designed the RISC V ISA and the first RISC-V microprocessors with Andrew Waterman, and led the development of the Hwacha decoupled vector-fetch extension. Yunsup is the chair of the technical steering committee of the RISC-V Foundation. Yunsup also holds an M.S. in Computer Science and Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST).

17.3GCUPS Pruning-Based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing

Xiao Wu, University of Michigan, Sequel, USA

We present the first ASIC accelerator for pair-Hidden-Markov-Model (Pair-HMM) in DNA variant calling, which conventionally requires ~250T FLOPs per sequenced human genome. Using a hardware-algorithm co-design, we opportunistically replace floating point (FP) multiplication with 20b log-domain addition while employing bound checks to maintain (provable) correct results in downstream processing. FP computation is reduced by 43× on real human genome data. Implemented in 40nm CMOS, the 5.67 mm² accelerator demonstrates 17.3G cell updates per second (CUPS) throughput, marking a 6.6× improvement over our baseline ASIC implementation and 355× GCUPS/mm² improvement over a recent FPGA implementation.

Xiao Wu received the B.S. degree in electrical engineering and computer science, both from the University of Michigan, Ann Arbor, MI, U.S.A., and Shanghai Jiao Tong University, Shanghai, China, in 2014. She received the Ph.D. degree in electrical and computer engineering from the University of Michigan, Ann Arbor, in 2019. Her research includes small sensor node design and high-performance hardware accelerator for genome sequencing.

A Probabilistic Self-Annealing Compute Fabric based on 560 Hexagonally Coupled Ring Oscillators for Solving Combinatorial Optimization Problems

Ibrahim Ahmed, University of Minnesota, USA

NP-hard combinatorial optimization problems (COPs) are very expensive to solve with traditional computers. COPs can be mapped to a coupled spin network where the ground state of the system is the solution. We propose a scalable truly coupled CMOS oscillator-based integrated system with self-annealing capabilities to solve COPs in hardware by mimicking spin network. Our simple and scalable latch-based coupling design finds solutions of difficult max-cut problems with 85%-100% accuracy 10⁴-10⁶ times faster than a commercial software running on a GPU.

Ibrahim Ahmed is currently pursuing his Ph.D. in electrical engineering at the University of Minnesota, Twin Cities, Minnesota. He received his B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 2013. His research focuses on designing and optimizing beyond CMOS devices and architectures. He models spintronic logic and memory devices in SPICE for realistic benchmarking. His work involves circuit and architecture optimization for improving performance statistics of novel memory solutions. Ibrahim’s latest work is designing circuits and architectures for the CMOS Ising computer, where he validates the designs by taping out in industry-standard PDKs. His true-coupling based Ising computers aim to solve a class of NP-hard problems that are intractable to solve in a traditional computer.
CA3.4 MANA: A Monolithic Adiabatic INtegration Architecture Microprocessor Using 1.4zJ/op Superconductor Josephson Junction Devices

Christopher Ayala, Yokohama National University, Japan

We present an adiabatic microprocessor based on Josephson junction (JJ) devices manufactured using a Nb/AlOₓ/Nb superconductor IC fabrication process. It is a hybrid of RISC and dataflow architectures operating on 4b data words. We demonstrate register file R/W access, ALU execution, and program branching performed at 100kHz under the cryogenic temperature of 4.2K. We also successfully demonstrated a high-speed chip of the microprocessor execution units up to 2.5GHz. We use a logic primitive called the adiabatic quantum-flux-parametron (AQFP) which has a switching energy of 1.4zJ when driven by a 4-phase 5GHz ac-clock at 4.2K.

Christopher Ayala received the combined B.Eng. and M.Sc. degrees in computer and electrical engineering respectively from Stony Brook University, New York, USA in 2009. He received his Ph.D. in computer engineering in 2012 from Stony Brook University for research in low-power, multi-GHz integer ALUs and data-flow microarchitectures implemented in superconductor logic. He interned at Nvidia where he worked on architectural power optimization techniques for next-generation GPU floating-point datapaths. From 2013 to 2015, he was a Post-Doctoral Fellow at IBM Research - Zurich where he was involved in the research of circuit design and computational systems using novel NEM switches. Since 2015, he has been with the Institute of Advanced Sciences, Yokohama National University, Japan where he is now an associate professor. His research interests include beyond-CMOS computing, rapid single-flux-quantum logic, adiabatic quantum-flux-parametron logic, NEMS-MEMS logic, computer architecture, and electronic design automation. Dr. Ayala is a member of The Japan Society of Applied Physics (JSAP); Institute of Electronics, Information and Communication Engineers of Japan (IEICE); Institute of Electrical and Electronics Engineers (IEEE); Eta Kappa Nu Electrical and Computer Engineering Honor Society; and Tau Beta Pi Engineering Honor Society.

CA3.5 32GHz 6.5mW Gate-Level-Pipelined 4-bit Processor using Superconductor Single-Flux-Quantum Logic

Koki Ishida, Kyushu University, Japan

A Single-Flux-Quantum (SFQ) 4-bit throughput-oriented processor has successfully been demonstrated at up to 32 GHz with the measured power consumption of 6.5 mW. This is the first implementation of the gate-level-pipelined processor, and it achieves 2.5 Tera-Operations Per Watt (TOPS/W) by circuit and architectural optimizations.

Koki Ishida received his B.E. and M.E. degrees from Kyushu University, Japan, in 2016 and 2018 respectively. He is currently a Ph.D. student in the Graduate School of Information Science and Electrical Engineering at Kyushu University. His research interests include the computer architecture of ultra-fast/energy-efficient computing using SFQ logic family.
A 785nW Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring

(EG4)  
Peng Wang, University of Virginia, USA

This paper presents a 785nW multimodal sensor interface IC enabling ozone pollutant sensing and correlated cardiovascular disease (CVD) monitoring based on electrocardiography (ECG) and photoplethysmography (PPG). The interface IC consists of a 165nW voltage-mode ECG channel, a 532nW current-mode PPG channel, a 75.6nW resistive ozone channel, and 12.6nW peripheral circuits, all at 0.6V. A 4MΩ-gain regulated cascode transimpedance amplifier (RGC-TIA) with a hybrid DC offset current cancellation (DCOC) loop reduces the PPG readout power by 37x compared to state-of-the-art PPG sensor interfaces. Fabricated in 65nm CMOS, the proposed IC is tested with a custom digital readout IC. The full system power consumption with an LED is 11.5μW, which is 54x less than prior ozone/CVD joint-monitoring sensor interface systems.

Peng Wang received her B.E. degree from Beihang University, Beijing, China in 2017. She is currently working towards her Ph.D. in electrical engineering at University of Virginia, Charlottesville, VA, USA. Her research interests include ultra-low-power mixed-signal sensor interface design and wearable system design for biomedical applications.

An Artificial Iris ASIC with High Voltage Liquid Crystal Driver, 10nA Light Range Detector and 40nA Blink Detector for LCD Flicker Removal

(EA2)  
Bogdan Raducanu, imec, Belgium

In a functional eye, the iris controls the pupil diameter to regulate the exposure of the retina. While iris deficiencies such as aniridia or leiomymyoma can be mitigated with fixed or adaptive artificial irises [1] and adaptive transparency glasses exist to alleviate this situation, they do not mimic the normal functionality of the natural iris. To address this, a fully encapsulated, self-contained iris embedded in a smart contact lens is proposed.

Bogdan C. Raducanu received the Ph.D. degree in electronics engineering from KU Leuven in 2018 in collaboration with imec, Belgium. He is currently working at imec as researcher in Connected Healthcare Solutions, focusing on designing microelectronic circuits for neural interfaces and wearables. His research interests include analog and mixed-signal circuits for biomedical applications, sensors and IoT.

A Packaged Ingestible Bio-Pill with 15-Pixel Multiplexed Fluorescence Nucleic-Acid Sensor and Bi-Directional Wireless Interface for In-vivo Bio-Molecular Sensing

(EA2)  
Chengjie Zhu, Princeton University, USA

This paper presents the first wireless multiplexed fluorescence-based bio-molecular sensing system in a pill form for GI-track health monitoring application. This application is geared towards quasi-real time analysis of microbiome distribution through nucleic acid detection. A silicon chip integrates both the sensor and the wireless system, including a 124 μW ULP wireless receiver with -59 dBm sensitivity, a dual mode FSK/OOK transmitter, and a fluorescent sensor array with 1.6 attomoles and 100 pM of target DNA detection limit per pixel. The complete package includes a CMOS fluorescent sensor chip with integrated filter, a prototyped UV LED and optical waveguide, functionalized biosip, off-chip power management and Tx/Rx antenna that fits in a standard FDA approved capsule size 000.

Chengjie Zhu graduated from the Georgia Tech Electrical Engineering Department and joined Prof. Kaushik Sengupta's research group in Spring 2017 at Princeton. He was twice awarded the PURA undergraduate research award and had a few publications during his undergraduate years, including TBioCAS, VLSI Tech Cir.

This paper presents a 1024-electrode hybrid voltage/current-clamp neural interface system-on-chip with dynamic incremental-SAR acquisition

(Jun Wang, University of California San Diego, USA

We present a neural interface system-on-chip (NISoC) with 1,024 channels of simultaneous electrical recording and stimulation for high-resolution high-throughput electrophysiology. The 2mm × 2mm NISoC in 65nm CMOS integrates a 32 × 32 array of electrodes vertically coupled to analog front-ends supporting both voltage and current clamping through a programmable interface, ranging over 100 dB in voltage and 120dB in current, with 0.82μW power per channel at 5.96μVrms input-referred voltage noise from DC to 12.5kHz signal bandwidth. This includes on-chip acquisition with a back-end array of 32 dynamic incremental SAR ADCs for 25Msps 11-ENOB acquisition at 2Ulevel FOM.

Jun Wang received the B.S. degree in instrumentation from Jiangsu University, Jiangsu, China, in 2011, and the M.S. degree (with honors) in precision instruments from Tsinghua University, Beijing, China, in 2014. He expects to receive his Ph.D. degree in bioengineering at the University of California, San Diego, CA, USA in 2020. His research interests include neuromorphic neural interfaces chip design, biomedical instrumentation, and bioMEMS. He received the Chiang Chen Overseas Graduate Fellowship in 2014.
Microelectrode arrays (MEAs) allow us to observe electrical activities from neurons at multiple sites. This paper presents a high-density microelectrode array (HD-MEA) for observing neuronal networks at a cellular level, featuring 236,880 electrodes at an 11.72 μm pitch and 33,840 readout channels with a noise level of 5.5 μVrms. The Peltier cooling system is integrated to maintain the temperature of the electrodes at approximately 37 °C. Moreover, electrical signals for the axonal propagation of rat neurons are successfully recorded.

**Demo**

Yuri Kato received the M.E. degree in electronic engineering from Tohoku University, Sendai, Japan, in 2010. He joined Sony Corporation, Japan, in 2010, where he has worked on the development of semiconductor sensing devices.
CB2 Circuits Session - Image Sensor & Imaging Techniques

Session Chairs: Neale Dutton (STMicroelectronics), Tomohiro Takahashi (Sony Semiconductor Solutions)

CB2.1 Invited
A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR
Tuan Thanh Ta, Toshiba, Japan

This paper introduces several key RX techniques to realize a 200m-range and low-cost high-pixel-resolution solid-state LiDAR for autonomous self-driving systems. In-Sensor Scanning 2D-SPAD array can remove the mechanical mirror and improve the pixel-resolution by implying short dead time active-queenching SPADs. For ToF calculating SoC, we adopt the world first dual-data converter (DDC) which consolidates the functions of ADC and TDC into a single circuitry, achieving the acquisition of both high-precision time/voltage data from a single input. Such innovations lead us to 200m-range 300x80-pixel solid-state LiDAR RX under 70klux solar radiation.

CB2.2 Invited
A 36-Channel SPAD-Integrated Scanning LiDAR Sensor with Multi-Event Histogramming TDC and Embedded Interference Filter
Hyeongseok Seo, Sungkyunkwan University, Republic of Korea

This paper presents a 36-channel scanning light detection and ranging (LiDAR) sensor with an on-chip single-photon avalanche diode (SPAD) array. The sensor has a 11b in-situ histogramming time-to-digital converter (hTDC) with a small area of 3000×78µm²/channel based on the mixed-signal accumulator. The sensor also employs an embedded interference (IF) filter for reliable direct time-of-flight (dTOF) measurement even if 32 different LiDARs interfere. The LiDAR system has a beam scanner that consists of dual laser diodes (LDs) for IF elimination and hybrid mirror such that high-resolution image of 2200 × 36 can be acquired with a wide field of view (FOV) of 120° × 8°.

Hyeongseok Seo received the B.S. degree in semiconductor systems engineering from Sungkyunkwan University, Suwon, Korea, in 2017. He is currently pursing the M.S. and Ph.D degrees in electrical engineering at the Sungkyunkwan University. His research interests are analog circuit design and CMOS LiDAR sensors.

CB2.3 Invited
A 3.0µW@5fps QQVGA Self-Controlled Wake-Up Imager with On-Chip Motion Detection, Auto-Exposure and Object Recognition
Arnaud Verdant, CEA-Leti-MINATEC, France

Analyzing image content usually comes at the expense of a power consumption incompatible with battery-powered systems. Aiming at proposing a solution to this problem, this paper presents an imager with full on-chip object recognition, consuming sub-10µW using standard 4T pixels in 90nm imaging CMOS technology, opening the path for both wake-up and high-quality imaging. It combines multi-modality event-of-interest detection with self-controlled capabilities, a key for low-power applications. It embeds a log-domain auto-exposure algorithm to increase on-chip automation. The power consumption figures range from 3.0 to 5.7µW at 5fps for a QQVGA resolution while enabling background subtraction and single-scale object recognition. This typically shows a measured 94% accuracy for a face detection use case.

Arnaud Verdant received the Ph.D. in microelectronics from the Paris Sud University. Since 2008, he has been at CEA-LETI as a Research Engineer. He is involved in industrial research activities related to analog and mixed-signal ASIC design, embedded image processing, and analog to digital conversion. His research focuses on smart image sensors for industrial and medical applications. He is author or co-author of more than 15 international peer-reviewed papers and involved in 23 patents.

CB2.4 Invited
A Low Noise Read-Out IC with Gate Driver for Full Front Display Area Optical Fingerprint Sensors
Yongil Kwon, Samsung Electronics, Republic of Korea

It is presented the first read-out IC (ROIC) for a TFT-based full-screen optical fingerprint (FP) sensor placed under the OLED display. The ROIC supports both the fast-scan mode to acquire 256x256 pixels FP image in anywhere on the display, and the full-scan mode to acquire a full-screen FP image (2,560x1,280 pixels). 2nd order correlated double sampling (CDS) and noise compensation techniques are used for low noise and leakage immunity. A low-cost single-slope ADC (SS-ADC) with enhanced input dynamic range (DR) per channel enables fast FP scans and a large area sensing without excessive die area increase. A breakdown voltage (BV) protection circuit allows the gate driver and IO pad in the ROIC to be driven up to 18Vpp(±9V) using 9V devices. The IC was fabricated in a 90nm CMOS process.

Sensing area, measured SNR, sensing time, and power consumption are 12.8x6.4cm² with 508dpi, 17dB, 208ms, and 56mW at 2.8V, respectively.

Yongil Kwon joined Samsung Electronics, Display Solution Development Team, Korea, in 2016 where he has been engaged in the design and testing of both touch controller and fingerprint sensor ICs. He was also an analog design lead for CMOS RFIC and RF system. His research interests include low-noise circuit and system design, high-frequency analog integrated circuits, continuous-time sigma-delta bandpass ADC, SoC design methodology, and wireless SoC designs.
This paper presents a 4x compressive CMOS imager for always-on operation that achieves an energy efficiency of 51pJ/pixel, while maintaining high image quality of PSNR>32dB and SSIM>0.84. This is enabled by an energy-efficient compressive-sensing (CS) encoder, which replaces a densely populated CS encoding method with a highly sparse pseudo-diagonal one. Since the proposed CS encoder can be implemented with an energy-efficient switched-capacitor matrix multiplier at pixel outputs, data compression is achieved prior to pixel digitization, thereby greatly reducing ADC power, data size, and I/O power. The energy efficiency of the imager is further improved by incorporating it into dynamic single-slope ADCs. A prototype VGA imager consumes only 0.7mW at 45 fps. The corresponding energy per pixel (51pJ/pixel) amounts to a 20x improvement over the previous low-energy benchmark on CS imagers.

Wenda Zhao received the B.S. degree from Peking University, Beijing, China, in 2016, and the M.S. degree in engineering from the University of Texas at Austin, Austin, TX, USA, in 2019, where he is currently pursuing the Ph.D. degree. His current research interests include power-efficient sensor readouts and data converters, as well as ultra-low-power compressive sensing techniques for IoT applications. He received the May-4th Scholarship in 2015 and the Outstanding Undergraduate Thesis Award in 2016, both from Peking University. He also received the Analog Devices Outstanding Student Designer Award in 2018 and the IEEE SSCS Predoctoral Achievement Award (2019-2020).
CB3 Circuits Session - Physical Sensors

Session Chairs: Loic Sibeud (CEA-Leti), Yutaka Hirose (Panasonic)

On-Demand Availability

Executive Sessions for Interactive Discussions, Paper Elevator-Pitch Summaries and Q&A

Related Live Event(s)

CB3.1

**A 50.7dB-DR Finger-Resistance Extractable Multi-Touch Sensor IC Achieving Finger-Classification Accuracy of 97.7% on 6.7-inch Capacitive Touch Screen Panel**

**Matheus Pimenta**, Columbia University, USA

This paper presents a 0.85 mm² user-recognizable 2D touch readout IC embedding finger resistance extraction (FRE) on a capacitive touch screen panel (TSP). The resonance-driven FRE technique and the clamped zoom-in integrator are exploited to achieve a wide dynamic range (DR). To readout the FRE and touch sensing (TS) signals, the switched-capacitor current-controlled oscillator (SC-CCO) based 14-bit ADC was also designed, which benefits low noise and compact size. The prototype chip fabricated in 0.18-µm CMOS offers the measured 37.5dB-SNR and 50.7dB-DR in TS and FRE modes, respectively, in a 6.7-inch TSP. By applying a support vector machine (SVM) learning to the FRE data, five different user-fingers were successfully classified with 97.7% accuracy after 500 learning-cycles, thereby bringing the reliable user-differentiation to multi-user collaborative touch interfaces.

**Tae-Gyun Song** received the B.S. degree in display engineering in 2018 and the M.S. degree in microelectronics and electrical engineering in 2020 from Dankook University, Korea. Since March 2019, he has been with the School of Electrical Engineering at KAIST, Daejeon, Korea, as a Visiting Researcher. His research interests are in the field of CMOS readout circuits.

CB3.2

**A Pressure Sensing System with ±0.75mmHg (3σ) Inaccuracy for Battery-Powered Low Power IoT Applications**

**Seok Hyeon Jeong**, University of Michigan, USA

This work presents an energy efficient piezoresistive pressure sensing system for low power IoT applications. The sensor adopts duty-cycling and sub-ranging to achieve high energy efficiency and accuracy. Fabricated in 180nm CMOS, the test chip with pressure transducer achieves state-of-art energy efficiency of 6.1nJ/mmHg² with ±0.75mmHg 3σ inaccuracy. The sensor is integrated into a wireless sensor node to demonstrate its operation at a system level.

**Seok Hyeon Jeong** received the B.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2011, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2017. He is currently with the University of Michigan and CubeWorks Inc., Ann Arbor, where he is involved in researching and developing interface circuits for ultra-low-power sensor nodes. His research interests include ultra-low-power sensor nodes and the design of millimeter-scale computing systems.

CB3.3

**A 200µW Eddy Current Displacement Sensor with 6.7nm rms Resolution**

**Matheus Pimenta**, Cypress Semiconductor, Ireland

This paper describes a low-power eddy current displacement sensor intended for safety-critical touch applications. A sensing inductor is incorporated into a digital PLL to efficiently digitize the displacement of a flexible metal foil. At a stand-off distance of 500µm, the sensor achieves 6.7nm resolution in a 3kHz bandwidth over a 43µm range. It consumes 200µW from a 1.8V supply, which represents a 35x improvement on the state of the art.

**Matheus Pimenta** received the B.Sc. degree in electrical engineering from the University of Brasilia, Brasilia, Brazil, in 2015, and the M.Sc. degree from the Electronic Instrumentation Laboratory, Delft University of Technology (Tu Delft), Delft, The Netherlands in 2019. Since 2020, he has been with Cypress Semiconductor, Cork, where he is working with low power analog building blocks for capacitive and inductive sensing. His current research interests include low-power sensor interface ICs and energy-efficient data converters.

CB3.4

**A 0.72nW, 1Sample/s Fully Integrated pH Sensor with 65.8LSB/pH Sensitivity**

**Yihan Zhang**, Columbia University, USA

This paper presents a 0.85 mm² fully integrated pH sensor IC utilizing an ion-sensitive field effect transistor (ISFET) and reference field effect transistor (REFET) pair in which the native foundry passivation layer is used as an ion-sensitive layer. The pH sensor has 10 bit resolution with 65.8 LSB/pH sensitivity, while consuming only 0.72 nW at 1 sample/s, improving an overall figure of merit (FoM) that accounts for power, sampling frequency, and sensitivity by > 4000×.

**Yihan Zhang** received the B.E. degree in microelectronics from Tsinghua University, Beijing, China, 2013, and the M.S degree in mechanical engineering from Columbia University, New York, USA, 2014. He joined the Bioelectricronic Systems Lab in Electrical Engineering at Columbia University in 2015 as a Ph.D. student. His research interests include circuits and systems for miniaturized biomedical implants, ultrasound-based power and data links, energy harvesting circuits, and energy-efficient computing.
An 8-Element Frequency-Selective Acoustic Beamformer and Bitstream Feature Extractor with 60 Mel-Frequency Energy Features Enabling 95% Speech Recognition Accuracy

Seungjong Lee, University of Michigan, USA

A synergistic approach to beamforming and feature extraction, reduces processing complexity and die area, and delivers the high SNR required for reliable speech recognition. The 1.1mm$^2$ IC combines frequency-selective bitstream beamforming, bitstream Mel frequency-band feature extraction, and an array of continuous-time sigma-delta modulators (SDMs) without area/power-intensive decimation. When coupled with a DNN, the prototype achieves 95.3% accuracy in recognizing spoken words from the Tensorflow dataset.

Seungjong Lee received the B.S. and M.S. degrees in electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2011 and 2013, respectively. He is currently working toward the Ph.D degree at the University of Michigan, Ann Arbor, MI, USA. From 2013 to 2016, he was an assistant research engineer with Silicon Works, Daejeon, South Korea, working on mixed-signal circuits. His current research interests include data converter and power management ICs.
CB4.1 A −105dB THD 88dB-SNR VCO-based Sensor front-end Enabled by Background- Calibrated Differential Pulse Code Modulation

Jiannan Huang, University of California San Diego, USA

This paper presents a VCO-based sensor front-end utilizing differential pulse-code modulation (DPCM) to substantially reduce the amplitude of the input signal to the VCO quantizer so that high linearity is achieved. Together with a background digital gain calibration and DEM, the techniques enable a high dynamic range (DR) using only 1st order noise-shaping and 32x oversampling. Fabricated in 65nm, the AFE consumes 3.2μW and achieves 1.18μVrms input-referred noise in 500Hz BW. It also achieves an SNDR/DR/THD of 88/94/-105dB respectively with a NEF of 4 and Schreier FoM of 170dB.

Jiannan Huang received the B.S degrees in electrical engineering from both the University of Michigan, Ann Arbor MI, with outstanding achievement and Shanghai Jiao Tong University, Shanghai China in 2016. In 2018, he received M.S. degree in electrical engineering from the University of California, San Diego (UCSD). He is now pursuing the Ph.D. degree in the EEMS group at UCSD. He has held internships with Analog Devices, MaXentric Technologies, and Movellus Circuits where he worked on high performance, low power mixed-signal circuits. His research interest includes analog/mixed-signal integrated circuits with a particular interest in developing low power Analog Front-ends (AFE) for biological applications.

CB4.2 A 4.3fJ/conversion-step 6440μm² All-Dynamic Capacitance-to-Digital Converter with Energy-Efficient Charge Reuse

Haoming Xin, Eindhoven University of Technology, Netherlands

An ultra-low power all-dynamic capacitance-to-digital converter (CDC) that exploits a novel charge reuse technique is proposed. Instead of resetting the large sensing capacitance for each measurement, its charge is maintained and reused from measurement to measurement. Passive charge sharing between front-end and ADC is used as well as an all-dynamic architecture to enable power-efficient performance and scalability versus measurement rate. Power gating techniques are employed to reduce the minimum power consumption. As a result, a FoM as low as 4.3fJ/conv-step is achieved, which is >3x better than the state-of-the-art. It supports an inherent scaling of power vs. speed with a minimum power of only 44pW and a compact chip area of 6440μm².

Haoming Xin was born in November 1991, in Henan, China. In 2013, he received the B.Sc. degree from Xi’an Jiaotong University, China. Later he continued to study electrical engineering at the Eindhoven University of Technology (TU/e), The Netherlands, where he received the M.Sc. degree in 2015. From October 2015, he started pursuing the Ph.D. degree with the Integrated Circuits (IC) Group at TU/e, with a main focus on the design of low-power versatile sensor interfaces. Since November 2019, he has been working as a post-doctoral researcher in the IC group at TU/e.

CB4.3 A 0.5V, 6.2μW, 0.059mm² Sinusoidal Current Generator IC with 0.088% THD for Bio-Impedance Sensing

Kwantae Kim, Korea Advanced Institute of Science and Technology, Republic of Korea

This paper presents the first sub-10μW, sub-0.1% THD sinusoidal current generator (CG) IC that is capable of 20kHz output for the bio-impedance (Bio-Z) sensing applications. To benefit from the ultra-low-power nature of near-threshold operation, a 9b pseudo-sine LUT is 3b ΔΣ modulated in the digital domain, thus linearity burden of the DAC is avoided and only a 1.29μW of logic power is consumed, from a 0.5V supply and a 2.56MHz clock frequency. A half-period (HP) reset is introduced in the capacitive DAC, leading to around 30dB reduction of in-band noise by avoiding the sampling of data-dependent glitches and attenuating the kT/C noise and the non-idealities of reset switches (SW).

Kwantae Kim received the B.S and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree. He is currently also with the Institute of Neuroinformatics, University of Zurich and ETH Zurich, Zurich, Switzerland, as a visiting student. His research interests include design of low-power bio-impedance sensors and low-power neuromorphic audio sensors.

CB4.4 A Portable NMR System with 50kHz IF, 10μs Dead Time, and Frequency Tracking

Sungjin Hong, University of Texas at Austin, USA

This paper presents a portable nuclear magnetic resonance (NMR) system with significantly enhanced capabilities. Unlike prior works that use the same clock frequency for TX excitation and RX LO, this work uses two separate frequencies with a 50-kHz intermediate frequency (IF) that break the tradeoff between cross-resonance excitation and 1/f-noise & offset suppression. It also proposes an accurate but low-cost method to ensure two clocks' phase coherence, which is necessary for time-domain averaging. Moreover, this work addresses the critical limitation of long RX dead time in prior works. By dynamically adjusting high-pass corner frequencies of IF filters and amplifiers, it shortens the dead time by 100 times to only 10us. Additionally, an automatic frequency tracking technique is devised to address the magnetic field drift. This work also reports the highest integration level achieved for an NMR transceiver, with on-chip ADC and DLL. Various measurements have been performed for system validation.

Sungjin Hong received the B.S degree in electrical engineering and management science from Korea Advanced Institute of Science and Technology in 2012. He is currently pursuing the Ph.D. degree at the University of Texas at Austin. His research interests are analog, mixed-signal, and RF circuit design for NMR spectroscopy and MR imaging. He held internship positions in Schlumberger-Doll Research in 2014 and Intel from 2018 to 2019.
CC1 Circuits Session - Circuits for Security and Safety

Session Chairs: Rob Aitken (Arm), Mototsugu Hamada (University of Tokyo)

On-Demand Availability

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CC1.1 A Performance-Flexible Energy-Optimized Automotive-Grade Cortex-R4F SoC through combined AVS/ABB/Bias-in-Memory-Array Closed-Loop Regulation in 28nm FD-SOI

Ricardo Gomez Gomez, STMicroelectronics, France

We propose an automotive-grade ARM® Cortex®-R4F core SoC that optimizes its energy across 11X frequency-wide Operational Performance Points (OPPs) by combining Adaptive Voltage Scaling (AVS), Adaptive Body-Biasing (ABB) and Bias-in-Memory-Array (BIMA); with a 3mV/bit Tunable Replica Circuit (TRC) for safety, embedded power regulation and compensation. The reported techniques respectively improve by, 21X performance, 120mV lower $V_{MIN}$, and 8X lifetime, the Low-Power, Mid-, and High-Performance OPPs. Results have been measured at extreme conditions, covering SS/TT/FF process, 0.5/1.2V, -40/150°C, and EOL aging.

Ricardo Gomez Gomez received the B.Sc in electrical engineering from the Technical University of Madrid, Spain, in 2014; and the M.Sc in system-on-chip design from Lund University, Sweden, in 2016. He is currently pursuing his Ph.D. in microelectronics as a research engineer at STMicroelectronics in Crolles, France. His main research interests are energy-efficient CMOS design with a focus on FD-SOI technology, PVTA monitoring, and automotive safety.

CC1.2 A SCA-Resistant AES Engine in 14nm CMOS with Time/Frequency-Domain Leakage Suppression Using Non-linear Digital LDO Cascaded with Arithmetic Countermeasures

Raghavan Kumar, Intel, USA

An AES engine with uniform side-channel-attack (SCA) resistance across time/frequency domains using a high-bandwidth non-linear digital low-dropout (NL-DLDO) regulator in conjunction with AES arithmetic countermeasures is fabricated in 14nm CMOS. Randomized regulator loop parameters and cascading LDO and arithmetic transformations provide >250K× increase in frequency/time-domain MTD, with no CPA attack detected on current/electromagnetic (EM) traces measured from 1 billion encryptions.

Raghavan Kumar received the M.S. and Ph.D. degrees in electrical engineering from the University of Massachusetts in 2012 and 2015 respectively. He is currently a research scientist at Circuit Research Labs, Intel Hillsboro, OR. His research interests include hardware security, machine learning, and high-performance and low-power datapath circuits. He has authored over 20 technical articles, 2 book chapters, and holds 5 U.S. issued patents with more than 50 patents pending.

CC1.3 A 0.26% BER, $10^{28}$ Challenge-Response Machine-Learning Resistant Strong-PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection

Vikram Suresh, Intel, USA

Strong Physically Unclonable Functions (PUF) are promising alternatives to expensive cryptographic functions for low-cost IoT device authentication. In this work, a $10^{28}$ challenge-response strong-PUF circuit is fabricated in 14nm CMOS, demonstrating modeling attack resistance across 6-million training samples. Two-stage non-linear cascaded PUF array organization with adversarial challenge selection increases modeling complexity by 4×, limiting ML attack accuracy to ~50%. Configurable cross-coupled inverter-based entropy source with stability-aware challenge pruning enables 9.8× higher array density, with linearly-scaling enrollment data and a worst-case bit-error-rate of 0.26% measured across 650-850mV, 0-100°C operation.

Vikram Suresh is a Research Scientist in the Circuit Research Lab, Intel Corporation. He received his M.S. and Ph.D. in electrical and computer engineering, both from University of Massachusetts, Amherst in 2011 and 2014 respectively. His research interests include high-performance and energy-efficient micro-architecture and circuit design for data encryption and authentication; design of cryptographic primitives for random number and key generation; and high-performance data compression. He has 22 issued patents and has co-authored 42 publications in peer reviewed conference and journals.

CC1.4 A 435MHz, 2.5Mbps/W Side-Channel-Attack Resistant Crypto-Processor for Secure RSA-4K Public-Key Encryption in 14nm CMOS

Raghavan Kumar, Intel, USA

A 0.072mm$^2$ SCA-Resistant RSA-4K crypto-processor fabricated in 14nm CMOS achieves peak encryption throughput of 0.08Mbps at 750mV, 25°C. Exponent magnitude timing randomization with dynamic RF addressing provide 711× lower means-separation in current/EM trace magnitudes, reducing attacker’s accuracy to an ineffective random guess classification while limiting area/performance overhead to 3%.

Raghavan Kumar received the M.S. and Ph.D. degrees in electrical engineering from the University of Massachusetts in 2012 and 2015 respectively. He is currently a research scientist at Circuit Research Labs, Intel Hillsboro, OR. His research interests include hardware security, machine learning, and high-performance and low-power datapath circuits. He has authored over 20 technical articles, 2 book chapters, and holds 5 U.S. issued patents with more than 50 patents pending.
CC2 Circuits Session - Adaptive Clocking and Power Delivery

Session Chairs: Paul Whatmough (Arm), Makoto Takamiya (University of Tokyo)

CC2.1 A Proactive Voltage-Droop-Mitigation System in a 7nm Hexagon™ Processor
(Vijay Kiran Kalyanam, Qualcomm Technologies, USA)

A proactive clock-gating system (PCGS) in a 7nm Qualcomm® Hexagon™ digital signal processor (DSP) predicts supply voltage (V_{dd}) droops based on microarchitectural events and a power-delivery-network (PDN) model and adapts clock frequency (F_{clk}) to reduce the V_{dd} droop. Silicon measurements demonstrate 10% higher F_{clk} or 5% lower V_{dd}.

Vijay Kiran Kalyanam is a Senior Staff Engineer at Qualcomm, Austin with 16 years of experience in processor design. He works on processor core micro-architecture, power and voltage mitigation of Hexagon™ processors. He is a Ph.D. candidate at the University of Texas at Austin.

CC2.2 An Autonomous Reconfigurable Power Delivery Network (RPDN) for Many-Core SoCs Featuring Dynamic Current Steering
(Khondker Ahmed, Intel, USA)

A new and improved Unified Clock and Power (UniCaP) architecture relies on dual-path feedback to further reduce supply voltage (V_{dd}) margins in an ARM Cortex M0 processor while minimizing both peak cycle loss (ΔΦ_{peak}) and cycle-loss recovery time (T_{recovery}) associated with adaptive clocking. Measurements on a 65nm test chip demonstrate 91–99% V_{dd} margin reduction and 36X T_{recovery} improvement over previous work. We also report measurements that quantify the impact of clock distribution delay τ_{dist} and V_{dd} sensitivity on V_{dd} margin reduction.

Khondker Ahmed is a Professor and leads the Integrated Circuits Embedded Systems area, as well as the Green IC group at the National University of Singapore. Previously, he held visiting positions at the University of California Berkeley (BWRC), University of Michigan Ann Arbor, Intel Labs, EPFL. He is author of 300 publications and four books, focusing on ultra-low power integrated system design, widely energy-scalable circuits, and hardware security, among the others. Currently, he is the Editor-in-Chief of IEEE Transactions on VLSI Systems, and Distinguished Lecturer of the IEEE Solid-State Circuits Society. He was also the Deputy Editor-in-Chief of IEEE JETCAS, Guest Editor of several IEEE journal special issues, Program Chair of numerous IEEE conferences. Prof. Alioto is an IEEE Fellow.

CC2.3 Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting
(Massimo Alioto, National University of Singapore, Singapore)

A sensor node with system power tuning is presented for 5-order-of-magnitude adaptation to harvested power. Coordinated tuning of unified voltage/capacitive/light sensor interface, MCU and direct MPPT with no intermediate power conversion scales system power to 3.1nW at 0.3V. Operation at 1lux (moonlight) with 4.1×4.1mm² light harvester is shown.

Massimo Alioto is a Professor and leads the Integrated Circuits Embedded Systems area, as well as the Green IC group at the National University of Singapore. Previously, he held visiting positions at the University of California Berkeley (BWRC), University of Michigan Ann Arbor, Intel Labs, EPFL. He is author of 300 publications and four books, focusing on ultra-low power integrated system design, widely energy-scalable circuits, and hardware security, among the others. Currently, he is the Editor-in-Chief of IEEE Transactions on VLSI Systems, and Distinguished Lecturer of the IEEE Solid-State Circuits Society. He was also the Deputy Editor-in-Chief of IEEE JETCAS, Guest Editor of several IEEE journal special issues, Program Chair of numerous IEEE conferences. Prof. Alioto is an IEEE Fellow.

CC2.4 UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in Designs with Large Clock Distribution Delays in 65nm CMOS
(Xun Sun, University of Washington, USA)

A new and improved Unified Clock and Power (UniCaP) architecture relies on dual-path feedback to further reduce supply-voltage (V_{dd}) margins in an ARM Cortex M0 processor while minimizing both peak cycle loss (ΔΦ_{peak}) and cycle-loss recovery time (T_{recovery}) associated with adaptive clocking. Measurements on a 65nm test chip demonstrate 91–99% V_{dd} margin reduction and 36X T_{recovery} improvement over previous work. We also report measurements that quantify the impact of clock distribution delay τ_{dist} and V_{dd} sensitivity on V_{dd} margin reduction.

Xun Sun received the B.S. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA and from Shanghai Jiao Tong University, Shanghai, China in 2016. Currently, she is pursuing the Ph.D. degree in electrical engineering at the University of Washington, where she is a member of the Processing Systems (PSy) Lab. Her research interests include integrated power converters, low-power mixed-signal circuits and the application of control ideas to power-management problems.
Low-clock-power digital standard cell IPs in 10nm CMOS, featuring low-power shared-clock (LPSC) flip-flops (FFs), LPSC back-to-back (B2B) FFs, and pass-gate (PG) integrated clock gates (ICGs), achieve up to 14%, 45%, and 14% measured clock energy improvements, respectively, by reducing the number of clocked devices over state-of-the-art conventional transmission-gate (TG) FF and AND ICG circuits. The LPSC FF achieves a mean worst-case black-hole-time (BHT) improvement of 17ps, while the PG ICG achieves a mean enable/disable setup time improvement of 16ps/15ps, compared to conventional circuits measured at 650mV, 25°C. Power analysis of a graphics processor block with these optimized IPs results in an overall 6% clock power reduction without frequency impact.

Steven Hsu received the B.S., M.S., and Ph.D. degrees in computer engineering from Oregon State University, Corvallis, OR, in 1999, 2001, and 2006, respectively. Since 2000, he has been with Intel Corporation's Circuits Research Lab, Hillsboro, Oregon. His research interests include design-technology co-optimization, PPA optimization utilizing improved standard cells/physical design, low-voltage/variation-tolerant circuit design, and special-purpose hardware accelerators. Steven has authored over 52 conference and journal papers, holds 46 pending and issued patents. He received the ESSCIRC Best Paper and ISSCC Distinguished Technical Paper in 2012, and was recognized as a top IEEE ISSCC paper contributor in 2013.
CD1 Circuits Session - High-Speed Data Converters

Session Chairs: Stacy Ho (MediaTek), Tomohiro Nezuka (MIRISE Technologies)

On-Demand Availability
June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Related Live Event(s)
EC2 - Analog Building Blocks - June-16 09:00 PDT / June-16 18:00 CET / June-17 01:00 JST (1 hour)
EC3 - Adaptive Systems - June-16 10:00 PDT / June-16 19:00 CET / June-17 02:00 JST (1 hour)
EF2 - Advances in Clocking and Data Converters - June-17 19:00 PDT / June-18 04:00 CET / June-18 11:00 JST (1 hour)

CD1.1 A 1MS/s to 1GS/s Ringamp-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm

Benjamin Hershberg, imec, Belgium

An 11b single-channel ADC with constant 14 fJ/c-step FoM energy efficiency from 1MS/s to 1GS/s introduces a fully-dynamic discrete-time reference regulation solution that consumes only 8% of total system power. A small, low power background monitoring circuit in each pipeline stage generates time-domain waveforms of amplifier settling behavior. Performance at 1GS/s with a Nyquist input is 59.5dB SNDR, 75.9dB SFDR, and consumes 10.9mW.

Benjamin Hershberg earned his Ph.D. from Oregon State University in 2012 for work on scalable, low-power switched-capacitor amplification solutions, including Ring Amplification and Split-CLS. Since 2013, he has been at imec in Leuven, Belgium researching a variety of topics encompassing the entire receiver chain from RF frontends to ADCs.

CD1.2 A 10-bit 100MS/s SAR ADC with Always-on Reference Ripple Cancellation

Xiyuan Tang, University of Texas at Austin, USA

This paper presents an always-on reference ripple cancellation technique that actively cancels the reference settling error throughout the entire SAR conversion process, thus significantly relaxing reference settling requirement. Equipped with the proposed technique, a 100-MS/s prototype SAR ADC only requires a 0.5-pF decoupling capacitor and an on-chip low-power reference buffer that consumes 60% less power compared to state-of-the-art designs with similar performance.

Fabricated in 40nm CMOS, it achieves an SNDR of 56.3dB at Nyquist rate while consuming 1.4mW, including the reference buffer.

Xiyuan Tang received the B.Sc. degree (Hons.) from the School of Microelectronics, Shanghai Jiao Tong University, Shanghai, China, in 2012, and the M.S. and Ph.D. degrees in electrical engineering from the University of Texas at Austin, TX, USA, in 2014 and 2019 respectively, where he is currently a post-doctoral researcher. He was a Design Engineer with Silicon Laboratories, Austin, from 2014 to 2017, where he was involved in receiver design. His research interests include digitally-assisted data converters, low-power mixed-signal circuits, and analog data processing.

CD1.3 An 8b 1GS/s 2.55mW SAR-Flash ADC with Complementary Dynamic Amplifiers

Dong-Ryeol Oh, Korea Advanced Institute of Science and Technology, Republic of Korea

An 8b SAR-Flash ADC is proposed, where four reset-power-free complementary dynamic amplifiers (CDAs) are first engaged to a 4b loop-unrolled (LU) SAR conversion and then reutilized for a 4.5b fine interpolating-flash conversion. The hardware-reusing flash ADC not only saves power consumption and area but also reduces the number of conversion cycles. A prototype 1GS/s ADC in 28nm CMOS achieves 45.5dB SNDR at a Nyquist input with 2.55mW power consumption, leading to a FoM of 16.6 fJ/c-s.

Dong-Ryeol Oh received the B.S. degree in electronic engineering from Soongsil University, Seoul, South Korea in 2013. He is currently working toward the unified master’s and doctorate course in electrical engineering at KAIST, Daejeon, South Korea. His research interests include high-speed, low-power data converter design, and mixed-signal circuits design.

CD1.4 A 177mW 10GS/s NRZ DAC with Switching-Glitch Compensation Achieving > 64dBc SFDR and < -77dBc IM3

Hung-Yi Huang, National Cheng Kung University, Taiwan

This work presents a 14-bit 10GS/s NRZ DAC in 28nm CMOS. Using the proposed switching-glitch compensation to reduce both the switching-glitch effect and code-dependent supply bouncing, this work achieves > 64dBc SFDR and < -77dBc IM3 over the entire Nyquist band at 10GS/s. Compared with other state-of-the-art CMOS Nyquist NRZ DACs with resolution ≥ 10 bits and f_s ≥ 6 GHz, this work has the smallest area of 0.1 mm², the lowest power consumption of 177mW, and the best FoM performance.

Hung-Yi Huang was born in Tainan, Taiwan, in 1987. He received a B.S. degree in electrical engineering with highest honors from National Cheng Kung University, Tainan, Taiwan, in 2010. He is currently working toward a Ph.D. degree, for which his research interests include Nyquist and oversampling ADCs and DACs.

CD1.5 A Compact 14GS/s 8-bit Switched-Capacitor DAC in 16nm FinFET CMOS

Pietro Caragiulo, Stanford University, USA

This paper presents a compact DAC for digital-intensive transmitter architectures. To minimize area and to leverage the strengths of FinFET CMOS, the implementation departs from the traditional current steering approach and consists mainly of inverters and sub-femtofarad switched capacitors. The 14 GS/s 8-bit design occupies only 0.011 mm² and supports up to 0.52 Vpp signal swing across its differential 100 Ω load. It achieves IM3 < 45.3 dBc across the first Nyquist zone while consuming 50 mW from a single 0.8 V supply.

Pietro Caragiulo is currently a Ph.D. student in electrical engineering at Stanford University in the Murmann’s Mixed-Signal Lab. His current research focus is on pushing the performance of high-speed digital-to-analog converters.
CD2 Circuits Session - Data Converter Techniques

Session Chairs: Ewout Martens (imec), Mitsuya Fukazawa (Renesas Electronics)

On-Demand Availability

June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

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CD2.1

A 440μW, 109.8dB DR, 106.5dB SNDR Discrete-Time Zoom ADC with a 20kHz BW

Efraïm Eland, Delft University of Technology, Netherlands

This paper presents a discrete-time (DT) zoom ADC for audio applications. A 2b quantizer in combination with a low power “fuzz” suppression technique, results in a significant improvement in linearity and energy-efficiency over previous designs. The ADC occupies 0.27mm² in 0.16μm CMOS and consumes 440μW from a 1.8V supply. In a 20kHz BW, it achieves 109.8dB DR and 106.5dB SNDR, resulting in a state-of-the-art Schreier FoM of 186.4dB.

Efraïm Eland was born in Vlissingen, The Netherlands in 1992. He received his B.Sc. degree in electrical engineering from Delft University of Technology in 2017. In May 2017, he started pursuing his M.Sc. degree in electrical engineering, specialised in microelectronics. In September 2018, he started his internship/thesis at NXP Semiconductors, after which he graduated in October 2019 with a master thesis work on energy-efficient zoom ADCs for audio applications. Efraïm is currently pursuing the Ph.D. degree at the Electronic Instrumentation Laboratory, working on energy-efficient, high-speed data converters in collaboration with NXP Semiconductors.

CD2.2

A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved Second-Order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm

Dongyang Jiang, University of Macau, China

This paper presents a 4X Time-Interleaved (TI) 2nd-order discrete-time (DT) ΔΣ Modulator (DSM) using digital feedforward extrapolation. Three feedforward paths digitize one channel information first and then extrapolate the other channels fully in the digital domain. Hence, this DSM only needs two op-amps in one channel to realize four interleaving paths, thus reducing analog hardware overheads. With the sampling clock @ 520MHz, this 28nm CMOS prototype achieves an equivalent output sampling rate of 2.08GS/s, 208x OSR, 86.1dB SNDR, and 98dB SFDR over a 5MHz BW, while the power consumption is 23.1mW. It results in an FOMo of 169.5dB.

Dongyang Jiang received the B.Sc. degree in electrical and electronics engineering from the University of Macau, Macau, China, in 2014, where he is currently pursuing the Ph.D. degree in electronic and computer engineering with the State Key Laboratory of Analog and Mixed-Signal VLSI. His current research interests include analog circuit techniques, time-interleaving circuits, and delta-sigma converters.

CD2.3

A 10.4mW 50MHz-BW 80dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp

Kai Xing, University of Macau, China

This paper presents a wideband and energy-efficient single-opamp 3rd order CTSDM enabled by an ELD-SAB-Merged integrator and a 3-stage opamp. We utilize only a single DAC and opamp to accomplish the ELD compensation in the SAB structure. While featuring a PSQ technique and a 1st order NS-SAR, the 28nm prototype achieves a 74.4dB SNDR in a 50MHz BW and consumes 10.4mW with 171.2dB FoMs.

Kai Xing received the B.Sc. degree in integrated circuit design and integrated system from the University of Electronic Science and Technology of China, Chengdu, China, in 2017. He is currently pursuing the Ph.D. degree at the University of Macau, Macau, China. His research interests include oversampling ADC and mixed-signal circuits. Currently, his research mainly focuses on the high speed continuous-time sigma delta modulators.

CD2.4

A 1GS/s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9dB FoMs

Yifan Lyu, MICAS-Katholieke Universiteit Leuven, Belgium

This paper presents a reconfigurable BW 2nd-order noise-shaping (NS) hybrid voltage-time ADC based on the two-step ADC structure. Composed by a SAR ADC in the 1st stage and a time-based-converter (TBC) in the 2nd stage, with a reconfigurable passive filter, it realizes a 2nd-order NS while simultaneously maintaining a simple and high-speed operation. Due to the delay introduced by the inter-stage residue amplifier (RA), one NS order is inherently provided by the pipelined architecture. Fabricated in 28 nm CMOS, the prototype chip operates at 1 GS/s while consuming 2.3 mW at 1 V. At an OSR of 4, the SNDR is 63.58 dB leading to a 170.9dB FoMs. Thanks to the reconfigurable filter, the ADC is able to achieve 163.5 dB and 171.6 dB FoMs at OSR of 2 and 6, respectively.

Yifan Lyu obtained the B.Eng. degree in opto-electrical engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2014, and the M.Sc. degree in electrical engineering from KU Leuven, Belgium, in 2016, where he is currently pursuing the Ph.D. degree in electrical engineering at the Department of Electrical Engineering (ESAT-MICAS). His current research interests include mixed-signal circuits and high-speed A/D converters.
This paper presents a SAR ADC with reduced front-end sampling kT/C noise. This is achieved by using an active sampling circuit with a specially designed 2-stage amplifier that decouples the tight relationship between the sampling noise power spectral density (PSD) and BW. A 12-bit 12-MS/s prototype ADC in 40nm CMOS achieves the sampling noise power reduction by 3.5 times. It permits the use of a small sampling capacitor of only 132 fF. This relaxes the requirement on the ADC input driver and reference buffer, which can lead to significant savings in power, area, and complexity on the system level.

Zhelu Li received the B.S. degree from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2014. He is now a Ph.D. candidate at the Institute of VLSI Design, Zhejiang University. He was a visiting Ph.D. student with the Department of Electrical and Computer Engineering, the University of Texas at Austin, Austin, TX, USA, from 2018 to 2019. His research interests include sensor readout circuits and data converters.
Embedded PLL Phase Noise Measurement Based on a PFD/CP MASH 1-1-1 ΔΣ Time-to-Digital Converter in 7nm CMOS

Mao-Hsuan Chou, TSMC, Taiwan

We propose an embedded PLL phase noise measurement macro for cost-effective SoC test based on a phase-frequency detector/charge pump (PFD/CP) MASH 1-1-1 ΔΣ time-to-digital converter (TDC). The decimated TDC output stream is post-processed to extract the phase jitter and noise spectrum. Measuring low jitter requires a short and precise reference delay which we generate with a charge-based pseudo-DLL that locks to the reference delay itself. Using a 14GHz LC-PLL built in 7nm CMOS as a demonstration vehicle, this macro measures 2.68ps rms jitter which closely matches 2.89ps measured by a phase noise analyzer. The built-in self-test (BIST) macro consumes 12.2mW on a 1.2V supply, occupying only 0.066mm² which is only one-third of the PLL area.

CF1.2
A Fast Locking 5.8−7.2 GHz Fractional-N Synthesizer with Sub-2µs Settling Time in 22nm FDSOI

Jeffrey Prinzie, Katholieke Universiteit Leuven, Belgium

This paper presents a fast settling all-digital fractional-N synthesizer that employs efficient frequency tuning word estimation with type-I and type-II loop settling. It is combined with a DCO with a highly linear coarse tuning bank allowing wide-band closed-loop operation. Linear frequency hopping prediction is used, followed by a series of type-I recovery phases to compensate for drifts and digital zero-phase resets to reduce phase transients due to type-I settling. The DCO gain is equalized by exploiting routing inductance and employs a hybrid binary-thermometric segmentation in a 5.8-7.2 GHz range. The circuit was processed in a 22 nm FDSOI technology and achieves a settling time below 2 µs in a 200 MHz hopping range. The synthesizer has an integrated phase noise of 115 fs with -108 dBc/Hz in band phase noise and 31 mW power consumption resulting in a -243.9 dB FOM.

Jeffrey Prinzie received his M.Sc. and Ph.D. degrees from the KU Leuven association in 2013 and 2017 respectively. During his Ph.D., he worked in the field of radiation tolerant integrated circuits at the Department of Electrical Engineering (ESAT) of KU Leuven. His main interest is in the hardening of time-based mixed-signal circuits, especially PLLs and TDCs, and radiation sensors. During his Ph.D., he was part of the CERN micro-electronics research group. In 2017, he continued his post-doctoral research. From 2018 to 2019, he worked with MediaTek United Kingdom as a visiting researcher on ultra-fast locking all-digital synthesizers for reliable 5G communication systems. Today, he is focusing on highly digital integrated circuits such as fast time-to-digital converters, fault tolerant digital implementations and digitally-assisted communication systems for harsh environments. Within his group, he is pushing the limits of all-digital frequency synthesizers in extreme environments.

A 4GHz 0.73ps rms-Integrated-Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring PLL with a Jitter-Tracking DLL-Assisted DTC

Jaehong Jung, Samsung Electronics, Republic of Korea

This paper proposes a fractional-N sub-sampling ring PLL employing a jitter-tracking DLL-assisted DTC. The DTC achieves 0.49ps resolution and 0.98LSB rms INL with a dynamic range reduction through multi-phases of the DLT. In addition, an adaptive pulse-width control technique allows the loop BW to be insensitive to PVT, yielding <9.6% jitter variation. The proposed ring PLL fabricated in a 14nm FinFET CMOS process achieves 0.73ps rms-integrated jitter and 10.2mW power in fractional-N mode.

Jaehong Jung received the B.S. and M.S. degrees in semiconductor systems engineering from Sungkyunkwan University, Suwon, South Korea, in 2015 and 2017, respectively. He joined an Internship Program at Samsung Electronics, Hwaseong, South Korea, in 2014, where he has been with the Mixed Signal Core Design Team since 2017. His current research interests include high-speed serial links, phase-locked loops (PLLs), data converters, and clock generation circuit designs.

A 3.3-GHz 101fs rms-Jitter, −250.3dB FOM Fractional-N DPLL with Phase Error Detection Accomplished in Fully Differential Voltage Domain

Lianbo Wu, ETH Zürich, Switzerland

A fractional-N (frac-N) digital phase-locked loop (DPLL) that resolves the phase error (PE) in a fully differential voltage (FDV) domain is presented. It enables a PE digitization with higher CMRR, lower PVT sensitivity, finer resolution, and better linearity and is more power-efficient than gate-delay dependent time-domain (T-domain) approaches. The implemented DPLL covers the frac-N operation by a 10b DAC in voltage-domain (V-domain). A differential dv/dt ramp is employed to linearly transfer the fractional phase difference into a small voltage error, which is digitized by a narrow range but fine resolution 7b ADC. The DPLL achieves an integrated RMS jitter of 101fs with -56dBc worst-case fractional spur and consumes 9.2mW translating to a FOM of -250.3dB.

Lianbo Wu received the B.Sc. degree (with honors) from University of Science and Technology of China, Hefei, China, and the M.Sc. degree (cum laude) from Delft University of Technology, Delft, the Netherlands, both in electronic engineering, in 2012 and 2014 respectively. From 2013 to 2014, he worked at NXP, Eindhoven, the Netherlands as an intern. He is currently pursuing the Ph.D. degree at ETH Zurich, Switzerland.
A dual-feedback architecture for a fractional-N PLL is proposed to achieve low spurs and reduced phase noise degradation from the DSM. With the assistance of an auxiliary loop, the proposed architecture avoids noise amplification that occurs in conventional architectures. The architecture is demonstrated in a calibration-free 3.2-3.8GHz analog fractional-N PLL that achieves −69dBc out-of-band spurs and −66dBc worst-case in-band fractional spurs.

Masaru Osada received the B.S degree in electrical and electronic engineering from the University of Tokyo, Tokyo, Japan in 2019. He is currently pursuing his M.S. degree at the University of Tokyo Graduate School of Engineering.
CF2 Circuits Session - RF & mm-Wave Circuits

Session Chairs: Mike Chen (University of Southern California), Ho-Jin Song (POSTECH)

On-Demand Availability

Executive Sessions for Interactive Discussions, Paper Evaluator-Pitch Summaries and Q&A

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Related Live Event(s)

EG5 - Devices and Circuits for Advanced Communications - June-18 10:00 PDT / June-18 19:00 CET / June-19 02:00 JST (1 hour)

EH2 - High Speed Circuits, Systems, and Devices - June-18 17:00 PDT / June-19 02:00 CET / June-19 09:00 JST (1 hour)

CF2.1

A 29% PAE 1.5bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked PLL

Yuncheng Zhang, Tokyo Institute of Technology, Japan

This paper proposes a power-efficient digital polar transmitter using 1.5bit-DSM-based Class-D PA and fractional-N injection-locked PLL. The DSM-based polar transmitter can avoid redundant charge/discharge of turned-off transistors in the conventional SCFA, which contributes to a drastic improvement in power efficiency at power back-off. The PLL is used as the phase modulator, and spur-mitigation technique is also applied to minimize the frequency mismatch between the oscillator and the reference. The transmitter implemented in 65nm CMOS achieves a PAE of 29% at an EVM of -25.1dB, and a system efficiency of 21.7%.

Yuncheng Zhang received the B.S. and M.E. degrees in electrical engineering from University of Science and Technology of China (USTC) in 2013 and 2016, respectively. He is currently a Ph.D. candidate at the Tokyo Institute of Technology. His research interests include power-efficient wireless transceivers, all-digital phase-locked-loops, and analog-to-digital converters.

CF2.2

A 28GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation

Jian Pang, Tokyo Institute of Technology, Japan

This paper introduces a CMOS 28-GHz phased-array beamformer chip supporting dual-polarized MIMO (DP-MIMO) operation. A cross-pol. leakage cancellation technique is implemented for improving the degraded H-V isolation caused by the chips and the antennas. More than 40-dB cross-pol. isolation is maintained along the TX array to the RX array. This work also adopts a compact neutralized bi-directional architecture to minimize the chip manufacturing cost. The bi-directional PA-LNA realizes a peak PAE of 33.1% in PA mode and an NF of 5.4dB in LNA mode. With the improved cross-pol. isolation, 2×2 DP-MIMO communication with two 5G NR OFDMA-mode streams in 256QAM is achieved in the OTA measurement. The corresponding TX-to-RX EVM is -29.7dB. The power consumptions for each antenna path are 18mW in TX mode and 88mW in RX mode.

Jian Pang received the Bachelor and Master degrees from Southeast University, Nanjing, China, in 2012 and 2014, respectively, and the Ph.D. degree from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2019. He is currently a Researcher with the Tokyo Institute of Technology, focusing on 5G millimeter-wave systems. His current research interests include high-data-rate area-efficient millimeter-wave transceivers, power-efficient power amplifiers for 5G mobile system, MIMO, and mixed-signal systems. Dr. Pang was a recipient of the IEEE SSCS Student Travel Grant Award in 2016, the IEEE SSCS Predoctoral Achievement Award for 2018–2019, and the Seiichi Tejima International Student Research Award in 2020.

CF2.3

A 293/440 GHz Push-Push Double Feedback Oscillators with 5.0/ -3.9dBm Output Power and 2.9/0.6% DC-to-RF Efficiency in 65nm CMOS

Dzuhri Radityo Utomo, Korea Advanced Institute of Science and Technology, Republic of Korea

This paper proposes the concept of double-\(G_{\text{max}}\) core based regenerative amplifier which, in principle, breaks the gain barrier of \(G_{\text{max}}\): maximum achievable gain) core based regenerative amplifier which, in principle, breaks the gain barrier of \(G_{\text{max}}\) (the highest gain that can be obtained from a single transistor) at the frequencies below the maximum oscillation frequency of the transistor. Regenerative amplifiers adopting the proposed double-\(G_{\text{max}}\) core are implemented in a 65 nm CMOS technology and measurements show the peak gain of 18 and 15 dB, 9 and 7.5 dB per stage, at 247 and 272 GHz, respectively, while dissipating a DC power of 21.5 mW.

Dzuhri Radityo Utomo received B.Eng. degree from the Department of Electrical and Information Engineering, Universitas Gadjah Mada (UGM), Yogyakarta, Indonesia in 2014. He received M.S. and Ph.D. degrees from the School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea in 2016 and 2019, respectively, where he joined as a post-doctoral researcher from 2019 to 2020. He joined the Department of Electrical and Information Engineering, Universitas Gadjah Mada (UGM), Yogyakarta, Indonesia as a faculty member in 2020. His research interests include mm-wave and sub-terahertz integrated circuits and systems based on CMOS technology.

CF2.4

A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-Gmax Gain Boosting Technique

Dae-Woong Park, imec, Republic of Korea

This paper proposes the concept of double-\(G_{\text{max}}\) core based regenerative amplifier which, in principle, breaks the gain barrier of \(G_{\text{max}}\) (the highest gain that can be obtained from a single transistor) at the frequencies below the maximum oscillation frequency of the transistor. Regenerative amplifiers adopting the proposed double-\(G_{\text{max}}\) core are implemented in a 65 nm CMOS technology and measurements show the peak gain of 18 and 15 dB, 9 and 7.5 dB per stage, at 247 and 272 GHz, respectively, while dissipating a DC power of 21.5 mW.

Dae-Woong Park was born in Daegu, South Korea, in 1987. He received the B.S. degree from the Department of Semiconductor Systems Engineering, Sungkyunkwan University, Seoul, South Korea, in 2013, and the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015 and 2018, respectively. From 2018 to 2019, he was with the Information and Electronics Research Institute, KAIST, as a Post-Doctoral Research Fellow. Since 2019, he has been with mm-wave team, Interuniversity Microelectronic Center (IMEC), Leuven, Belgium, as a researcher. His interests include device physics, extremely high-frequency (THz), mm-wave, RF integrated circuits, and systems.
A self-synchronizing minimum shift keying (MSK) receiver operating at 315-GHz RF is demonstrated in 65-nm CMOS. The receiver outputs digital bits and utilizes a PLL based architecture that includes a frequency doubler in the loop to achieve the 315-GHz operation. The receiver is used to form a 10-Gbps link with BER < 10^{-11} at an RF input power of -21-dBm without using separate frequency synchronization between the transmitter and receiver, and data equalization. The 315-GHz RF is the highest for self-synchronizing receivers and for MSK receivers.

Ibukun Momson is working towards his Ph.D. in electrical engineering at the University of Texas at Dallas, focusing on millimeter wave systems in silicon processes for broadband communications, imaging and radar. He received his B.S.E.E. from the University of Lagos, Nigeria and his M.S.E.E. from the University of Texas at Dallas. His current research interests include methods to efficiently and sustainably generate and utilize sub-THz signals for engineering applications.
**CF3 Circuits Session - IoT and Wireless Receivers**

Session Chairs: Alireza Zolfaghari (Broadcom), Chun-Huat Heng (National University of Singapore)

### On-Demand Availability

June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST → June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

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**CF3.1**

**SamurAI: a 1.7MOPS-36GOPS Adaptive Versatile IoT Node with 15,000x Peak-to-Idle Power Reduction, 207ns Wake-Up Time and 1.3TOPS/W ML Efficiency**

*Ivan Miro-Panades, Université Grenoble Alpes, CEA, LIST, France*

IoT node application requirements are torn between sporadic data-logging and energy-hungry data processing (e.g. image classification). This paper presents a versatile IoT node covering this gap in processing and energy by leveraging two on-chip sub-systems: a low power, clock-less, event-driven Always-Responsive (AR) part and an energy-efficient On-Demand (OD) part. The AR contains a 1.7MOPS event-driven, asynchronous Wake-up Controller (WuC) with 207ns wake-up time optimized for short sporadic computing. OD combines a deep-sleep RISC-V CPU and 1.3TOPS/W Machine Learning (ML) and crypto accelerators for more complex tasks. The node can perform up to 36GOPS while achieving 15,000x reduction from peak-to-idle power consumption. The interest of this versatile architecture is demonstrated with 105µW daily average power on an applicable classification scenario.

Ivan Miro-Panades received a M.S. degree in telecommunication engineering from the Technical University of Catalonia (UPC, Barcelona, Spain) in 2002, a M.S. and Ph.D.degrees in computer science from the University Pierre & Marie Curie (UPMC, Paris, France) in 2004 and 2008 respectively. He worked at Philips Research and STMicroelectronics before joining CEA, Grenoble, France in 2008, where he is currently a Research Engineer in digital integrated circuits. His main research interests are artificial intelligence, Internet-of-Things, low-power architectures, energy-efficient systems, and Fmax/Vmin tracking methodologies.

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**CF3.2**

**Industrial IoT with Crystal-Free Mote-on-Chip**

*Thomas Watteyne, Inria, France*

SCuM is a 2x3x0.3 mm\(^3\) system-on-chip that contains an ARM Cortex-M0 and a 2.4 GHz IEEE802.15.4 radio. This paper describes the two-step calibration routine needed to run a full 6TiSCH stack on SCuM. It is, to the best of our knowledge, the first time a fully standards-compliant protocol stack runs on a crystal-free radio, such that it can participate in a network with off-the-shelf radios.

Thomas Watteyne is an insatiable enthusiast of low-power wireless mesh technologies. He holds a Research Director position at Inria in Paris, in the EVA research team, where he leads a team that designs, models and builds networking solutions based on a variety of Internet-of-Things (IoT) standards. He is Senior Networking Design Engineer at Analog Devices, in the Dust Networks product group, the undisputed leader in supplying low power wireless mesh networks for demanding industrial process automation applications. Since 2013, he co-chairs the IETF 6TiSCH working group, which standardizes how to use IEEE802.15.4e TSCH in IPv6-enabled mesh networks, and is member of the IETF IoT Directorate. Prior to that, Thomas was a postdoctoral research lead in Prof. Kristofer Pister’s team at the University of California, Berkeley. He founded and co-leads Berkeley’s OpenWSN project, an open-source initiative to promote the use of fully standards-based protocol stacks for the IoT. Between 2005 and 2008, he was a research engineer at France Telecom, Orange Labs. He holds a Ph.D. degree in computer science (2008), an M.Sc. degree in networking (2005), and an M.Eng. degree in telecommunications (2005) from INSA Lyon, France. He is an IEEE Senior Member and is fluent in four languages.

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**CF3.3**

**A Multichannel, MEMS-Less ~99dBm 260nW Bit-level Duty Cycled Wakeup Receiver**

*Anjana Dissanayake, University of Virginia, USA*

This paper describes a ~99dBm sensitivity, 260nW 434 MHz ISM band wakeup receiver (WuRX) in 65nm CMOS without MEMS filters, which is 18dB better sensitivity than any prior MEMS-less sub-µW design. The WuRX supports a new Channel-Embedded OOK single-tone TX scheme to enable multichannel operation without a local oscillator, improving usability for long-range, high density IoT applications. Reconfigurable within-bit duty cycling of the tuned-RF front end trades power for latency between 260µs latency at 2.17µW and 2.6s latency at 260nW.

Anjana Dissanayake received the B.S. (2015) and M.S. (2017) degrees from the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), South Korea. He is currently a doctoral candidate at RLP-VLSI and IECS groups at University of Virginia, USA. His current research interests include robust and interference resilient ultra-low power wake-up receivers and mixed-mode reconfigurable receivers.

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**CF3.4**

**CF3.4 - A 4.4µW ~92/~90.3dBm Sensitivity Dual-mode BLE/Wi-Fi Wake-Up Receiver**

*Po-Han Peter Wang, University of California San Diego, USA*

This paper presents the first dual-mode wake-up receiver (WuRX) that supports both BLE and Wi-Fi standards. The proposed WuRX achieves state-of-the-art power (as low as 4.4µW), sensitivity (as low as -92dBm), and interference resilience (SIR=-67dB) via a frequency plan that supports BLE advertisement channel hopping or a proposed subcarrier-based within-channel Wi-Fi frequency hopping scheme, a frequency conversion plan that enables a low power RX architecture, and an polyphase image rejection filter for full on-chip integration.

Po-Han Peter Wang received the B.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2011, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California at San Diego (UCSD), La Jolla, CA, USA, in 2014 and 2019, respectively. He was an RFIC Design Intern with Broadcom Corp., San Diego, CA, USA, in 2013. He is currently an RFIC Design Engineer with Broadcom Inc., San Diego, CA, USA. His research interests include the design of energy-efficient transceivers for wireless communications, reconfigurable RF front-ends and filters, and ultra-low-power mixed-
This paper presents the first low-power IC implementation of a 16-FSK receiver towards enabling energy-efficient wide area networking. The receiver specifically exploits the inherent 5.1dB $E_b/N_0$ advantage of 16-FSK over BFSK to improve sensitivity over prior-art, all while minimizing power via a bank of 16 integrated N-path filters for 16-FSK tone selection. Implemented in 65nm chip, the receiver achieves a sensitivity of -103dBm at a data rate of 100kbps, all at a power consumption of 0.6mW.

**Ali Nikoofard** received the M.S. degree in microelectronics from the Sharif University of Technology, Tehran, in 2014, and the M.S. degree in electrical engineering and computer science from Case Western Reserve University, Cleveland, OH, in 2017. Since 2017, he has been working toward his Ph.D. degree at the University of California, San Diego, under Prof. Mercier’s supervision. He was an RFIC Design Intern with MaXentric Technologies, San Diego, CA, in summers of 2018 and 2019 working on N-path filter design for GPS application and self-interference cancellation in transceivers using N-path filters as delay cells, respectively. He has co-authored a book “Introduction to Wireless Communication Circuits”. His current research interests include low-power RF transceiver and reconfigurable high-Q high-order bandpass filter design.
CF4 Circuits Session - Low Power Oscillators

Session Chairs: Danielle Griffith (Texas Instruments), Yoji Bando (Socionext)

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**CF4.1** A 8.7ppm/°C, 694nW, One-Point Calibrated RC Oscillator Using a Nonlinearity-Aware Dual Phase-Locked Loop and DSM-Controlled Frequency-Locked Loops

*Giorgio Cristiano,* ETH Zürich, Switzerland

This paper presents an on-chip timer composed of two DSM-controlled RC oscillators, locked through a non-linearity aware digital dual phase-locked loop. The proposed design achieves an accurate temperature coefficient below 8.7ppm/°C from 10 samples from two different wafer lots with only one-point calibration and an Allan deviation floor of 4 ppm. The power consumption is 694nW at 116 kHz.

*Giorgio Cristiano* is a Ph.D. student at the Institute for Integrated Systems at ETH Zürich, Switzerland. He received his B.S. in computer engineering from Politecnico di Torino, and his M.S. in micro- and nanotechnologies for integrated systems as a joint degree from Politecnico di Torino, Grenoble INP, and EPFL, Lausanne in 2016 and 2019 respectively. Mr. Cristiano joined ETH Zürich in November 2018. His research interests include frequency synthesizers and ultra-low-power systems.

**CF4.2** A 0.5V 560kHz 18.8fJ/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop

*Daniel Truesdell,* University of Virginia, USA

This work presents an on-chip oscillator for energy-efficient IoT applications based on a duty-cycled digital frequency-locked loop (DFLL). The digital implementation allows low-voltage operation at 0.5V to reduce energy and enable voltage rail integration with low-energy digital logic, while the duty-cycled operation further improves energy efficiency to a record value of 18.8fJ/cycle (10.5nW @ 560kHz) while maintaining a high temperature stability of 96.1ppm/°C from 0°C to 100°C.

*Daniel Truesdell* received the B.S. degree in electrical engineering from the University of Central Florida, Orlando, FL, USA, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Virginia, Charlottesville, VA. His current research interests include energy-efficient mixed-signal circuit design, on-chip oscillators and sensors, energy-harvesting and performance-scalable systems, and low-power digital circuit techniques.

**CF4.3** A 0.9pJ/cycle 8ppm/°C DFLL-based Wakeup Timer Enabled by a Time-Domain Trimming and an Embedded Temperature Sensing

*Ming Ding,* imec, Netherlands

An on-chip DFLL-based wakeup timer with a time-domain trimming featuring an embedded temperature sensor is presented. The proposed trimming exploits the deterministic temperature characteristics of two complementary resistors and results in a fine trimming step (±1ppm), allowing a small frequency error after trimming (<±20ppm). The temperature sensing is running in the background with negligible power (2%) and hardware overhead (<1%). The chip is fabricated in 40nm CMOS, consumes 380nW, resulting 0.9pJ/cycle energy efficiency while achieving 8ppm/°C from -40°C to 80°C.

*Ming Ding* received the B.Sc. degree in 2009 from Huazhong University of Science and Technology, China, M.Sc. degree (cum laude) in 2011 and Ph.D. degree in 2019 from the Eindhoven University of Technology, the Netherlands. From 2011, he has been with imec Netherlands, where he is now a senior research scientist. His research interests include ultra-low-power circuit design such as clock generations, data converters, ultra-low-power radio design for IoT and implantable applications. His research resulted in more than 20 papers, 2 book chapters, and 6 patents.
# CM1 Circuits Session - Advanced SRAM Design

**Session Chairs:** Igor Arsovski (Marvell), Tsung-Yung Jonathan Chang (TSMC)

## CM1.1 A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 175mV VMIN Reduction with Negligible Power Overhead

**Zheng Guo, Intel, USA**

A 21Mb/mm² SRAM design using 0.0367μm² HCC bitcell on a 10nm CMOS technology is presented. Gate-modulated self-collapse (GSC) write assist is utilized to enable 175mV reduction in \( V_{\text{min}} \) with minimal energy overhead. Array area overhead is limited to 3.5% by implementing the GSC circuitry in a row-based configuration with modified SRAM bitcells.

Zheng Guo received his M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley in 2005 and 2009, respectively. In 2010, Dr. Guo joined the Logic Technology Development Organization at Intel Corporation, where he currently leads a design team focused on advanced memory circuit technology for low-power, high-performance, and high-density applications.

## CM1.2 A 29.2Mb/mm² Ultra High Density SRAM Macro Using 7nm FinFET Technology with Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit

**Yoshisato Yokoyama, Renesas Electronics, Japan**

A 29.2Mb/mm² ultra high density SRAM macro has been proposed using 7-nm CMOS FinFET technology. The SRAM macro has only one SRAM cell array despite of the huge array of 512 rows x 512 columns. The circuitry of dual-edge driver for such long wordline and bitline in such huge array are newly proposed. The SRAM macro using proposed circuit was designed, and a test chip was fabricated using 7-nm CMOS FinFET technology. The minimum operation voltage is improved 170 mV by the new circuits.

Yoshisato Yokoyama received the B.E. degree from Chuo University in 2001, and the M.E. degree in electronics from the Tokyo Institute of Technology Tokyo, Japan, in 2003. He currently works on R&D of SRAM macro design in the Technology Development Unit, Renesas Electronics Corporation, Kodaira, Tokyo, Japan.

## CM1.3 Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1R1W 8T-bitcell SRAM in 10nm FinFET CMOS

**Jaydeep P. Kulkarni, Intel, USA**

A 1.09Mb, high density (HD), 1R1W 8T-bitcell SRAM is demonstrated in 10nm FinFET CMOS featuring Low Swing (LS) and Column Multiplexed (CM) bitline (BL) techniques. Read-Vmin and noise-tolerance is improved using a series NMOS clipper in the LBL read path and a split input NAND for early keeper turnoff. Measurements show 30(40)mV lower read-Vmin, 18(30)% lower BL power for the proposed LS (LS+CM) BL techniques, with improved noise tolerance, and minimal area overhead.

Jaydeep P. Kulkarni received the B.E. degree from the University of Pune in 2002, the M.Tech. degree from the Indian Institute of Science (IISc) in 2004, and Ph.D. degree from Purdue University in 2009 all in electronics/electrical engineering. During 2009–17, he was with Intel Circuit Research Lab, Hillsboro, OR where he worked on energy-efficient integrated circuit technologies. He is currently an assistant professor in electrical and computer engineering at the University of Texas at Austin and presently holds the AMD endowed chair position in computer engineering. His research focuses on machine learning hardware accelerators, in-memory computing, emerging nano-devices, hardware security and design methodologies for heterogeneous integration. He has filed 35 patents and published 75 papers. Dr. Kulkarni received the best M.Tech student award from IISc, SRC best paper and inventor recognition awards, Purdue outstanding doctoral dissertation award, seven Intel divisional awards, 2015 IEEE Transactions on VLSI systems best paper award, SRC outstanding industrial liaison award, and Micron faculty awards. He has served as General Co-chair for 2018 ISLPED, and is currently in CICC, ICCAD, and AICAS committees. He also serves as an associate editor for IEEE SSCL and Transactions on VLSI Systems. He currently chairs IEEE Central Texas SSCS/CAS joint chapter.

## CM1.4 2X-Bandwidth Burst 6T-SRAM for Memory Bandwidth Limited Workloads

**Charles Augustine, Intel, USA**

A 20KB 6T-SRAM array in 10nm CMOS demonstrates 2X higher read bandwidth in burst mode operation. The doubling of bandwidth is achieved with 51% higher energy efficiency than frequency doubling and 30% better area efficiency than doubling the number of banks.

Charles Augustine received the Bachelors in electronics from BITS, Pilani, India in 2004 and the Ph.D. degree in electrical and computer engineering from Purdue University in 2011. He is currently a Staff Research Scientist in the Circuit Research Lab (CRL) at Intel Corporation in Hillsboro, OR. Charles served as adjunct faculty in WSU, Vancouver from 2015 to 2018. He received patent recognition awards from Intel for 3 consecutive years (2015-2018), 2015 Mahboub Khan Outstanding Industry Liaison Award from SRC, Best Paper Award in International Symposium on Low Power Electronics and Design (ISLPED) in 2012, Best Paper in Session Award at SRC Techcon in 2009, AMD Design Excellence Award from Purdue in 2008, and won the Bronze Medal for academic excellence from BITS, Pilani in 2004. Charles currently serves as a TPC co-chair in CICC conference and as a TPC member in DAC conference. Charles has published more than 60 papers in refereed journals and conferences and has filed 34 patents (issued) and 4 patents (pending).
A 7nm Fin-FET 4.04-Mb/mm² TCAM with Improved Electromigration Reliability Using Far-Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier

Makoto Yabuuchi, Renesas Electronics, Japan

In the era where electromigration (EM) resistance is degraded by the continuous process advancement, we provide a solution to improve this EM resistance by 60% using our ternary content-addressable memory (TCAM). We designed the high-density TCAM macro in a 7nm Fin-FET process which includes novel circuitry: far-side driver of match and search line, and self-adjust reference match amplifier. Measurement shows that total active power in our proposed macro is 15% less than that in the conventional one. A 4.04 Mb/mm² marks the world highest memory density at this time.

Makoto Yabuuchi received the B.S. and M.S. degrees in electronic engineering from Kanazawa University, Japan in 2002 and 2004, respectively, and the Ph. D. degree in the Graduate School of Natural Science and Technology from Kanazawa University, in 2018. He joined Renesas Technology Corp. after his graduation and transferred to Renesas Electronics Corp. in 2010, where he has been working on designing embedded SRAMs for advanced CMOS logic process.
CM2 Circuits Session - Emerging Memory Design

Session Chairs: Seung Kang (Qualcomm Technologies), Makoto Miyamura (NEC)

On-Demand Availability

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CM2.1 A 14.7Mb/mm² 28nm FDSOI STT-MRAM with Current Starved Read Path, 52Ω/ Sigma Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference

El Mehdi Boujamaa, Arm, France

In this paper we present a read circuitry that tackles all STT-MRAM read challenges. First, a negative temperature coefficient (NTC) reference based on an MTJ in series with an "NTC" resistor circuit emulator is described. Then, an offset cancelled voltage sense amplifier using low read current and reference averaging is discussed. Measurement results show a maximum of 2% reference impedance error (vs. ideal) and 1.7% read error rate degradation (vs. technology intrinsic defectivity rate). A 14.7Mb/mm² memory density is also achieved, which is the best STT-MRAM published density for embedded applications.

El Mehdi Boujamaa was born in Oujda, Morocco, in 1983. He received the B.E. and M.E. degrees in electrical engineering from the University of Montpellier II (France), in 2003 and 2005, respectively. He also holds a Ph.D. in microelectronics also from the University of Montpellier II (France) in 2010. From 2011 onward, he was working as a memory R&D engineer for multiple companies including Infineon, Intel and ARM (current company). His research interests include MRAM, SRAM, and eFuse memories. He has written multiple scientific papers and is author and co-authors of 16 patents (5 granted, 11 pending).

CM2.2 Dual-Port Field-Free SOT-MRAM Achieving 90MHz Read and 60MHz Write Operations Under 55nm CMOS Technology and 1.2V Supply Voltage

Masanori Natsui, Tohoku University, Japan

We demonstrate an SOT-MRAM, a nonvolatile memory using spin-orbit-torque (SOT) devices that have a read-disturbance-free characteristic. The SOT-MRAM fabricated by a 55-nm CMOS process achieves 60-MHz write and 90-MHz read operations with a 1.2-V supply voltage under a magnetic-field-free condition. The SOT-MRAM is also implemented in a dual-port configuration utilizing a three-terminal structure of the device, which realizes a wide bandwidth applicable to high-speed applications. The main contributions of this work are summarized as follows. (1) A 4×4 SOT-MRAM is fabricated using a hybrid process of 55-nm standard CMOS and SOT devices on a 300-mm wafer line. (2) A dual-port memory configuration that enables a read-during-write operation is implemented. (3) A self-termination mechanism to prevent unnecessary current leakage during the read operation is implemented. (4) 60-MHz write and 90-MHz read operations are confirmed from the field-free measurement results of the fabricated prototype chip.

Masanori Natsui received the B.E. degree in electronic engineering and M.S. and Ph.D. degrees in information sciences from Tohoku University, Sendai, Japan, in 2000, 2002, and 2005, respectively. He is currently an Associate Professor with the Research Institute of Electrical Communication, Tohoku University, Sendai, Japan. His research interest includes automated circuit design technique, nonvolatile-based circuit architecture and its application, and design of high-speed low-power integrated circuits based on multiple-valued current-mode circuit technology. Dr. Natsui was the recipient of the IEEE Sendai Section Student Award in 2003, the Excellent Paper Award of The Institute of Electronics, Information and Communication Engineers of Japan in 2010, and the Kenneth C. Smith Early Career Award for Microelectronics Research in 2012.

CM2.3 A 28nm 1.5Mb Embedded 1T2R RRAM with 14.8 Mb/mm² Using Sneaking Current Suppression and Compensation Techniques

Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China

For the first time, 1T2R RRAM cell using PMOS selector is proposed and demonstrated with improved reset voltage and high density for embedded NVM. Hierarchical bit line and 3-state cell storage confine the associated sneaking current locally within a small zone and further suppress it by >90%. Self-adaptive write driver with current limiter and sneaking current compensator realizes power saving and accurate current compliance for set. To suit PMOS selector, reverse read using current sensing with dummy reference brings fast and reliable read. A 1.5Mb RRAM test chip in 28nm improved the record storage density by 40% to 14.8 Mb/mm². Reliable read is performed at low VDD of 0.6V@(-40, 125)°C.

Jianguo Yang is an associate professor in the Key Laboratory of Microelectronics Devices and Integrated Technology at Institute of Microelectronics of the Chinese Academy of Sciences. His research interests include circuit designs for volatile and nonvolatile memory, hardware security, memory-centric computing, and memristor logics. He has authored or co-authored several technical papers such as JSSC, Symposium on VLSI, TVLSI, TCAS-II, ASSCC, ISCAS, ESSCIRC & ESSDERC, etc. Some of his recognitions include two Best Paper Awards from the IEEE International Conference on ASIC on high-performance memory circuit design. He has participated in several large industry and government-sponsored center-level projects. He earned a Ph.D. from Fudan University (Shanghai, China).
An RRAM macro equips a hybrid self-tracking reference and a low ripple charge pump is presented to realize the configurable read windows and a consistent write performance over operation voltage range 1.62V–3.63V. It shows 6.5ns and 10ns of access time at 0.7V can be achieved for OTP (one-time-program) and 10K endurance applications, respectively.

Chung-Cheng Chou received the M.S.E.E. degree in 1992 from National Taiwan University. He joined Ti-Acer in May 1994 and contributed in Product Engineering and SPICE modeling. He then joined TSMC in January 1998 until now. During 22 years with TSMC, he has contributed to circuit design for DRAM, MRAM and RRAM. He is currently a manager responsible for RRAM macro design. He holds 48 U.S. patents.
CM3.1 A 28nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation  
(HOYOUNG SHIN)  
Hoyoung Shin, Samsung Electronics, Republic of Korea  
In this paper, we present an Embedded Flash Memory (eFlash) based on logic-28nm process for Internet of Things (IoT) product. IoT product requires high performance, low power operation and immunity to the high temperature. Based on a power-efficient 28nm process technology, we implemented the ultra-deep sleep model (<1µA). Through the WL Boosting and Adaptive Control Sensing Scheme (WBACS), we achieved fast read speed (3.2 Gbit/s) and robust sensing margin. High voltages can be generated stably in ultra-low power IO 1.1V by using Double-Boost-Clock (DBC). Through the technique that positive/negative Bi-Directional Charge Pump (BDCP), three high voltages required for Program/Erase operation can be generated from two charge pumps. As a result, we have developed an area competitive eFlash IP (Size 1.27 mm²). Based on these technologies, it was confirmed that 28nm-eFlash operates at ultra-low power (Core-VDD 0.85V & IO 1.1V) and high temperature (Tj 150°C) successfully. And these technologies were mounted in the world’s first 28nm process MCU-Connectivity One Chip Solution.  
Hoyoung Shin received the B.S. degree from ChungAng University, Korea in 2013. He is currently an engineer at Samsung Electronics SLSI division since 2013, designing embedded flash memory. His research interest is in embedded non-volatile memory.

CM3.2 A 65nm 16kb SRAM with 131.5pW Leakage at 0.9V for Wireless IoT Sensor Nodes  
(SHOURYA GUPTA)  
Shourya Gupta, University of Virginia, USA  
This paper presents a 16kb SRAM that achieves an ultra-low leakage of less than 132pW across its entire operational VDD range (0.3-0.9V). It is implemented using a new robust two-port bitcell with 614aW leakage, which, to the best of the authors’ knowledge, is the lowest leakage bitcell reported to date. Additionally, new peripheral techniques enable 1000x reduction in bit-line (BL) leakage, up to 89% improvement in access speed at low VDD, and up to 63.6% reduction in peripheral circuitry area over state-of-the-art works. The SRAM achieves an array area efficiency of 67.87%, leakage power of 51.8pW to 131.5pW for VDD at 0.3V and 0.9V, and >6.5 MHz access frequency.  
Shourya Gupta was born in New Delhi, India, in 1994. He received the B.Tech. degree in electronics and communications engineering from Guru Gobind Singh Indraprastha University, New Delhi, India in 2017. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Virginia, Charlottesville, VA, USA. His current research interests include the design of low-power logic and memory circuits in emerging and exploratory technologies.

CM3.3 1.03pW/bit Ultra-Low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors  
(JINGCHENG WANG)  
Jingcheng Wang, University of Michigan, USA  
A stacked voltage domain SRAM is proposed where arrays are split into two sets (top and bottom) with their supplies connected in series. System supply current is reused by top and bottom sets, and supply voltage is divided among the two sets of arrays, enabling seamless integration of very low voltage SRAM retention in a larger system with a nominal supply, without need for an efficiency-reducing LDO. An array swapping approach provides stable access to arbitrary banks within one system clock cycle. A comprehensive sizing strategy (W&L) is employed to optimally balance hold stability and bitcell size. Integrated in an IoT imaging system in 40nm CMOS, the proposed 8.9Mb SRAM achieves 1.03pW/bit leakage, a >100x reduction over conventional SRAM in the same technology.  
Jingcheng Wang received the B.S. degree in electrical engineering and computer science from both University of Michigan, Ann Arbor, MI, USA, and Shanghai Jiao Tong University, Shanghai, China, in 2014, and the M.S. degree from the University of Michigan in 2017, where he finally received the Ph.D. degree in electrical and computer engineering in 2020. His previous research projects include low-power and low-leakage SRAM design, near-in-memory computing, and neural network accelerators, and global interconnect.

CM3.4 Z-PIM: An Energy-Efficient Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision  
(JI-HOON KIM)  
Ji-Hoon Kim, Korea Advanced Institute of Science and Technology, Republic of Korea  
This paper presents Z-PIM, an energy-efficient processing-in-memory (PIM) architecture that supports zero-skipping operations and fully-variable weight bit-precision for efficient deep neural network (DNN). The 8T-SRAM cell based bit-serial operation with hierarchical bit-line structure enables variable weight precision and reduces bit-line switching by 95.42% in convolution layers of VGG-16. Z-PIM handles abundant zeros in weight data by skip-reading their corresponding input data while read-sequence rearranging and pipelining improves throughput by 66.1%. In addition, diagonal accumulation logic is proposed to accumulate both partial-sums for bit-serial operation and spatial products. As a result, the Z-PIM chip fabricated in a 65nm process consumes average 5.294mW power and achieves 0.31-49.12 TOPS/W energy efficiency for convolution operations as sparsity and weight bit-precision vary from 0.1 to 0.9 and 1b to 16b, respectively.  
Ji-Hoon Kim received the B.S. degree in electrical engineering from Kyung-Hee University, Suwon, South Korea, in 2017 and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2019, where he is currently pursuing the Ph.D. degree. His current research interests span various aspects of hardware system design including low power deep learning and intelligent vision SoC design with memory architecture, hardware accelerator for distributed computing system, computer architecture, and hardware/software co-design for hardware development.
### CP1 Circuits Session - Amplifiers

**Session Chairs:** Hylas Lam (Analog Devices), Kuan-Dar Chen (MediaTek)

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<td>EG4 - Sensing Interfaces and Building Blocks - June-18 09:00 PDT / June-18 18:00 CET / June-19 01:00 JST (1 hour)</td>
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#### CP1.1 A −107.8dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier

**Huajun Zhang,** Delft University of Technology, Netherlands

This paper describes a class-D audio amplifier with a multi-level output stage that reduces both EMI and idle power. High loop gain, and thus high linearity, are enabled by a relatively high (4.2 MHz) switching frequency, which relaxes the requirements on its output LC filter. Fabricated in a 180nm BCD technology, it can drive 14 W into an 8-Ω load with state-of-the-art performance: −107.8 dB THD+N, 91 % peak efficiency, and 7 mA quiescent current. It meets the CISPR 25 Class 5 radiated emission standard with a low-cost 580 kHz LC filter, improving the state-of-the-art by 5.8x.

Huajun Zhang was born in Beijing, China. He obtained the B.E. degree in electrical and computer engineering from Shanghai Jiao Tong University in 2015 and the B.S.E. and M.S. degrees in electrical engineering from the University of Michigan, Ann Arbor in 2015 and 2017, respectively. From May 2017 to February 2019, he was a Mixed-Signal Design Engineer with Analog Devices, Inc., Norwood, MA, USA. Mr. Zhang joined the Electronic Instrumentation Laboratory at TU Delft in March 2019 where he is pursuing the Ph.D. degree in microelectronics. His technical interests include precision analog circuits, Class-D audio amplifiers, and data converters.

#### CP1.2 An 8Ω, 1.4W, 0.0024% THD+N Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Mode Achieving Low Standby Quiescent Current of 660μA

**Ji-Hun Lee,** Korea Advanced Institute of Science and Technology, Republic of Korea

In this paper, a Class-D audio amplifier (CDA) with bridge-tied load half-side switching (BTLHS) mode is presented. The BTLHS mode through a digital pulse width subtractor (DPWS) enables low quiescent current (IQ) by suspending the output switching at idle condition while maintains high linearity with seamless zero-crossings and mode change. The CDA achieves 0.0024% THD+N, IQ of 0.66mA, and 95% peak efficiency on an 8Ω-speaker. The chip was fabricated in a 0.18-μm CMOS, and it occupies 0.83mm².

Ji-Hun Lee received the B.S. and M.S. degrees in electrical engineering from KAIST, Daejeon, Korea, in 2014 and 2016, respectively. He is currently pursuing the Ph.D. degree at KAIST. His research interests include designs of power converters, mixed-modes, and Class-D audio amplifiers for mobile applications.

#### CP1.3 Sample and Average Common-Mode Feedback in a 101nW Acoustic Amplifier

**Rohit Rothe,** University of Michigan, USA

This work presents a Sample and Average Feedback Resistor (SAFR) that effectively controls the High-Pass corner across PVT variations with the added benefit of corner frequency programmability. Using this approach, the variation across temperature and process corners is reduced by 226x and 4.38x respectively as compared to a conventional pseudo-resistor. The SAFR was implemented in a low-power audio LNA + PGA + ADC chain, achieving a resistance of 100 TΩ and HP corner programmability from 16 mHz to 4 Hz.

Rohit Rothe received the B.Tech. and M.Tech. degree in electrical engineering from the Indian Institute of Technology Bombay, Mumbai, India, in 2018. He is currently pursuing the Ph.D. degree in electrical and computer engineering at the University of Michigan, Ann Arbor, MI, USA. His current research interests include ultra-low power analog VLSI design.

#### CP1.4 A 0.0046mm² 6.7μW Three-Stage Amplifier Capable of Driving 0.5-to-1.9nF Capacitive Load with >0.68MHz GBW without Compensation Zero

**Hongseok Shin,** Korea Advanced Institute of Science and Technology, Republic of Korea

This paper presents a high-gain energy-efficient three-stage amplifier which employs buffering-based pole relocation and a dual-path structure (BPR-DP). The proposed design does not rely on the introduction of compensation zero and preserves the unity-gain bandwidth of the local feedback loop (LFL), thus improving FOM_L by 1.36 times, LC-FOM_L by 1.26 times, and LC-FOM_L by 3.18 times, as well as the performance robustness, compared to the state-of-the-art designs.

Hongseok Shin received the B.S. degree from Ajou University, Gyeonggi-do, South Korea, in 2015, and the M.S. degree from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2017, all in electrical engineering. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering at KAIST. His current research interests include analog circuits about power management IC for mobile and wireless power transfer IC for biomedical application.
This paper presents a single-trim switched-capacitor (SC) CMOS bandgap reference (BGR) for battery monitoring applications. A β-compensation technique, which is used in conjunction with mismatch averaging, and discrete time (DT) domain curvature correction are proposed to minimize non-PTAT errors. The remaining PTAT errors are cancelled out by using a single room-temperature (27°C) trimming. Implemented in a 0.18μm CMOS, the proposed SC BGR achieves a 3σ inaccuracy of +0.02%, -0.12% and an average temperature coefficient (TC) of 4.3ppm/°C from -40ºC to 125°C. It consumes 17μA at 27°C from 1.8V supply.

Jun-Ho Boo received the B.S. degree in electronic engineering from Sogang University, Seoul, South Korea, in 2017, where he is currently pursuing the Ph.D. degree. His current research interests include analog and mixed-signal circuits, data converters, and sensor interface.

This work introduces a compact voltage reference operating at pW-power and 250-mV supply (e.g., direct harvester-powered). Body biasing assisted by replica biasing enables 25μV/°C temperature coefficient, 140μV/V line sensitivity, and 0.42mV process sensitivity in 180nm. 2.55-mV overall accuracy is achieved at 2,200μm² area, without trimming.

Jun-Ho Boo, Sogang University, Republic of Korea

CP2.2 A 0.25-V, 5.3-pW Voltage Reference with 25μV/°C Temperature Coefficient, 140μV/V Line Sensitivity and 2,200μm² Area in 180nm

Longyan Lin, National University of Singapore, Singapore

This work presents a 4-channel, mm-scale, electrostatic and piezoelectric actuator driver that uses < 1μA total quiescent bias current and can drive actuator loads up to 120-330V at frequencies over 1kHz. The driver achieves over 99% current efficiency and can operate untethered with an integrated photovoltaic array driven by a collimated or diffuse optical power source. The circuit is tested with an off-chip boost circuit, generating over 1.5kV with 85% power efficiency at 45mW load. The circuit is tested with an off-chip boost circuit, generating over 1.5kV with 85% power efficiency at 45mW load. The system uses a simple 4-bit CMOS logic level interface with 100 kHz clock to actuate high voltage channels; on-chip photovoltaics also power the digital controller, and I/O bus.

Jan Rentmeister received the B.S. degree in 2015 from the University of Kassel, Germany. He is currently a graduate student at Dartmouth College where he is conducting research on high density and integrated power converters. His research interests include resonant switched capacitor power supplies with a special focus on self-finance students abroad.

CP2.4 A 120-330V, Sub-μA, 4-Channel Driver for Microrobotic Actuators with Wireless-Optical Power Delivery and Over 99% Current Efficiency

Jan Rentmeister, Dartmouth College, USA

To achieve a misalignment-free wireless power transfer (WPT), an IC for an adaptive magnetic field adder (AMFA), where the magnetic fields from multiple transmitter (TX) coils are adaptively added based on the coupling coefficient (k) between each TX coil and the receiver (RX) coil, is realized for the first time. A 6.78 MHz AMFA IC fabricated in 1.8 V, 180nm CMOS integrating four power amplifiers (PAs) and shared k sensor increases the perpendicular WPT efficiency from 0.02 % to 48.2 % with the load power of 458 mW.

Hao Qiu received the B.S. degree in materials science and M.Eng. degree in electrical engineering from Nanjing University, China, in 2010 and 2013, and Ph.D. degree in electrical engineering from The University of Tokyo, Japan, in 2016, respectively. After graduation, he has been a researcher in The University of Tokyo. His research interest covers from materials, devices, to circuits. His present emphasis is circuit design for wireless power transfer and wireless communication systems for IoT applications. Dr. Qiu served as the research fellow in the Japan Society for the Promotion of Science (JSPS) from 2015 to 2017 and the representative in Japan Society of Applied Physics (JSAP) from 2016 and 2018. He was the recipient of 2016 IEEE EDS Japan chapter student award and 2017 Chinese government award for outstanding self-finance students abroad.

CP2.3 A 6.78MHz Wireless Power Transfer System Enabling Perpendicular Wireless Powering with Efficiency Increase from 0.02% to 48.2% by Adaptive Magnetic Field Adder IC Integrating Shared Coupling Coefficient Sensor

Hao Qiu, University of Tokyo, Japan

To achieve a misalignment-free wireless power transfer (WPT), an IC for an adaptive magnetic field adder (AMFA), where the magnetic fields from multiple transmitter (TX) coils are adaptively added based on the coupling coefficient (k) between each TX coil and the receiver (RX) coil, is realized for the first time. A 6.78 MHz AMFA IC fabricated in 1.8 V, 180nm CMOS integrating four power amplifiers (PAs) and shared k sensor increases the perpendicular WPT efficiency from 0.02 % to 48.2 % with the load power of 458 mW.

EE1 - Ultra Low Energy Systems - June-17 10:00 PDT / June-17 19:00 CET / June-18 02:00 JST (1 hour)

EE1 - Ultra Low Energy Systems - June-17 10:00 PDT / June-17 19:00 CET / June-18 02:00 JST (1 hour)
CP3.1   
(Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching)

Dong Yan, University of Texas at Dallas, USA

This paper reports an automotive-use 5-24V V_{IN} to 1V V_{O} GaN-based power converter that achieves 20dBμV electromagnetic interference (EMI) reduction with anti-aliasing multi-rate (MR) spread-spectrum modulation (SSM) and in-cycle zero-voltage switching (ZVS). Compared to classic fixed-rate (FR) SSM, the proposed MR-SSM technique accomplishes 29% further EMI reduction, with the use of an active shaping controller. To improve the efficiency, an elastic t_{dead} control facilitates in-cycle ZVS switching despite of random f_{SW} variation caused by any SSM. The design was implemented on a 180nm BCD process, with an active die area of 0.87mm². It achieves a peak efficiency of 90.2% over a load range of 0.01 to 1.2W.

Dong Yan received the B.E. degree in electronic information science and technology and the M.E. degree in microelectronics from Harbin Institute of Technology (HIT), Harbin, China, in 2014 and 2016, respectively. Currently, he is currently pursuing the Ph.D. degree in electrical engineering at the University of Texas at Dallas, Richardson, TX, USA. His research interests include high step-down voltage conversion GaN-based power converters and analog and mixed-signal ICs.

CP3.2   
(Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 65nm CMOS)

Xun Sun, University of Washington, USA

This paper describes a digital control architecture for integrated voltage regulators (IVRs) that achieves time-optimal transient supply-voltage (V_{IN}) response under random load-current (I_{LOAD}) fluctuation. Implementing low-complexity low-latency Model Predictive Control (MPC) is key to achieving a measured 2.49X settling-time (\tau_{sett}) improvement over optimally tuned Proportional Integral Differential (PID) control.

Xun Sun received the B.S. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA and from Shanghai Jiao Tong University, Shanghai, China in 2016. Currently, she is pursuing the Ph.D. degree in electrical engineering at the University of Washington, where she is a member of the Processing Systems (PSy) Lab. Her research interests include integrated power converters, low-power mixed-signal circuits and the application of control ideas to power-management problems.

CP3.3   
(An N-Path Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting Achieving 13.9x Power Extraction Improvement)

Loai Salem, University of California, Santa Barbara, USA

N-path passive mixers have been employed in RF systems to realize high-Q impedance matching in an ultra-small size. In this paper, an N-path passive mixer is utilized to provide conjugate impedance matching between a piezoelectric transducer (PT) and a dc load to maximize the power transfer from the PT. Measurements of the 180nm CMOS prototype demonstrate 13.9x improvement in extracted power compared to an ideal full-bridge rectifier.

Loai G. Salem is an assistant professor in Electrical and Computer Engineering at the University of California, Santa Barbara. He received the Ph.D. degree in electrical and computer engineering from the University of California San Diego in 2018, the M.Sc. degree in microelectronics system design from Nile University, Egypt, in 2011, and the B.Sc. degree in electronics and communication engineering from Cairo University, Egypt, in 2008. His research interests include the design of efficient power converters using innovative circuits in scaled CMOS for a range of applications from high power to biomedical systems. Prof. Salem was a recipient of the 2019 DARPA Young Faculty Award, the 2017 IEEE Solid-State Circuits Society Predoctoral Achievement Award, the 2016 International Solid-State Circuits Conference Analog Devices Outstanding Student Designer Award, and the ECE Departmental Fellowship at the University of California, San Diego.

CP3.4   
(A 4V-0.55V Input Fully Integrated Switched-Capacitor Converter Enabling Dynamic Voltage Domain Stacking and Achieving 80.1% Average Efficiency)

Tim Thieleman, MICAS-Katholieke Universiteit Leuven, Belgium

This paper introduces a novel DC/DC converter topology to increase the average efficiency for wide input voltage ranges as required in capacitive energy storage applications. The FSM-controlled system places four stacked loads piecwise in parallel, while a reconfigurable ladder converter compensates for load imbalance and a gearbox converter guarantees efficient and continuous operation during the whole discharge cycle of the storage capacitor. Measurements on a 40nm prototype show a best-in-class wide input range average efficiency of 80.1% while supplying four dynamically stacked loads from a 4V-0.55V discharging storage capacitor.

Tim Thieleman was born in Leuven, Belgium, in 1993. He received the B.Sc. and M.Sc. degrees in electrical engineering from KU Leuven, Heverlee, Belgium, in 2014 and 2016, respectively. In 2016, he joined as a research assistant the ESAT-MICAS research group at KU Leuven, where he is currently pursuing a Ph.D. degree in the field of fully integrated power management circuits in baseline CMOS.
A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency

Xiaosen Liu, Intel, USA

A dual-rail hybrid analog/digital LDO achieves both high efficiency and tunable high PSRR simultaneously using a dynamic current steering mechanism. Measurements on a 22nm CMOS test chip demonstrate up to -46dB PSRR and 89% efficiency across 0-80mA load from 1.8V/1.05V dual-input rails.

Xiaosen Liu received the B.S. degree in electrical engineering from the Southeast University, Nanjing, China, the M.Phil. degree from the Hong Kong University of Science and Technology, Hong Kong, and the Ph.D. degree from the Texas A&M University, College Station, in 2008, 2011, and 2016 respectively. He is currently a research scientist in Circuit Research Lab of Intel Labs, OR, USA. He was a recipient of the 2015-2016 Solid-State Circuits Society Predoctoral Achievement Award, 2016 Chinese Government Award For Outstanding Self-Financed Students Abroad, and TPC member of IEEE SOCC, MWSCAS, and ISQED. His current research interests include power management for next-generation SoC, energy harvesting, wide-bandgap electronics, and electrosurgical instruments.

A Domino Bootstrapping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 96% High Efficiency

Hsuan-Yu Chen, National Chiao Tung University, Taiwan

The proposed monolithically integrated 12V Gallium Nitride (GaN) driver utilizes a domino bootstrapping technique to an on-chip 650V enhancement mode Gallium Nitride (eGaN) in a GaN process. The proposed self-biasing loop (SBL) reduces the quiescent current to 120μA and achieves 96% high efficiency. Furthermore, derivative-voltage divided by derivative-time (dV/dt) controller with a dual current supply (DCS) technique is proposed to modulate the slew rate of eGaN HEMT from 53.3V/ns to 12.5V/ns.

Hsuan-Yu Chen received the B.S. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2019. He is currently working toward the Ph.D. degree at the Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan.
CW1 Circuits Session - Ultra-High-Speed Wireline

Session Chairs: Jon Proesel (IBM), Jri Lee (National Taiwan University)

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<td>EG5 - Devices and Circuits for Advanced Communications</td>
<td>June-18 10:00 PDT / June-18 19:00 CET / June-19 02:00 JST (1 hour)</td>
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CW1.1 A 4x112 Gb/s ADC-DSP Based Multistandard Receiver in 7nm FinFET

Haidang Lin, Rambus, USA

This paper describes a 4 x 112 Gb/s digital receiver targeting Long Reach (LR) channels. The discrete time front-end overcomes gain-BW limitations to provide 10+dB gain at 28GHz. A 56GS/s ADC then converts the signal to 6-b digital consuming only 195mW. The following DFE-FFE based digital equalizer is capable of compensating 36 dB loss achieving BER of 2e-5. Furthermore, TDC and ISI filter based low latency timing recovery meets jitter tolerance specs over a wide range of data rates (25Gb/s NRZ to 106.25Gb/s PAM-4). The overall receiver consumes 338mW with 3.18pJ/bit energy efficiency.

Haidang Lin received the B.S. degree in electrical engineering and computer science from the University of California at Berkeley in 1996, and the M.S. degree in electrical engineering from Stanford University in 1998. He held various design positions with Teridian, MoSys, and Altera. In 2013, he joined Inphi Corporation, Santa Clara, CA, USA to design high speed transceivers. From 2017 to 2019, he was with Rambus Incorporated, Sunnyvale, CA, USA, working on high speed transceiver front ends. He is currently with Microsoft Corporation. His research interests include high speed low power transceiver circuits.

CW1.2 A 25-50Gb/s 2.22pJ/b NRZ RX with Dual-Bank and 3-tap Speculative DFE for Microprocessor Application in 7nm FinFET

Yang You, IBM, USA

This work presents an NRZ receiver (RX) implementation for microprocessor application in 7nm FinFET CMOS technology. It covers data rate from 25 to 50Gb/s and features on-chip AC coupling to support a wide input common-mode range. The RX includes two identical banks with their own clock and data recovery (CDR) to dynamically tackle parameter drift over time. A quarter-rate 3-tap fully speculative decision feedback equalizer (DFE) opens eyes over channel with 30dB insertion loss. Current-mode logic (CML) based clock path boasts three degrees of freedom of phase adjustment and random jitter (RJ) attenuation to broaden the eyes. At 0.9V supply the energy-efficiency is 2.22pJ/b with 28% eye opening (BER<10^-12) at 50Gb/s with PRBS31 and channel loss of 20dB.

Yang You graduated from Southern Methodist University in 2015 with a Ph.D. degree in electrical engineering. Since then, he has joined IBM's microprocessor chip design team in Austin, Texas, where he is now a senior engineer.

CW1.3 A 4-to-18GHz Active Poly Phase Filter Quadrature Clock Generator with Phase Error Correction in 5nm CMOS

Wei-Chih Chen, TSMC, Taiwan

We present a high-accuracy wideband quadrature clock generator (QCG) built in 5nm FinFET CMOS. To achieve low power and high bandwidth, we employ an active poly phase filter (APPF) to generate the quadrature phases with 6dB gain boost and 30% bandwidth extension. The subsequent quadrature error corrector (QEC) and phase error detector (PED) corrects the APPF output phases with phase interpolation to achieve <1° quadrature error across 4-18GHz. At 18GHz, jitter integrated across 100kHz–1GHz and 100kHz–9GHz is respectively 148 and 218fs with 154fs rms phase jitter measured at 14GHz. The noise floor is below –138dBc/Hz at 1GHz offset. The QCG occupies 0.0017mm² and consumes only 21mW on a 1.0V supply to yield a FoM of 1.16mW/GHz.

Wei-Chih Chen received the M.S. degree in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2004. He is currently a Technical Manager in the Mixed-Signal Design Department at TSMC, and working on high-speed circuit design and backplane data transceiver development in advance CMOS technology.
### CW2 Circuits Session - Wireline Techniques

**Session Chairs:** Parag Upadhyaya (Xilinx), C. Patrick Yue (Hong Kong University of Science and Technology)

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#### CW2.1 A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ Calibration for Memory Interfaces

**Yong-Un Jeong,** Seoul National University, Republic of Korea

This paper presents a single-ended transmitter (TX) with a voltage-mode (VM) PAM-4 driver. The proposed driver simultaneously satisfies impedance matching and linearity, and occupies a small area without resistors and inductors. A ZQ calibration scheme that automatically and precisely adjusts the PAM-4 driver is also addressed. The proposed calibration has three calibration points, which allow the driver to have high linearity by taking into account the impedance variations of the TX and the receiver (RX) according to the output levels. The prototype chip is fabricated in 65 nm CMOS process and occupies 0.033 mm². The proposed TX achieves a data rate of 28 Gb/s/pin with the level separation mismatch ratio (RLM) of 0.993 while consuming 0.64 pJ/b.

Yong-Un Jeong received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2013. He is currently pursuing the Ph.D. degree with Seoul National University, Seoul. His current research interests include design of high-speed I/O circuits, clock generation circuits, display interface, and memory interface.

#### CW2.2 A 0.1pJ/b/dB 28Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler

**Moon-Chul Choi,** Seoul National University, Republic of Korea

This paper presents a forwarded-clock receiver (RX) that consists of a weight-adjusting sign-sign Mueller-Müller clock and data recovery (CDR) and an adaptive decision-feedback equalizer (DFE) with a single shared error sampler. Only two samples per bit are utilized for both CDR and adaptive DFE, which minimizes clocking power consumption. In addition, a maximum-eye tracking algorithm is proposed to enhance the vertical eye margin without any extra high-speed analog circuitry. The RX fabricated in a 28nm CMOS technology achieves BER less than $10^{-12}$ with a 20dB-loss channel. It occupies an active area of 0.108 mm², and consumes 56.65 mW at 28 Gb/s.

Moon-Chul Choi received the B.S. degree in electrical and electronic engineering from Chung Ang University, Seoul, Korea, in 2015. He is currently working toward the Ph.D. degree at Seoul National University under the supervision of Prof. Deog-Kyoon Jeong. His current research interests include integrated circuits for silicon photonics and high-speed I/O circuits.

#### CW2.3 Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20GS/s 5b ENOB Analog-to-Digital Converter and 5GHz Phase Interpolator

**Sung-Jin Kim,** Stanford University, USA

Using digital standard cells and digital place-and route (PnR) tools, we created a 20 GS/s, 8-bit analog-to-digital converter (ADC) for use in high-speed serial link applications with an ENOB of 5.4, a DNL of 0.55 LSB, and an INL of 2.39 LSB, which dissipates 175 mW in 0.102 mm² in a 16nm technology. The design is entirely described by HDL so that it can be ported to other processes with minimal effort and shared as open source.

Sung-Jin Kim received his B.S. and M.S. in electrical and computer engineering from KAIST in 2008 and 2010 respectively. He is currently a Ph.D. student in electrical engineering at Stanford University. His current interests are synthesizable analog circuits and high speed serial links. Prior to starting the PhD program at Stanford, he was a research engineer at Samsung Electronics.

#### CW2.4 A 28mW 32Gb/s/pin 16-QAM Single-Ended Transceiver for High-Speed Memory Interface

**Jieqiong Du,** University of California Los Angeles, USA

A 32-Gb/s low-power single-ended 16-QAM transceiver using four signal levels is presented for high-speed memory interface. With four-bit per symbol, the transceiver increases the symbol period by 4x to enhance energy-efficiency by reducing the bandwidth requirement for most circuit blocks and mitigating equalization requirements. The transmitter achieves 16-QAM modulation by combining two QPSK modulators for linearity relaxation. Taking advantage of the DC-balanced 16-QAM signal, the receiver adopts a low-noise single-to-differential amplifier with a low-power DC feedback to recover the signal without requiring an external reference. The proposed transceiver achieves 0.875 pJ/bit at full rate while occupying 0.018 mm² in 28-nm CMOS technology.

Jieqiong Du received the B.S. degree in microelectronics from Shanghai Jiao Tong University, China, in 2012, and the M.S. and Ph.D. degrees in electrical engineering from University of California, Los Angeles (UCLA), in 2014 and 2019, respectively. She is currently an analog design engineer at Intel. Her research interests include high-speed mixed signal circuits and high-speed I/O links.
Memory Technology and Logic Technology have evolved along different paths. The emergence of new system architectures for heterogeneous compute has given new usage models for memory and potentially the need for new optimizations. Current AI/ML architectures are not well balanced with respect to memory performance and/or capacity, for instance. How will technology respond to this challenge? New memories? New architectures? Alternate technology optimization? Packaging solutions? This panel will bring together these different viewpoints to debate these questions.

Moderator: Gary Bronner, Rambus, USA

Gary Bronner is Senior Vice President of Rambus Labs, where he is responsible for his company’s long term research in memory devices, systems, and security. Prior to joining Rambus in 2006, he was at IBM where he was responsible for the development of many generations of DRAM and Logic technology. He has been an active participant in IEEE technical societies, serving as a reviewer for IEEE Trans. Electron Devices and EDL, past General Chair of IEDM, past Chair of the Cleo Brunetti Award committee, and a committee member of the IEEE SOI (now S3S) Conference. He is the author or co-author of over 80 issued US patents along with numerous journal and conference publications. He received his Sc.B. degree from Brown University and M.S. and Ph.D. degrees from Stanford University. He is a Fellow of the IEEE.

Panelist: Subramanian Iyer, University of California, Los Angeles, USA

All systems need to both think and remember and there are many ways to accomplish this. But today, even with advanced packaging constructs like interposers, communication between memory and logic accounts for greater than 30% of both the system power budget and chip real estate. Attempts to integrate large amounts of memory and logic, such as eDRAM are incremental at best, but do address the issue of latency, energy per bit and bandwidth. The new paradigm of heterogeneous dielet (or chiplet) integration at "fat-wire" type pitches (10nm) and close die spacing (~0+) allows for a System on Wafer (SoW) approach to build ultra-large and intimately connected systems that can address contemporary workloads without compromising either memory or logic - vive la difference!

Subramanian S. Iyer (Subu) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at UCLA. He is Director of the Center for Heterogeneous Integration and Performance Scaling (CIPHS). Prior to that, he was an IBM Fellow. His key technical contributions have been the development of the world’s first SiGe base HBT, salicide, electrical fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products. He also was among the first to commercialize bonded SOI for CMOS applications through a start-up called SiBond LLC. More recently, he has been exploring new packaging paradigms and architectures that they may enable including in-memory analog compute and medical engineering applications. He has published over 300 papers and holds over 75 patents. He is an IEEE Fellow, an APS Fellow and a Distinguished Lecturer of the IEEE EDS and EPS and a member of the Board of Governors of IEEE EPS. He is also a Fellow of the National Academy of Inventors. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012.

Panelist: Gabriel Loh, AMD, USA

AI/ML are driving a new surge in computation, memory performance, and memory capacity requirements, and attempts to simultaneously address all of these are often hamstrung by the power, latency, and bandwidth limitations of data movement. Bringing memory and logic technology back together (in some form) may have the potential to enable new AI/ML capabilities, but success highly depends on collaborative co-design across many different layers from devices to circuits and all the way to architectures and applications.

Gabriel H. Loh is a Senior Research Fellow in AMD Research, the research and advanced development lab for Advanced Micro Devices. He received his Ph.D. and M.S. in computer science from Yale University in 2002 and 1999, respectively, and his B.Eng. in electrical engineering from the Cooper Union in 1998. Dr. Loh was also a tenured associate professor in the College of Computing at the Georgia Institute of Technology, a visiting researcher at Microsoft Research, and a senior researcher at Intel Corporation. He is a Fellow of the ACM and IEEE, recipient of ACM SIGARCH’s Maurice Wilkes Award, Hall of Fame member for the MICRO, ISCA, and HPCA conferences, (co-)inventor on over one hundred US patent applications and sixty granted patents, and a recipient of an NSF CAREER Award. His research interests include computer architecture, processor microarchitecture, emerging technologies, and 3D die stacking.

Panelist: Steve Pawlowski, Micron, USA

Artificial Intelligence, or more specifically, Machine Learning exemplifies a new class of computing. As was typical for traditional computing, the memory BW and capacity are highly dependent on the algorithm and the architecture of the underlying device. For example, the number of bytes per operation necessary for the system to be compute limited can vary by at least an order of magnitude. With the race to higher TOPs (Tera OPerations per Second), balanced memory BW will have a power footprint that needs to be comprehended as well. In order to not repeat the focus on higher flops, while leaving the memory innovations behind, we need to address ML use cases and their impact to the memory architecture to insure that we create high efficiency ML based systems.

Steve Pawlowski is advanced computing solutions vice president at Micron Technology. He is responsible for defining and developing innovative memory solutions for the enterprise and high-performance computing markets. Prior to joining Micron in July 2014, Mr. Pawlowski was a senior fellow and the chief technology officer for Intel’s Data Center and Connected Systems Group. Mr. Pawlowski’s extensive industry experience includes 31 years at Intel, where he held several high-level positions and led teams in the design and development of next-generation system architectures and computing platforms. Mr. Pawlowski earned bachelor’s degrees in electrical engineering and computer systems engineering technology from the Oregon Institute of Technology and a master’s degree in computer science and engineering from the Oregon Graduate Institute. He also holds 58 patents.
Vivienne Sze, Massachusetts Institute of Technology, USA

It is increasingly important to bring memory and compute together in order to reduce data movement costs, which limits both the energy efficiency and throughput of today's processing systems. In-memory computing aims to address this by moving the compute into the memory; however, it is also faced with many challenges (e.g., increased sensitivity to circuit and device non-idealities). In order to address these challenges and realize the full potential of in-memory computing, it is critical to co-design across the entire stack including devices, circuits, architectures, and algorithms. For example, architecture exploration, and circuit/device development should be performed jointly rather than in isolation; and, deep neural networks should be designed to specifically target in-memory computing rather than using those designed for traditional processors (e.g., GPUs). Collaboration across research communities and design tools that can bridge these different layers of abstraction are key.

Vivienne Sze is an associate professor in MIT’s Department of Electrical Engineering and Computer Science and leads the Research Lab of Electronics’ Energy-Efficient Multimedia Systems research group. Her group works on computing systems that enable energy-efficient machine learning, computer vision, and video compression/processing for a wide range of applications, including autonomous navigation, digital health, and the internet of things. She is widely recognized for her leading work in these areas and has received many awards, including the Air Force Office of Scientific Research and DARPA Young Faculty Award, the Edgerton Faculty Award, faculty awards from Google, Facebook, and Qualcomm, the Symposium on VLSI Circuits Best Student Paper Award, the IEEE Custom Integrated Circuits Conference Outstanding Invited Paper Award, and the IEEE Micro Top Picks Award. As a member of the Joint Collaborative Team on Video Coding, she received the Primetime Engineering Emmy Award for the development of the High Efficiency Video Coding video compression standard. Sze earned a B.S. from the University of Toronto, and an M.S. and Ph.D. from MIT.

Keh-Chung Wang, Macronix International, Taiwan

Semiconductor industry continues to enhance memory and logic technologies on different paths due to device structure and operation requirement. AI/ML and other applications (IoT, 5G, etc.) will bring them together by 3D IC integration technologies. Memory-centric computing is emerging as a viable solution to complement traditional processor-centric computing. We propose a dream 3D-NVM with heterogeneous IC integration for future computing and data storage.

Keh-Chung Wang received a B.S. degree in physics from National Taiwan University and a Ph.D. degree in physics from California Institute of Technology. He joined Macronix as a Chief Scientist in 2015, responsible for emerging R&D in memory technologies and system applications. He served Hong Kong ASTRI as a Vice President and Group Director from 2009 to 2015, managing IC development for a broad range of applications. Before joining ASTRI, Dr. Wang was a Chief Engineer of UMC’s System & Architecture Support Division in USA, directing analog and RF IC development. During 1985–2005, he worked at Rockwell, Conexant, OpNext, and HRL. He had 35-year experience in IC design and management. He and his colleagues at Rockwell pioneered the development of GaAs HBT technologies that have been used broadly in RF power amplifiers of cellular phones. Dr. Wang co-authored about 200 journal and conference papers in the areas of physics, electronic devices, circuits, and systems. He served in numerous technical, advisory, and community-service committees. He was a guest editor of Journal of Solid-State Circuits. He was a recipient of Rockwell’s 1994 Engineer of the Year Award and 1995 Chairman’s Team Award. He is an IEEE Fellow.

Zhao Wang, Facebook, USA

In my opinion the divergence will become greater. Different AI/ML applications are accelerating this trend. Leading high tech companies like Facebook, Google, Amazon are exploring different ways of silicon development to maximize the optimization on their own workload, for example, different machine learning applications. Different applications and platforms will eventually create many different technology and design choices and options.

Zhao Wang received the Ph.D. in electrical and computer engineering from the University of Texas at Dallas in 2012. He is currently a ASIC designer with Facebook in the infra foundation group. Prior to Facebook he has worked on chip development and silicon technology in various companies including Texas Instruments, Qualcomm, Apple, Baidu, and TSMC. He has published 7 papers and filed 5 patents.
The last 40 years of progress in our field has been so explosive that it would have been impossible to forecast. The VLSI Symposium has chronicled the journey and can perhaps give us a glimpse of what lies ahead. We will be bringing a collection of thought leaders from the past and today to celebrate (and laugh at) the past and to try to predict the future.

**Panelist**

**Asad Abidi**, University of California, Los Angeles, USA

Asad Abidi is Distinguished Chancellor's Professor of Electrical and Computer Engineering at the University of California, Los Angeles. His research interests lie in RF-CMOS circuits, data converters, and other analog and mixed-signal circuits for communications. He is a frequent contributor to the Symposium on VLSI Circuits, who has missed attending only one symposium since its inception.

**Panelist**

**Tsu-Jae King Liu**, University of California, Berkeley, USA

Tsu-Jae King Liu earned her B.S., M.S. and Ph.D. degrees in electrical engineering from Stanford University. From 1992 to 1996 she worked at the Xerox Palo Alto Research Center as a Member of Research Staff. In August 1996 she joined the faculty of the University of California at Berkeley, where she presently is the Dean and Roy W. Carlson Professor of Engineering. Her research interests lie in RF- and mixed-signal integrated circuits for wireless and wireline communications, RF frontend circuits for wireless transceivers, and hardware-software co-design of RF transceivers for mobile platforms.

**Panelist**

**Akira Matsuzawa**, Tokyo Institute of Technology, Japan

Akira Matsuzawa received B.S., M.S., and Ph.D. degrees in EE from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Panasonic. Since then, he has been working on R&D of analog and Mixed Signal LSI technologies; video rate ADCs, CMOS sensors, RF CMOS, and MS SoC for DVD systems. On April 2003, he joined Tokyo Institute of Technology as a full professor. He has been researching in M/S technologies: millimeter-wave CMOS TRX, and advanced ADCs. He retired from Tokyo Institute of Technology on March 2018 and became an honorary professor. He is now a president of Tech Idea Co., Ltd., which he founded. He served the editor in chief of IEICE TRAN on electronics in 1992, 1997, and 2003, the Vice-TPC Chair for SSDM in 1999 and 2000, TPC for analog technology in ISSCC, the executive committee of VLSI Symposia. He received the R&D100 award in 1994, the ISSCC evening panel award in 2003, 2005, 2015, the MEXT science and technology award in 2017, and the IEICE great achievement award in 2019. He is an IEEE Fellow since 2002, and an IEICE Fellow since 2010.

**Panelist**

**Charlie Sodini**, Massachusetts Institute of Technology, USA

Charles G. Sodini received the B.S.E.E. degree from Purdue University in 1974, and the M.S.E.E. and Ph.D. degrees from the University of California, Berkeley, in 1981 and 1982 respectively. He was a member of technical staff at Hewlett-Packard Laboratories from 1974 to 1982 designing MOS memory. He joined the MIT faculty in 1983 where he is currently the LeBel Professor of Electrical Engineering. His research focuses on medical electronic systems for monitoring and imaging. He has served on a variety of IEEE conference committees, including IEDM where he was the General Chair in 1988. He has served on the IEEE EDS AdCom, was the SSCS President during 2002-2004, and Chair of the Executive Committee of the VLSI Symposia from 2006 to 2014. He serves on a variety of industry boards and is a IEEE Fellow.

**Panelist**

**Naveen Verma**, Princeton University, USA

Naveen Verma received the B.A.Sc. degree in electrical and computer engineering from The University of British Columbia, Vancouver, BC, Canada, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2005 and 2009, respectively. Since 2009, he has been with the Department of Electrical Engineering, Princeton University, Princeton, NJ, USA, where he is currently a Professor. His research focuses on advanced sensing systems, including low-voltage digital logic and DRAMs, low-noise analog instrumentation and data-conversion, large-area sensing systems based on flexible electronics, and low-energy algorithms for embedded inference, especially for medical applications. Dr. Verma was a recipient or co-recipient of the 2006 DAC/ISSCC Student Design Contest Award, the 2008 ISSCC Jack Kilby Paper Award, the 2012 Alfred Rheinstein Junior Faculty Award, the 2013 NSF CAREER Award, the 2013 Intel Early Career Award, the 2013 Walter C. Johnson Prize for Teaching Excellence, the 2013 VLSI Symposium Best Student Paper Award, the 2014 AFOSR Young Investigator Award, the 2015 Princeton Engineering Council Excellence in Teaching Award, and the 2015 IEEE Transactions on CPMT Best Paper Award. He is a Distinguished Lecturer of the IEEE Solid-State Circuits Society, and serves on the ISSCC, VLSI Symposia, DATE, and DISIPS technical program committees.
From the second design of an op-amp or NAND gate on to today designers have been trying to “automate circuit design”. Has this progressed from the Quixote quest of the past to a practical effort? Will and how well will it work? Will it replace circuit designers or assist them? We have assembled a mix of panelists with high level views and those in the trenches to assess the progress toward this goal and the effects of reaching it.

**Moderator**

**Chris Mangelsdorf**, Analog Devices, USA

Christopher W. Mangelsdorf received a B.S. in physics, magna cum laude, from Davidson College, Davidson, NC in 1977. In 1980 and 1984, he received the M.S. and Ph.D. degrees in electrical engineering at M.I.T. where he held the first Analog Devices Fellowship. He has been associated with Analog Devices since summer employment in 1980 and has been a Fellow of Analog Devices since 1998. From 1996 to 2013, Dr. Mangelsdorf worked in Tokyo, running the Analog Devices Tokyo Design Center and then adding responsibility for the Shanghai and Beijing Design Centers with the title of Asia Technical Director. In 2013, he moved to the Analog Devices San Diego office, where he is engaged in the development of high speed A/D converters. Dr. Mangelsdorf is a member of Phi Beta Kappa and Sigma Pi Sigma (physics), and has served on both the ISSCC Program Committee and the AdComm for the IEEE Solid-State Circuits Society. He holds 18 patents and has won the ISSCC Best Evening Session Award nine times.

**Panelist**

**Elad Alon**, University of California, Berkeley, USA

While I have no doubt that codified approaches will play a key role in future circuit designers activities, particularly in the analog/mixed-signal/custom space, I believe that machine learning (ML) techniques will be relegated to very specific tasks that designers don’t have any other (good) approach to solve. The reasons for this are both technical and human in nature, but in particular, that analog designers generally hate constraining tools to force them to not do “stupid” things (with “stupid” often being related to some unmodeled effect the tools can’t directly learn about), and that the space of stupid things a general purpose optimizer (of which ML can be considered a flavor) can do is enormous. Regardless of this, there is also no question in my mind that the “domain expertise” held by talented, knowledgeable, and/or experienced circuit designers will remain invaluable for the foreseeable future.

**Panelist**

**Linton Salmon**, Semi Tech Associates, USA

Machine Learning algorithms play a significant role in VLSI design and that role will continue to increase in the future. The first and largest contribution will be in the Verification, however the impact of Machine Learning will extend to many other areas of design as well. In spite of these advances however, Machine Learning is not a panacea that will solve all of the challenges posed by the ever increasing complexity of Leading-Edge SoC design. Meeting those challenges will require not only Machine Learning algorithms, but also advances in higher level hierarchical design and automation of design.

**Panelist**

**Nan Sun**, University of Texas at Austin, USA

The strong need to automate analog circuit design will eventually make it happen. The tasks of analog circuit sizing and layout design are not much harder than playing GO. I believe that we will witness a significant increase in the design automation level of analog circuits within the next 5 years, powered by state-of-the-art machine learning techniques. Within the next 10 years, I am optimistic that machines will be able to invent better circuit topologies that humans have never designed before.

**Nan Sun** is Associate Professor and holds the Temple Foundation Endowed Faculty Fellowship No. 5 in the Department of Electrical and Computer Engineering at the University of Texas at Austin. He received the B.S. degree from Tsinghua University in 2006 and Ph.D. degree from Harvard University in 2010. His current research interests include analog, mixed-signal, and RF-integrated circuits, miniature spin resonance systems, magnetic and image sensors, and micro-scale and nano-scale solid-state platforms (silicon ICs and beyond) to analyze biological systems for biotechnology and medicine. Dr. Sun was a recipient of the NSF Career Award in 2013 and the Jack Kilby Research Award from UT Austin in 2015 and 2016. He was the AMD Endowed Development Chair from 2013 to 2017. He serves on the IEEE CICC and A-SSCC Technical Program Committees. Dr. Sun is currently the Distinguished Lecturer of the IEEE Circuits-and-Systems Society. He serves as an Associate Editor for the IEEE Transactions on Circuits and Systems I and as a Guest Editor for the IEEE Journal of Solid-State Circuits.
Panelist  
David Wentzloff, University of Michigan, USA

ML and circuit design automation are increasingly important in the era of FinFETs where the complexity of design for manufacturability rules have outpaced the capability of tools used for traditional full-custom and manual design. ML can more efficiently identify patterns that result in successful designs. One challenge will be tapping the rich set of existing designs which can be used for training, since these are proprietary.

David Wentzloff received a B.S. from the University of Michigan, and Ph.D. from MIT, both in electrical engineering. He is currently a Professor of Electrical Engineering and Computer Science at the University of Michigan. His research focuses on mixed-signal and RF circuits, and design automation using a cell-based methodology for analog circuits that was pioneered in his group. In 2012, he co-founded Everactive, a fabless semiconductor company developing ultra-low power wireless SoCs, where he is currently the cc-CTO. He also serves on the Board of Directors at Movellus, which delivers PLL and DLL IP.

Panelist  
Kazuo Yano, Hitachi, Japan

Data always belongs to the past. The future cannot be predicted using past data. The widely used AI (supervised learning) only repeats past success and, hence, does not find new things. Reinforcement learning is limited to problems that can be simulated on computers. However, the decision in the complicated reality cannot be simulated. In order for AI to be used in Circuit Design with meaningful impact, it is necessary to switch to a new method which enables us to confront the unpredictability. I would like to propose how.

Kazuo Yano is a Fellow, Corporate Officer, Hitachi. He is known for pioneering work in the world’s first room-temperature single-electron memories in 1993, which ushered in the era of room-temperature operation of nanodevices. In 2003, he pioneered the measurement and analysis of social big data. He succeeded in quantifying the happiness of people from unconscious physical motion. He worked on the multi-purpose artificial intelligence which has been applied to many real cases. He has provided keynote and invited speeches on AI for human happiness at international conferences in Colombo, Dubai, Hanoi, Kyoto, Las Vegas, Los Angeles, London, Lausanne, Seoul, Singapore, Tokyo, etc. He has applied for over 350 patents and his papers are cited by over 2500 papers. His book, “The Invisible Hand of Data,” is cited as one of top-10 business books in Japan in 2014. He received 2020 IEEE Frederik Phillips Award and many other international awards, and is an IEEE Fellow.
P4 SSCS/EDS-Sponsored Diversity Panel -
Cultivating Engineering Confidence in COVID-19 Times

Organizers: Nadine Collaert (imec), Carolina Mora Lopez (imec)

Live Event
P4 Diversity Panel - June-16 08:00 PDT / June-16 17:00 CET / June-17 00:00 JST (1 hour)

On-Demand
Availability
June-17 09:00 PDT / June-17 18:00 CET / June-18 01:00 JST ➔ June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST. for recording of live event

The current COVID-19 pandemic has challenged the way we work, collaborate, communicate and socially engage with our colleagues, clients, and partners. In this panel, we would like to discuss how we can keep people motivated during the COVID-19 times and how we can use technology to change or accommodate the big impact of this crisis.

Moderator
Danielle Griffith, Texas Instruments

Panelist
Susan Feindt, Analog Devices

Susan Feindt is an ADI fellow and Director of Analog's Advanced Process Development Group in Wilmington, MA. She has been with Analog Devices for over 30 years. During her career at ADI, she has worked on multiple generations of complementary bipolar and BiCMOS processes; pioneering the use of bonded wafer SOI (silicon-on-wafer) substrates and full dielectric isolation on ADI's complementary bipolar processes. While continuing to advance Silicon based BiCMOS processes, her group also works on Gallium Nitride, Heterogeneous Integration, and other novel processes and devices. Before joining Analog Device, Susan worked for Harris Semiconductor in Melbourne, Florida. Susan received her B.S. in chemical engineering from the Massachusetts Institute of Technology. She serves on the boards for MIT's Microsystems Technology Laboratories, the new MIT.nano center, and the Singapore MIT Alliance for Research and Technology Low Energy Electronic Systems (LEES).

Panelist
Danielle Griffith, Texas Instruments

Danielle Griffith has been with Texas Instruments in Dallas, Texas since 2003 and is a Fellow in the Connectivity business unit. She develops circuits and techniques for reducing cost, power consumption, and circuit board area for wireless connectivity products that support standards such as Bluetooth Low Energy and Zigbee. Her current focus areas are architectures for efficient wireless systems, low power oscillators and MEMS circuits. She has published >50 papers, most of them in IEEE journals or conferences. She has written a book chapter titled “Synchronization Clocks for Ultra-Low Power Wireless Networks” which was published by Springer as part of the book "Ultra-Low-Power Short-Range Radios". Danielle holds 18 issued US patents and has given multiple university and IEEE conference tutorial and workshop sessions. She was a member of the Technical Program Committees for the IEEE RFIC Symposium for conferences years 2014 and 2015, the IEEE International Solid State Circuits Conference for conference years 2015-2019, and the VLSI Symposium starting in 2019. Danielle received the B.S.E.E. and M.Eng. degrees from the Massachusetts Institute of Technology, Cambridge in 1996 and 1997, respectively.

Panelist
Makoto Ikeda, University of Tokyo

Makoto Ikeda received the BE, ME, and Ph.D. degrees in electrical engineering from the University of Tokyo, Japan, in 1991, 1993 and 1996, respectively. He joined the University of Tokyo in 1996 and is now professor at d.lab and Department of Electrical Engineering and Information Systems, Graduate School of Engineering. He has been involved in VDEC activities to promote VLSI design education and research in Japanese academia and has initiated “AI chip design project” for Japanese startups, supported by Ministry of Economy, Trade and Industry (METI) of Japan. His research topics including hardware security, smart image sensor for 3-D range finding, and time-domain circuits including asynchronous controlling and associate memories. He has published more than 230 technical publications, including 10 invited papers, and 7 books/chapters. He served as an IEEE SSCS Distinguished Lecturer in 2015-2016, IEEE SSCS Japan Chapter Chair (2017-2018), IEEE Japan Council, Chapter Operation Committee Secretary (2007-2008), and has served numerous conference activities including symposium chair and program chair of VLSI Circuits Symposium, program chair or A-SSCC, and so on. He is now a International Program Committee Chair or ISSCC 2021, and AdCom member of IEEE SSCS. He is a senior member of IEEE, a senior member of IEICE, and a member of ACM and IPSJ.

Panelist
Myung-Hee Na, imec

Myung-Hee Na is a semiconductor technologist and currently work at imec as the Vice President of Technology Solutions and Enablement. She is currently responsible for CMOS and AI hardware technology research for new semiconductor era. Dr. Na received a Ph.D. in physics and started her career at IBM in 2001 where she held various technical, managerial and executive roles until early 2019. At IBM, she successfully led Research and Development for multiple generations of semiconductor technologies, including high-K metal gate, FinFET, and Nanosheet development. Moreover, she has co-authored numerous research papers and holds several U.S. and international patents.
Do You Really Know What Is In Your Computer? Perspectives on Verifiable Supply Chains

Andrew “bunnie” Huang, Singapore

We normally think of design verification as an activity that wraps up once a product goes to production. However, in the face of increasingly adversarial supply chains, it can no longer be taken for granted that the product’s intention matches the product received by the end customer. In this talk we will briefly overview the adversarial landscape of the supply chain, and then switch gears to discuss a range of potential solutions.

Andrew “bunnie” Huang is best known for his work hacking the Microsoft Xbox, as well as for his efforts in designing and manufacturing open source hardware, including the chumby (app-playing alarm clock), chibitronics (peel-and-stick electronics for craft), and Novena (DIY laptop). He received his PhD in EE from MIT in 2002. He currently lives in Singapore where he runs a private product design studio, Kosagi, and he actively mentors several startups and students.
YP - EDS/SSCS Young Professionals Event - Micro-Mentoring and Career Coaching

Organizers: Zeynep Lulec (Analog Devices), Camilo Vélez Cuervo (Real NanoMicro), Xinfei Guo (Nvidia), Ka-Meng Lei (University of Macau), Nilesh Pandey (Indian Institute of Technology Kanpur), Pragya Kushwaha (Indian Space Research Organization)

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<th>Live Event</th>
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We have been organizing mentoring sessions for our Young Professional (YP) and Student members over a decade, and as conferences are going online, we are transferring mentoring sessions to online as well. The event is structured as follows:

- EDS/SSCS introductions (5 minutes)
- Mentor introductions (5 minutes)
- Parallel mentoring sessions (40 minutes)

For the mentoring sessions, we will create breakout rooms for each mentor following a common brief introduction. We are aiming for around 5-10 mentees in each breakout room. As a mentee, you can join whichever room you choose and chat with the mentor assigned to that room. It will also be possible to switch between rooms if you wish to chat with different mentors during the event. The session is intended to go as a casual Q&A. To seed some discussions, we will provide mentors with a few starter questions such as:

- "Why did you choose academia/industry/entrepreneurship?"
- "Could you introduce your background and research briefly?"
- "Do you have any advice for people looking for a position in your field?"
- "What are the important skills a graduate student should gain during grad school?"
- "Do you have any advice on early career navigation?"
- "What are the future directions in your field of research?"

Everyone is welcome to participate. We look forward to seeing you in the event!
The purpose of this workshop is to outline the challenges and novel solutions to implement analog computing for machine learning (ML) hardware. Deep Neural Networks (DNN) constitute the state-of-the-art in AI, from image processing to translation and speech recognition. Energy-efficient DNN is key to bringing these capabilities to edge devices. Analog In-Memory Computing (AInMC) using novel technologies such as RRAM, PCM, MRAM is gaining a large interest due to superb energy-efficiency. However, implementation of AInMC in a primarily digital system brings new challenges that range from device specifications to system architecture definition. The objective of this workshop is to share innovations at both technology and design space to enable system-technology co-optimization for ML hardware.

WS1.1 Prospects of Analog In-Memory Computing – An Overview

**Boris Murmann**, Stanford University, USA

This introductory workshop presentation provides an overview of the aspects that make analog in-memory computing attractive for machine learning applications. It begins by reviewing asymptotic limits of purely digital implementations and estimates the benefits of moving to in-memory fabrics with reduced data movement. The discussion will include circuit details of “memory-like” topologies as well as SRAM and RRAM-based macros to project their achievable efficiency. Finally, this talk will summarize the most significant challenges with in-memory architectures, as for instance their A/D interface overhead and potentially limited programmability.

**Boris Murmann** is a Professor of Electrical Engineering at Stanford University. He joined Stanford in 2004 after completing his Ph.D. degree in electrical engineering at the University of California, Berkeley in 2003. From 1994 to 1997, he was with Neutron Microelectronics, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Since 2004, he has worked as a consultant with numerous Silicon Valley companies. Dr. Murmann’s research interests are in mixed-signal integrated circuit design, with special emphasis on sensor interfaces, data converters and custom circuits for embedded machine learning. In 2008, he was a co-recipient of the Best Student Paper Award at the VLSI Circuits Symposium and a recipient of the CICC Best Invited Paper Award. He received the Agilent Early Career Professor Award in 2009 and the Friedrich Wilhelm Bessel Research Award in 2012. He has served as a JSSC Associate Editor, an SSCS and AdCom member and Distinguished Lecturer, as well as the ISSCC Data Converter Subcommittee Chair and the Technical Program Chair. He is the founding faculty co-director of the Stanford SystemX Alliance and the faculty director of Stanford’s System Prototyping Facility (SPF). He is a Fellow of the IEEE. He is a Fellow of the IEEE.

WS1.2 Designing Material Systems and Algorithms for Analog Computing

**Robert L. Bruce**, IBM Research, USA

Deep learning has proven to be a major force in Big Data applications such as speech recognition, computer vision and natural language processing. However, there are opportunities to make exponential performance/power gains by looking to analog memory-based hardware accelerators to improve computational efficiency. The purpose of analog memory for deep neural networks is to encode weights into arrays of non-volatile memory devices to perform simple matrix operations in parallel and in constant time. Several implementations of this concept have been demonstrated using emerging memory technologies including phase change memory (PCM), resistive random access memory (RRAM) and electrochemical random access memory (ECRAM). The focus of this talk will be to review the upcoming memory technologies that can be used as analog memory weight elements for deep neural networks. Material requirements to achieve classification accuracy and to target training or inference applications will be discussed. Finally, we explain innovation of algorithms and hardware to overcome material limitations to vastly improve accuracy.

**Robert L. Bruce** received his B.S. from the University of Illinois at Urbana-Champaign in 2000 and Ph.D. from the University of Maryland, College Park in 2010, both in materials science and engineering. In the same year, he joined IBM T.J. Watson Research Center as a Research Staff Member. From 2010 to 2018, as a plasma etch expert, he delivered patterning solutions for GAA FET, III-V FET, phase change memory, photonics, DNA transistor and microfluidic technologies. In 2018, he joined the Phase Change Memory group. His current research interests are in phase change memory materials and integration for storage and AI. His work has been rewarded internally with several technical accomplishments, including the Research Division Award in 2017. He has authored or coauthored over 110 papers and presentations and is the holder of over 30 patents.

WS1.3 Monolithically Integrated RRAM-based Analog/ Mixed-Signal In-Memory Computing for Energy-Efficient Deep Learning

**Jae-Sun Seo**, Arizona State University, USA

Resistive RAM (RRAM) has been presented as a promising memory technology towards deep neural network (DNN) hardware design, with non-volatility, high density, high on-off ratio, and compatibility with logic process. However, prior RRAM works for DNNs have shown limitations on parallelism for in-memory computing, array efficiency with large peripheral circuits, multi-level analog operation, and demonstration of monolithic integration. In this talk, we present device-circuit-level optimizations to improve the energy and density of RRAM-based in-memory computing architectures. We report experimental results based on prototype chip design of 128x64 RRAM array and CMOS peripheral circuits, where RRAM devices are monolithically integrated in a commercial 90nm CMOS technology. We will discuss in-memory computing results based on both single-cell RRAM devices and 2-bit-per-cell RRAM devices. In addition, we employ input-splitting algorithm for DNN training so that ADCs at the array periphery could be reduced to binary sense amplifiers. Employing the proposed techniques, our RRAM based in-memory computing demonstrates up to 136 TOPS/W at 84% CIFAR-10 accuracy for single-cell RRAMs and 25 TOPS/W at 87% CIFAR-10 accuracy for 2-bit-per-cell RRAM.

**Jae-Sun Seo** received his Ph.D. degree from University of Michigan in 2010. From 2010 to 2013, he was with IBM T. J. Watson Research Center, where he worked on computer chip design for the DARPA SynNPSE project. In January 2014, he joined Arizona State University as an assistant professor in the School of ECEE. His research interests include energy-efficient hardware design for deep learning and neuromorphic computing. He was a recipient of IBM Outstanding Technical Achievement Award in 2012 and NSF CAREER Award in 2017.
WS1.4 Compute-in-Memory Circuit and Device Technologies: Trends and Prospects

Jaydeep P. Kulkarni, University of Texas at Austin, USA

With the emergence of machine learning and artificial intelligence applications, there is a growing need for large capacity memories to handle complex neural network parameters. The data movement from the memory to the processing engines incurs significant energy and latency costs (aka Memory Wall). Compute-in/near Memory approaches aim to mitigate these issues by performing specific ML workloads related computations within/near the memory array. In this part of the workshop, I shall focus on the Compute-in-Memory (CiM) approaches implemented in Static Random Access Memories (SRAM). I shall present various design topologies, analog matrix computation techniques, design tradeoffs and future design topics for efficient CiM designs.

Jaydeep P. Kulkarni received the B.E. degree from the University of Pune in 2002, the M.Tech. degree from the Indian Institute of Science (IISc) in 2004, and Ph.D. degree from Purdue University in 2009 all in electronics/electrical engineering. During 2009–17, he was with Intel Circuit Research Lab, Hillsboro, OR where he worked on energy-efficient integrated circuit technologies. He is currently an assistant professor in electrical and computer engineering at the University of Texas at Austin and presently holds the AMD endowed chair position in computer engineering. His research focuses on machine learning hardware accelerators, in-memory computing, emerging nano-devices, hardware security and design methodologies for heterogeneous integration. He has filed 35 patents and published 75 papers. Dr. Kulkarni received the best M.Tech student award from IISc, SRC best paper and inventor recognition awards, Purdue outstanding doctoral dissertation award, seven Intel divisional awards, 2015 IEEE Transactions on VLSI systems best paper award, SRC outstanding industrial liaison award, and Micron faculty awards. He has served as General Co-chair for 2018 ISLPED, and is currently in CICC, ICCAD, and AICAS committees. He also serves as an associate editor for IEEE SSCL and Transactions on VLSI Systems. He currently chairs IEEE Central Texas SSCS/CAS joint chapter.

WS1.5 Analog Computing for Machine Learning – An Ideal Case for Co-Optimization of System and Device Technology

Arindam Mallik, imec, Belgium

Energy-efficiency of ML hardware is a key motivating factor for Analog Computation In Memory (ACiM). In this presentation, I will share a path towards a 10000TOPS/W analog matrix-vector multiplier for DNN inference. To achieve such an objective, co-optimization of ML algorithm and device architecture is necessary. The primary objective of this presentation is to demonstrate how such a System Technology Co Optimization methodology can be put in place. At algorithm level, low precision quantization and training with variation and circuit errors would be discussed. For deriving device specifications for such a hardware, I will discuss how performing DNN inference in an analog hardware imposes additional constraints at circuit and technology level. An efficient implementation of ACiM will eventually allow for a minimization of silicon area (i.e. chip cost) while maintaining target accuracy, latency and throughput.

Arindam Mallik received his M.S, and Ph.D degrees in electrical engineering and computer science from Northwestern University, USA in 2004 and 2008, respectively. Arindam is a technologist working on Design Technology Co-Optimization techniques for the past 15 years. Arindam leads the device technology and DTCO interaction for imec's Machine Learning program as a Principal Member of Technical Staff. Arindam is a true believer of cross-domain research. He has authored or co-authored more than 100 papers in international journals, conference proceedings, and holds number of international patent families.

WS1.6 System and Architecture Level Considerations in Leveraging Mixed-Signal Techniques for ML at the Edge

Mahesh Mehendale, Texas Instruments, USA

ML at the Edge demands low power and low cost realization of Deep Neural Network (DNN) based inferencing. One of the primary techniques deployed is to reduce the DNN complexity via aggressive quantization of both weights and activations – especially for the compute intensive layers. At precision of 4 bits or lower, analog computation of convolutions embedded within the memory results in significantly lower power than conventional digital implementation. In this talk we highlight challenges that need to be addressed so as to realize this power advantage at the full application level while managing the impact to accuracy, latency and die-size. These include variability, ADC/DAC non-linearity, inaccuracies due to intermediate quantization, in-memory macro area overhead and in-efficient mapping for certain NN layer types. We also look at the entire signal chain “sensor interface => pre-processing/feature extraction => DNN => post-processing” and discuss opportunities for leveraging mixed-signal techniques beyond DNN acceleration.

Mahesh Mehendale is a Texas Instruments Fellow and works in the areas of ultra-low power circuits, architectures and systems at TI’s Kilby Labs. Presently he is focusing on embedded machine learning targeting “always-on” IoT sensor nodes. Mahesh has published more than 50 papers at international conferences/journals and presented many invited talks/tutorials. He holds 17 U.S. patents. He has co-authored a book on "VLSI synthesis of DSP kernels" and also two book chapters. Mahesh holds B. Tech degree (1984) in Electrical Engineering, M.Tech and Ph.D. degrees in computer science and engineering, all from Indian Institute of Technology (IIT) Bombay, from where he received the ‘Distinguished Alumnus Award’ in 2012. He was elected Fellow of the Indian National Academy of Engineers in 2016.
WS2 Workshop - Know Where You Are Going; Metrology In the New Age of Semiconductor Manufacturing

Organizers: Tom Larson (Nova Measuring Instruments), Gosia Jurczak (Lam Research)

On-Demand Availability
June-14 09:00 PDT / June-14 18:00 CET / June-15 01:00 JST → June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Related Live Event
PWS2 Workshop 2 Panel and Q&A - June-16 19:00 PDT / June-17 04:00 CET / June-17 11:00 JST (1 hour)
Recording available on-demand June-17 09:00 PDT / June-17 18:00 CET / June-18 01:00 JST → June 27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST

Measurement is at the forefront of every integration and process engineer’s daily life, whether for process control, development, yield ramping or failure analysis. But understanding the basics of how the measurements are made, what technologies are deployed and what challenges remain is not universal. This workshop will provide an outline overview from world class experts of the major technologies and approaches used now and looking into the future of inspection, process control and analysis. The overview sessions will provide the attendee with an understanding of how measurement data is produced, how it is used and how measurements solve critical problems every day. The agenda will span several talks from experts in the fab as well as experts from the fields of dimensional measurements, materials metrology, defect inspection and laboratory analysis including discussion around how machine learning is enhancing what we can extract from the data. The organizers hope the attendees will leave the workshop with a more robust understanding of how their measurement data is created and perhaps with a better understanding of how to use the data.

WS2.1 Introduction to Metrology Workshop
(PWS2)
Tom Larson, Nova Measuring Instruments, USA

Tom Larson is Vice President of New Business Innovation at Nova Reporting to the CEO, and is responsible for expanding Nova’s markets by strategic acquisition and innovation. He began his career at Tencor Instruments in applications engineering and progressing through various technical and product roles before and after the acquisition by KLA. He spent two years at Applied Materials helping with the first process modules using data integration from integrated metrology. He moved to Physical Electronics to lead their effort expanding from the analytical lab into the fab. In an unexpected series of events, the products defined in that effort formed the basis of ReVera - a spin-out from Physical Electronics co-founded by Mr Larson and three colleagues. ReVera defined the new market of Materials Metrology, formed around the first ever in-line XPS technology. Several years of adoption and success led to exciting acquisition of ReVera by Nova. Now known as the Materials Metrology Division, it continues to solve hard problems in process control with unique and compelling technologies. Tom holds a B.S. in physics from ASU.

WS2.2 Manufacturing Process Challenges and Requirements for Metrology in Semiconductor Memory Devices
(PWS2)
Keiji Suzuki, Kioxia, Japan

Keiji Suzuki is Sr. Manager Process Technology Development Department III at Kioxia where he manages the process technology department, which develops the process, simulation, metrology, analysis and production management system. Previously, he developed the manufacturing engineering for semiconductor or TFT-LCD process, especially plasma processing. He also led simulation technology (CAE, TCAD) team. Dr. Suzuki received his Ph.D. in engineering and has been working with Toshiba, now Kioxia, since 1997.

WS2.3 Metrology with Angstrom Accuracy Required by Logic IC Manufacturing – Challenges From R&D to High Volume Manufacturing and Solutions in the AI Era
(PWS2)
Yi Hung Lin, TSMC, Taiwan

Transistor trend is moving to Nanosheet from FinFET while AI is evolving one step closer to super-intelligence with generative deep learning. They are driving each other for breakthroughs. To craft such a 3D miniature at Angstrom-level accuracy with a large quantity, metrology inevitably becomes the enabler. The requirement is challenging every fundamental aspect of metrology from R&D to high volume manufacturing to innovate with AI; otherwise, no solutions appear feasible. This talk will discuss the challenges of four critical areas. Potential AI applicable and shortfalls will be introduced. The goal is to excite both worlds seemingly apart to collaborate closely.

Yi Hung Lin is Manager of the Advanced Metrology Engineering group at Taiwan Semiconductor Manufacturing Company, currently in charge of R&D in-line metrology development and deployment. He has been working in the areas of optical dimensional metrology and chamber physics simulations for two decades, and owns 132 papers/patents/trade-secrets. He joined TSMC in 2010 after serving as a TCAD technologist for 11 years at Intel, Santa Clara. Since then, his focus has been on machine learning to resolve challenges for in-line metrology. Dr. Lin received his Ph.D. in chemical engineering from the University of Maryland at College Park in 1999.
WS2.4 Dimensional Metrology Overview, Trends and Upcoming Challenges

Philippe Leray, imec, Belgium

Metrology, backbone of semiconductor industry, is facing 2 main challenges. The first one is due to the introduction of the third dimension in the construction of the devices (3Dnand, CFET, wafer bonding, etc). It requires the method used to investigate complex and eventually opaque structures to extract buried dimension. The second one is linked to the scaling of dimensions; metrology requires to achieve sub angstrom performance. These 2 problems need solution for the “absolute” metrology required for process characterization and the “relative” metrology to monitor high volume manufacturing. We will describe the trends and the development of existing solution, optical or SEM based, to solve these challenges. We will also show new emerging ideas like new sensors and the use of machine learning. Finally, we will propose extremely fast monitoring technique to avoid the challenges of “absolute” metrology and, instead, detect deviation from operating points.

Philippe Leray is Director of Advanced Patterning including metrology, etch and lithography at imec. After 4 years in plasma characterization in JRC-Ispra (Italy), he joined imec, Belgium in 2001. He worked in overlay targets design and optimization for implementation in IMEC pilot line. He ran evaluation of overlay emerging techniques (DBO and multi-layer target). He developed CD scatterometry models for IMEC processes (Fins, Gate and BEOL after CMP). He studied immersion defectivity issues when first immersion hoods was implemented. In 2014, he became group leader of the advanced metrology group in imec, and the technical leader of supplier hub with metrology companies (ASML, KLA, HHT, NOVA). Since last year, he is the director of the advanced patterning department of imec. He contributed to more than 60 publications in SPIE for metrology session. Dr. Leray received his Ph.D. in 1997 from the University Paris XI, France.

WS2.5 Defect Inspection: A Trio of Trends for the 2020s

Mark Shirey, KLA, USA

As we enter the 2020s, defect inspection for effective IC yield and reliability improvement is more important than ever. Mega trends like artificial intelligence, 5G connectivity, and autonomous transportation drive higher demand for a wide range of semiconductor devices, with the resulting advances in semiconductor technology creating many new challenges for defect inspection. We will explore a trio of defect inspection trends that are being driven to address these challenges: continued core technology innovation, implementing inspection strategies that monitor defects at their source, and data linkages and analytics that provide more effective yield improvement actions.

Mark Shirey is Vice President of Customer Engagement at KLA, working in the Semiconductor Process Control Group. He began his career as a college intern at KLA Instruments and has been at KLA for over 25 years. He has worked closely with customers around the world in implementing inspection and metrology solutions as an Applications Engineer and has held various management and product development roles across KLA. Mark holds a B.S. degree in International business from San Jose State University and M.B.A. from Santa Clara University.

WS2.6 Enabling Modern Semiconductor Manufacturing With Materials Metrology

Kavita Shah, Nova Measuring Instruments, USA

The growing adoption of new materials, along with innovative device concepts, heralds exciting opportunities for both metrology and process control. The manufacturing of advanced semiconductor devices is already extremely complicated. As process and integration complexities increase with the introduction of new materials, so do the interdependencies. Identifying the sources of variability and solving these challenges is becoming more difficult as the industry roadmap evolves. Today, conventional metrology technologies can fall short of the high-sensitivity and resolution needed to address an ever-evolving class of applications. Fabs either live with inefficient and expensive workarounds or, in many cases, run the processes blind. One contributing factor for this is the fixed mindset around fab metrology and process control, which has developed around dimensional scaling needs. Using examples, we discuss how early engagement in new in-line materials metrology enables fundamentally better direct process control and accelerates development for new process technologies. This emerging class of in-line materials metrology techniques has the potential to revolutionize semiconductor process control practices as the manufacturing paradigm shifts to enable radically different chip designs for the AI era.

Kavita Shah joined Nova’s Materials Metrology division in 2017. As Senior Director for Strategic Marketing, Kavita enjoys distilling technical and business complexity into actionable, forward-thinking strategies, with a focus on bringing new technologies to market. Before joining Nova, Kavita had a diverse 14-year career with Applied Materials, with roles in process development, product management, and back-end-of-line integration. Her efforts led to industry-wide adoption of the revolutionary Volta CVD Co technologies for liner and selective metal capping. Kavita has more than 20 patents and co-authored publications in semiconductor processing and hardware. She holds a Masters’ degree in chemical engineering from Cornell University.

WS2.7 Opportunities and Challenges for Lab-based Characterization for Emerging Technologies

Markus Kuhn, Intel, USA

Advanced CMOS technology development has evolved from the use of geometric scaling to the introduction of novel materials and non-planar architectures. With this there is an accelerating demand for enhanced analytical capabilities that not only include dimensional measurements but increasingly also the measurement of materials properties. Since lab-based methods can be more suited to provide these, there is an increasing trend to use lab methods in a hybrid/near-fab approach. Overall, it is a unique challenge that involves development and integration of advanced analysis capabilities/automation, emerging machine learning applications and equipment supplier ecosystems.

Markus Kuhn is Manager of the Analytical Pathfinding Group, Intel Quality Network tasked with leading Intel’s materials analysis pathfinding efforts. He joined Intel in 1998. Dr. Kuhn has published 100+ refereed papers and he holds 30+ patents in the areas of high k/metal gate, FinFET, and strain development for semiconductor applications. His research interests include the advancement of analytical capabilities and he has a broader interest in the synergies between analytical characterization methods, machine learning and process metrology to help enable emerging technologies. He received his Ph.D. in chemistry from the University of Western Ontario, London, Canada.
This workshop outlines the state of the art of quantum computing from material and integration to IC design and architecture and system. We will discuss and argue how quantum computing could be supported by our electrical engineering community and could provide a very aggressive path towards dedicated high performance computing problems. Through the workshop, we will try to provide a comprehensive and concise overview of the field of quantum computing enabled by VLSI technology.

**WS3.1 3D Integration and Challenges for Scaling**

*William Oliver, Massachusetts Institute of Technology, USA*

Quantum computers are fundamentally different than conventional computers. They promise to address important problems that are practically prohibitive and even impossible to solve using today’s supercomputers. The challenge is building one that is large enough to be useful. Superconducting qubits are a leading quantum computing technology today. They are coherent “artificial atoms” assembled from electrical circuit elements and microwave optical components. Their lithographic scalability, compatibility with microwave control, and operability at nanosecond time scales all converge to make the superconducting qubit a highly attractive candidate for the constituent logical elements of a quantum information processor. In this talk, we review the promise, progress, and challenges of quantum computing, with a focus on 3D integration of superconducting qubits.

*William D. Oliver* is jointly appointed Associate Professor of Electrical Engineering and Computer Science and Lincoln Laboratory Fellow at the Massachusetts Institute of Technology. He serves as the Director of the Center for Quantum Engineering and as Associate Director of the Research Laboratory of Electronics. Will’s research interests include the materials growth, fabrication, design, and measurement of superconducting qubits, as well as the development of cryogenic packaging and control electronics. Dr. Oliver is a Fellow of the American Physical Society, Senior Member of the IEEE, serves on the US Committee for Superconducting Electronics, and is an IEEE Applied Superconductivity Conference (ASC) Board Member. He received his Ph.D. in electrical engineering from the Stanford University in 2003.

**WS3.2 Superconducting Qubits: How Technology/ Processing/ Materials Impact Coherence Time and How Design Impacts Gate Fidelity**

*Doug McClure, IBM, USA*

Just over two decades since their first demonstration, superconducting qubits have become a leading quantum computing platform. An outlier among established qubit systems, superconducting qubits can be seen with the naked eye and can be tailor-made to have desired parameters using standard microfabrication and microwave design tools. Advances in coherence times, control and readout techniques, and multi-qubit device design have enabled the development of prototype quantum processors capable of running small quantum algorithms, which sit at the heart of most of today’s cloud-accessible quantum systems. In this talk I will review key principles of superconducting qubits, factors limiting their performance, and approaches being pursued to reduce decoherence and other sources of error.

Doug McClure is a Research Staff Member and Manager of Quantum System Deployment at IBM Research in Yorktown Heights, New York. Since joining IBM in 2012, he has focused on several aspects of building quantum computers based on superconducting qubits: improving quantum measurements, qubit coherence times, and most recently the performance and reliability of large multi-qubit systems. He received his PhD in experimental physics from Harvard University, where under the guidance of Professor Charlie Marcus he studied the physics of fractional quantum Hall states with potential applications in topological quantum computing.

**WS3.3 Si Based Qubits: Technology and Material Impact on Performance**

*Iuliana Radu, imec, Belgium*

Quantum computing is fundamentally different that classical computing but many of the technology challenges are similar to those for building classical systems. Building the first viable quantum computers comes with many challenges, some conceptual, yet many technological. In this talk, we outline how learning and practices from standard CMOS technology development can be used to enable quantum computing. We will discuss how materials and process development can improve device performance. We explain how standard modeling can be extended to describe accurately enough qubits.

*Iuliana P. Radu* is Director of Quantum and Exploratory Computing at imec. Her activities include work on beyond CMOS device concepts such as spintronic majority gates and wave computing and novel materials and their possible applications in the semiconductor industry. Quantum Computing includes work on qubit devices and the periphery circuits meant to control them. Prior to establishing the Beyond CMOS program at imec in 2013, she was a Marie Curie and FWO fellow at KU Leuven and imec. Her work encompassed devices using the metal to insulator transition, ionic and electronic transport in functional oxides, and devices with graphene and other 2D materials. Iuliana has received a Ph.D. in physics from MIT in 2009 where she searched for Majorana fermions in the quest to build very reliable qubits for Quantum Computing. She has been an author on over 170 papers in leading peer-reviewed journals and conferences. She has given more than 40 invited talks at international conferences and seminars where she is a frequent speaker on quantum computing and exploratory devices for classical computing. Currently a subcommittee co-chair for IEDM, and program committee member for SISC and SNW.
WS3.4  Architectures Challenges for Si Spin Qubits

Maud Vinet, CEA-Leti, France

Si-based QC appears as a promising approach to build a quantum processor; thanks to the size of the qubits, the quality of the quantum gates and the VLSI ability to fabricate billions of closely identical objects. The quality of Si spin qubits has improved very fast thanks to material and technology developments. Still there are lots of open questions on how to shape a quantum accelerator based on Si spin qubits. In this presentation, I will start with a description of the assumptions that are commonly used by the community to design one and two qubit-gates and will discuss the consequences on architecture for large scale quantum computing. I will review the propositions made in the literature and will present progress made towards the actual demonstration of these architectures.

Maud Vinet is currently leading the quantum computing program in Leti. Together with Tristan Meunier (CNRS) and Silvano de Franceschi (Fundamental research division from CEA), they received an ERC Synergy grant in 2018 to develop silicon based quantum computer. She defended a Ph.D. in physics from the University of Grenoble Alps and joined Leti in 2001 as a CMOS integration and device engineer. From 2009 to 2013, she spent 4 years with IBM to develop Fully Depleted SOI with IBM and STMicroelectronics. In 2015, she spent 6 month with Globalfoundries in Malta, NY to participate to the launch of 22FDX program. From 2013 to 2018, she managed the Advanced CMOS integration team activities in Leti (~50 people). In 2019, she was appointed project leader for the quantum computing program in Leti. Maud Vinet authored or co-authored about 200 papers and holds more than 70 patents related to nanotechnology. Her Google h-index is 42.

WS3.5  Cryogenic CMOS for Control of Transmon Qubits

Joseph Bardin, Google AI Quantum & University of Massachusetts Amherst, USA

Today's state-of-the-art superconducting qubits are controlled using a mixture of microwave and baseband waveforms. In this talk, we will first review the requirements for the control of contemporary quantum processors and explain how this task is achieved using arrays of high-performance arbitrary waveform generators. We will then show that, while this approach is appropriate for use with small-scale quantum processors, a more scalable approach will be required to move towards large-scale fault tolerant systems. We will then describe the design, implementation, and characterization of a prototype integrated quantum controller, which has been optimized to carry-out single-qubit gate operations on superconducting transmon qubits. The presentation will conclude with a discussion of future research that is required to enable the implementation of fault tolerant quantum computers.

Joseph Bardin received the Ph.D. degree in electrical engineering from Caltech in 2009 and joined the Department of Electrical and Computer Engineering at the University of Massachusetts Amherst in 2010, where he is currently an Associate Professor. In 2017, he joined the Google AI Quantum team as a visiting researcher and, in addition to his university duties, he currently serves as a research scientist with this team, focusing on integrated electronics for quantum computing. His research group at UMass Amherst focuses on the design of low power electronics for use at cryogenic temperatures and has made a number of important contributions in low noise amplifier and single photon detector technologies. He is an associate editor for IEEE Transactions on Quantum Engineering and IEEE Journal of Microwaves and a recipient of a 2011 DARPA Young Faculty Award, a 2014 NSF CAREER Award, a 2015 ONR YIP Award, a 2016 UMass College of Engineering Outstanding Junior Faculty Award, a 2016 UMass Award for Outstanding Accomplishments in Research and Creative Activities, and a 2020 IEEE MTT-S Outstanding Young Engineer Award.
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**7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing**  
*Sylvain Barraud, CEA-Leti-MINATEC, France*

#### TC1.4

**All-Operation-Regime Characterization and Modeling of Drain Current Variability in Junctionless and Inversion-Mode FDSOI Transistors**  
*Daphnée Bosch, CEA-Leti-MINATEC, France*

#### TC2.2

**Addressing Key Challenges for SiGe-pFin Technologies: Fin Integrity, Low-D_{it} Si-cap-free Gate Stack and Optimizing the**  
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#### TC3.2

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**Composite Interconnects for High-Performance Computing Beyond the 7nm Node**  
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**Improved Air Spacer Co-Integrated with Self-Aligned Contact (SAC) and Contact Over Active Gate (COAG) for Highly Scaled CMOS Technology**  
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*Anshul Gupta, imec, Belgium*
EA2 Executive Session - Sensor Systems

Session Chairs: Neale Dutton (STMicroelectronics)

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What is an Executive Session?

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Hyochan An, University of Michigan, USA

**CA2.2** A 0.05pJ/Pixel 70fps FHD 1Meps Event-Driven Visual Data Processing Unit
Somnath Paul, Intel, USA

**CA2.3** A 65nm Image Processing SoC Supporting Multiple DNN Models and Real-Time Computation-Communication Trade-Off via Actor-Critical Neuro-Controller
Ningyuan Cao, Georgia Institute of Technology, USA

**CA2.4** A Ray-Casting Accelerator in 10nm CMOS for Efficient 3D Scene Reconstruction in Edge Robotics and Augmented Reality Applications
Steven Hsu, Intel, USA

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Bogdan Raducanu, imec, Belgium

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Chengjie Zhu, Princeton University, USA

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<td>Huai-Yu Cheng, Macronix International, Taiwan</td>
<td>Macronix International, Taiwan</td>
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<tr>
<td>TM2.2</td>
<td>A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory</td>
<td>Weier Wan, Stanford University, USA</td>
<td>Stanford University, USA</td>
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<tr>
<td>TM2.3</td>
<td>Industrially Applicable Read Disturb Model and Performance on Mega-Bit 28nm Embedded RRAM</td>
<td>Chang-Feng Yang, TSMC, Taiwan</td>
<td>TSMC, Taiwan</td>
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EB2 Executive Session - Intelligent Computing

Session Chairs: Zhengya Zhang (University of Michigan), Vinayak Honkote (Intel)

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<td>June-16 09:00 PDT / June-16 18:00 CET / June-17 01:00 JST → June-27 23:59 PDT / June-28 08:59 CET / June-28 15:59 JST for recording of live event</td>
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What is an Executive Session?

**CA1.3**  
*Chieh-Fang Teng*, National Taiwan University, Taiwan

**CA1.4**  
A 4.45ms Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices  
*Dongseok Im*, Korea Advanced Institute of Science and Technology, Republic of Korea

**CA2.5**  
A 1200x1200 8-Edges/Vertex FPGA-Based Motion-Planning Accelerator for Dual-Arm-Robot Manipulation Systems  
*Takashi Oshima*, Hitachi, Japan

**CA3.1**  
Managing Chip Design Complexity in the Domain-Specific SoC Era  
*Yunsup Lee*, SiFive, USA

**CA3.4**  
MANA: A Monolithic Adiabatic iNtegration Architecture Microprocessor Using 1.4zJ/op Superconductor Josephson Junction Devices  
*Christopher Ayala*, Yokohama National University, Japan

**CA3.5**  
32GHz 6.5mW Gate-Level-Pipelined 4-bit Processor using Superconductor Single-Flux-Quantum Logic  
*Koki Ishida*, Kyushu University, Japan

**CM3.4**  
Z-PIM: An Energy-Efficient Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision  
*Ji-Hoon Kim*, Korea Advanced Institute of Science and Technology, Republic of Korea

**JFS4.4**  
PNPU: A 146.52TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping  
*Sangyeob Kim*, Korea Advanced Institute of Science and Technology, Republic of Korea
What is an Executive Session?

**CM1.4** 2X-Bandwidth Burst 6T-SRAM for Memory Bandwidth Limited Workloads  
*Charles Augustine*, Intel, USA

**CM2.1** A 14.7Mb/mm² 28nm FDSOI STT-MRAM with Current Starved Read Path, 52Ω/Σ Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference  
*El Mehdi Boujamaa*, Arm, France

**CM3.2** A 65nm 16kb SRAM with 131.5pW Leakage at 0.9V for Wireless IoT Sensor Nodes  
*Shourya Gupta*, University of Virginia, USA

**CM3.3** 1.03pW/b Ultra-Low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors  
*Jingcheng Wang*, University of Michigan, USA

**JFS3.3** Buried Powered SRAM DTCO and System-Level Benchmarking in N3  
*Shairfe Salahuddin*, imec, Belgium

**TF2.2** A Novel Dual Ferroelectric Layer Based MFMFIS FeFET with Optimal Stack Tuning Toward Low Power and High-Speed NVM for Neuromorphic Applications  
*Tarek Ali*, Fraunhofer IPMS Center Nanoelectronic Technologies, Germany

**TF2.4** Nanosecond Laser Anneal (NLA) for Si-Implanted HfO₂ Ferroelectric Memories Integrated in Back-End Of Line (BEOL)  
*Laurent Grenouillet*, CEA-Leti-MINATEC, France

**TF2.7** Probing the Evolution of Electrically Active Defects in Doped Ferroelectric HfO₂ During Wake-Up and Fatigue  
*Umberto Celano*, imec, Belgium

**TM1.4** Understanding of Tunable Selector Performance in Si-Ge-As-Se OTS Devices by Extended Percolation Cluster Model Considering Operation Scheme and Material Design  
*Shoichi Kabuyanagi*, Kioxia, imec, Japan

**TM2.1** A SiO₂ RRAM-Based Hardware with Spike Frequency Adaptation for Power-Saving Continual Learning in Convolutional Neural Networks  
*Irene Munoz-Martin*, Politecnico di Milano, Italy

**TMFS.2** Magnetic Random Access Memories (MRAM) Beyond Information Storage  
*Ricardo Sousa*, Université Grenoble Alpes / CEA / CNRS, Spintec, France
EC2 Executive Session - Analog Building Blocks

Session Chairs: Ewout Martens (imec)

### What is an Executive Session?

**CD1.2**
A 10-bit 100MS/s SAR ADC with Always-on Reference Ripple Cancellation
Xiyuan Tang, University of Texas at Austin, USA

**CD1.5**
A Compact 14GS/s 8-bit Switched-Capacitor DAC in 16nm FinFET CMOS
Pietro Caragiulo, Stanford University, USA

**CD2.1**
A 440μW, 109.8dB DR, 106.5dB SNDR Discrete-Time Zoom ADC with a 20kHz BW
Efraim Eland, Delft University of Technology, Netherlands

**CF1.2**
A Fast Locking 5.8–7.2 GHz Fractional-N Synthesizer with Sub-2μs Settling Time in 22nm FDSOI
Jeffrey Prinzie, Katholieke Universiteit Leuven, Belgium

**CF1.4**
A 3.3-GHz 101fs rms-Jitter, −250.3dB FOM Fractional-N DPLL with Phase Error Detection Accomplished in Fully Differential Voltage Domain
Lianbo Wu, ETH Zürich, Switzerland

**CF3.5**
CF3.5 - A 920MHz 16-FSK Receiver Achieving a Sensitivity of −103dBm at 0.6mW via an Integrated N-Path Filter Bank
Ali Nikoofard, University of California San Diego, USA

**CP1.1**
A −107.8dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier
Huajun Zhang, Delft University of Technology, Netherlands

**CP3.5**
A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency
Xiaosen Liu, Intel, USA

**JFS5.4**
A 3D-Stacked Cortex-M0 SoC with 20.3Gbps/mm2 7.1mW/mm² Simultaneous Wireless Inter-Tier Data and Power Transfer
Benjamin Fletcher, University of Southampton, United Kingdom
EC3 Executive Session - Adaptive Systems

Session Chairs: Bora Nikolic (University of California, Berkeley)

**Live Event**
June-16 10:00 PDT / June-16 19:00 CET / June-17 02:00 JST (1 hour)

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**What is an Executive Session?**

**CC2.2**
An Autonomous Reconfigurable Power Delivery Network (RPDN) for Many-Core SoCs Featuring Dynamic Current Steering
*Khondker Ahmed*, Intel, USA

**CD1.1**
A 1MS/s to 1GS/s Ringamp-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm
*Benjamin Hershberg*, imec, Belgium

**CD2.4**
A 1GS/s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9dB FoMs
*Yifan Lyu*, MICAS-Katholieke Universiteit Leuven, Belgium

**CF3.1**
SamurAI: a 1.7MOPS-36GOPS Adaptive Versatile IoT Node with 15,000x Peak-to-Idle Power Reduction, 207ns Wake-Up Time and 1.3TOPS/W ML Efficiency
*Ivan Miro-Panades*, Université Grenoble Alpes, CEA, LIST, France

**CP3.1**
An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching
*Dong Yan*, University of Texas at Dallas, USA

**CP3.2**
Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 65nm CMOS
*Xun Sun*, University of Washington, USA

**CP3.4**
A 4V-0.55V Input Fully Integrated Switched-Capacitor Converter Enabling Dynamic Voltage Domain Stacking and Achieving 80.1% Average Efficiency
*Tim Thielemans*, MICAS-Katholieke Universiteit Leuven, Belgium
# ED1 Executive Session - Heterogeneous Integration (1)

Session Chairs: Willy Rachmady (Intel), Osbert Cheng (UMC)

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## What is an Executive Session?

### JFS5.1
Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry: Multi-Tier Complementary Carbon Nanotube Logic and Resistive RAM at a 130 nm Node  
*Tathagata Srimani*, Massachusetts Institute of Technology, USA

### TH2.2
Surrounding Gate Vertical-Channel FET with Gate Length of 40nm Using BEOL Compatible High-Thermal-Tolerance In-Al-ZnOxide Channel  
*Hirokazu Fujiwara*, Kioxia, Japan

### TH2.3
Amorphous IGZO TFTs featuring Extremely-Scaled Channel Thickness and 38nm Channel Length: Achieving Record High \( G_{m,\text{max}} \) of 125 \( \mu S/\mu m \) at \( V_{DS} \) of 1V and \( I_{ON} \) of 350\( \mu A/\mu m \)  
*Subhranu Samanta*, National University of Singapore, Singapore

### TH3.4
First Demonstration of Low Temperature (≤500°C) CMOS Devices Featuring Functional RO and SRAM Bitcells toward 3D VLSI Integration  
*Claire Fenouillet-Beranger*, CEA-Leti-MINATEC, France

### TH3.5
Flexible and Transparent BEOL Monolithic 3DIC Technology for Human Skin Adaptable Internet of Things Chips  
*Ming-Hsuan Kao*, Taiwan Semiconductor Research Institute, Taiwan
# ED2 Executive Session - Power

**Session Chairs:** Hylas Lam (Analog Devices), Sung-Wan Hong (Sookmyung Women’s University)

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## What is an Executive Session?

**CP1.2** An 8Ω, 1.4W, 0.0024% THD+N Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Mode Achieving Low Standby Quiescent Current of 660μA  
Ji-Hun Lee, Korea Advanced Institute of Science and Technology, Republic of Korea

**CP1.4** A 0.0046mm² 6.7μW Three-Stage Amplifier Capable of Driving 0.5-to-1.9nF Capacitive Load with >0.68MHz GBW without Compensation Zero  
Hongseok Shin, Korea Advanced Institute of Science and Technology, Republic of Korea

**CP2.1** A Single-Trim Switched Capacitor CMOS Bandgap Reference with a 3σ Inaccuracy of +0.02%, -0.12% for Battery Monitoring Applications  
Jun-Ho Boo, Sogang University, Republic of Korea

**CP2.2** A 0.25-V, 5.3-pW Voltage Reference with 25μV/°C Temperature Coefficient, 140μV/V Line Sensitivity and 2,200µm² Area in 180nm  
Longyan Lin, National University of Singapore, Singapore

**CP2.3** A 6.78MHz Wireless Power Transfer System Enabling Perpendicular Wireless Powering with Efficiency Increase from 0.02% to 48.2% by Adaptive Magnetic Field Adder IC Integrating Shared Coupling Coefficient Sensor  
Hao Qiu, University of Tokyo, Japan

**CP3.6** A Domino Bootstrapping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 96% High Efficiency  
Hsuan-Yu Chen, National Chiao Tung University, Taiwan

**JFS3.2** Can We Ever Get to a 100nm Tall Library? Power Rail Design for 1nm Technology Node  
Victor Moroz, Synopsys, USA

**THL.2** GaN and Si Transistors on 300mm Si(111) enabled by 3D Monolithic Heterogeneous Integration  
Han Wui Then, Intel, USA

**TN1.9** GaN PMIC Opportunities: Characterization of Analog and Digital Building Blocks in a 650V GaN-on-Si Platform  
Wan Lin Jiang, University of Toronto, Canada
What is an Executive Session?

**JFS5.5**  
Heterogeneous Power Delivery for 7nm High-Performance Chiplet-Based Processors Using Integrated Passive Device and In-Package Voltage Regulator  
*Alan Roth, TSMC, USA*

**TH1.1**  
Low Temperature SoIC Bonding and Stacking Technology for 12/16-Hi High Bandwidth Memory (HBM)  
*C.H. Tsai, TSMC, Taiwan*

**TH1.3**  
Bumpless Build Cube (BBCube): High-Parallelism, High-Heat-Dissipation and Low-Power Stacked Memory Using Wafer-Level 3D Integration Process

**TH1.5**  
Immersion in Memory Compute (ImMC) Technology  
*C.T. Wang, TSMC, Taiwan*

**TH1.6**  
Low Temperature Cu/SiO₂ Hybrid Bonding with Metal Passivation  
*Demin Liu, National Chiao Tung University, Taiwan*
ED4 Executive Session - Sensors

Session Chairs: Ron Kapusta (Analog Devices), Tomohiro Takahashi (Sony Semiconductor Solutions)

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What is an Executive Session?

**CB1.4**
1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-Chip with Dynamic Incremental-SAR Acquisition
Jun Wang, University of California San Diego, USA

**CB1.5**
High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at 11.72μm Pitch for Neuronal Network Analysis
Yuri Kato, Sony Semiconductor Solutions, Japan

**CB2.1**
A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR
Tuan Thanh Ta, Toshiba, Japan

**CB2.2**
A 36-Channel SPAD-Integrated Scanning LiDAR Sensor with Multi-Event Histogramming TDC and Embedded Interference
Hyongseok Seo, Sungkyunkwan University, Republic of Korea

**CB2.4**
A Low Noise Read-Out IC with Gate Driver for Full Front Display Area Optical Fingerprint Sensors
Yongil Kwon, Samsung Electronics, Republic of Korea

**CB2.5**
An Always-On 4x Compressive VGA CMOS Imager with 51pJ/pixel and >32dB PSNR
Wenda Zhao, The University of Texas at Austin, USA

**CB3.1**
A 50.7dB-DR Finger-Resistance Extractable Multi-Touch Sensor IC Achieving Finger-Classification Accuracy of 97.7% on 6.7-inch Capacitive Touch Screen Panel
Tae-Gyun Song, Korea Advanced Institute of Science and Technology, Republic of Korea

**CB4.3**
A 0.5V, 6.2μW, 0.059mm² Sinusoidal Current Generator IC with 0.088% THD for Bio-Impedance Sensing
Kwantae Kim, Korea Advanced Institute of Science and Technology, Republic of Korea

**CC2.3**
Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting
Massimo Alioto, National University of Singapore, Singapore
EE1 Executive Session - Ultra Low Energy Systems

Session Chairs: Danielle Griffith (Texas Instruments)

What is an Executive Session?

**CF3.2**
**Industrial IoT with Crystal-Free Mote-on-Chip**
Invited
Thomas Watteyne, Inria, France

**CF3.3**
**A Multichannel, MEMS-Less −99dBm 260nW Bit-level Duty Cycled Wakeup Receiver**
Anjana Dissanayake, University of Virginia, USA

**CF3.4**
**CF3.4 - A 4.4μW −92/−90.3dBm Sensitivity Dual-mode BLE/Wi-Fi Wake-Up Receiver**
Po-Han Peter Wang, University of California San Diego, USA

**CF4.1**
**A 8.7ppm/°C, 694nW, One-Point Calibrated RC Oscillator Using a Nonlinearity-Aware Dual Phase-Locked Loop and DSM-Controlled Frequency-Locked Loops**
Giorgio Cristiano, ETH Zürich, Switzerland

**CF4.2**
**A 0.5V 560kHz 18.8fJ/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop**
Daniel Truesdell, University of Virginia, USA

**CF4.3**
**A 0.9pJ/cycle 8ppm/°C DFLL-based Wakeup Timer Enabled by a Time-Domain Trimming and an Embedded Temperature Sensing**
Ming Ding, imec, Netherlands

**CP2.4**
**A 120-330V, Sub-μA, 4-Channel Driver for Microrobotic Actuators with Wireless-Optical Power Delivery and Over 99% Current Efficiency**
Jan Rentmeister, Dartmouth College, USA

**CP3.3**
**An N-Path Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting Achieving 13.9x Power Extraction Improvement**
Loai Salem, University of California, Santa Barbara, USA
EF1 Executive Session - Ferroelectrics

Session Chairs: Suman Datta (University of Notre Dame), Byoung-Hun Lee (Gwangju Institute of Science & Technology)

**Live Event**
June-17 19:00 PDT / June-18 04:00 CET / June-18 11:00 JST (1 hour)

**On-Demand Availability**
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**What is an Executive Session?**

**TF1.1** FeFET Memory Featuring Large Memory Window and Robust Endurance of Long-Pulse Cycling by Interface Engineering  
*Chi-Yu Chan*, National Tsing Hua University, Taiwan

**TF1.2** Re-Examination of $V_{th}$ Window and Reliability in HfO$_2$ FeFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation  
*Reika Ichihara*, Kioxia, Japan

**TF1.3** Hot Electrons as the Dominant Source of Degradation for Sub-5nm HZO FeFETs  
*Ava Tan*, University of California, Berkeley, USA

**TF1.4** A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation  
*Kai Ni*, Rochester Institute of Technology, USA

**TF1.5** Asymmetric Polarization Response of Electrons and Holes in Si FeFETs: Demonstration of Absolute Polarization Hysteresis Loop and Inversion Hole Density Over $2\times10^{13}$ cm$^{-2}$  
*Kasidit Toprasertpong*, University of Tokyo, Japan

**TF2.1** SoC Compatible 1T1C FeRAM Memory Array Based on Ferroelectric Hf$_{0.5}$Zr$_{0.5}$O$_2$  
*Jun Okuno*, Sony Semiconductor Solutions, Japan

**TF2.3** Improved State Stability of HfO$_2$ Ferroelectric Tunnel Junction by Template-Induced Crystallization and Remote Scavenging for Efficient In-Memory Reinforcement Learning  
*Shosuke Fujii*, Kioxia, Japan

**TF2.5** Fast Thermal Quenching on the Ferroelectric AI: HfO$_2$ Thin Film with Record Polarization Density and Flash Memory Application  
*Changhwan Choi*, Hanyang University, Republic of Korea

**TF2.6** Multi-Probe Characterization of Ferroelectric/Dielectric Interface by C-V, P-V and Conductance Methods  
*Junkang Li*, Purdue University, USA

**TF2.8** Atomic-Scale Imaging of Polarization Switching in an (Anti-)Ferroelectric Memory Material: Zirconia (ZrO$_2$)  
*Sarah Lombardo*, MSE, Georgia Institute of Technology, USA
## EF2 Executive Session - Advances in Clocking and Data Converters

Session Chairs: Stacy Ho (MediaTek), Kenichi Okada (Tokyo Institute of Technology)

### Live Event
- June-17 19:00 PDT / June-18 04:00 CET / June-18 11:00 JST (1 hour)

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### What is an Executive Session?

#### CD1.3
- An 8b 1GS/s 2.55mW SAR-Flash ADC with Complementary Dynamic Amplifiers
  - **Dong-Ryeol Oh**, Korea Advanced Institute of Science and Technology, Republic of Korea

#### CD1.4
- A 177mW 10GS/s NRZ DAC with Switching-Glitch Compensation Achieving > 64dBc SFDR and < -77dBc IM3
  - **Hung-Yi Huang**, National Cheng Kung University, Taiwan

#### CD2.2
- A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved Second-Order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm
  - **Dongyang Jiang**, University of Macau, China

#### CD2.3
- A 10.4mW 50MHz-BW 80dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp
  - **Kai Xing**, University of Macau, China

#### CD2.5
- A SAR ADC with Reduced kT/C Noise by Decoupling Noise PSD and BW
  - **Zhelu Li**, Zhejiang University, China, University of Texas at Austin, USA

#### CF1.1
- Embedded PLL Phase Noise Measurement Based on a PFD/CP MASH 1-1-1 ΔΣ Time-to-Digital Converter in 7nm CMOS
  - **Mao-Hsuan Chou**, TSMC, Taiwan

#### CF1.3
- A 4GHz 0.73ps\(^{rms}\)-Integrated-Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring PLL with a Jitter-Tracking DLL-Assisted DTC
  - **Jaehong Jung**, Samsung Electronics, Republic of Korea

#### CF1.5
- A 3.2-to-3.8GHz Calibration-Free Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving −66dBc Worst-Case In-Band Fractional Spur
  - **Masaru Osada**, University of Tokyo, Japan

#### CW1.3
- A 4-to-18GHz Active Poly Phase Filter Quadrature Clock Generator with Phase Error Correction in 5nm CMOS
  - **Wei-Chih Chen**, TSMC, Taiwan
What is an Executive Session?

**JFS1.5**  
O-Band GeSi Quantum-Confined Stark Effect Electro-Absorption Modulator Integrated in a 220nm Silicon Photonics  
*Clement Porret, imec, Belgium*

**TH1.2**  
3D Heterogeneous Package Integration of Air/Magnetic Core Inductor: 89%-Efficiency Buck Converter with Backside Power Delivery Network  
*Xiao Sun, imec, Belgium*

**TH1.4**  
TH1.4 - ExaNoDe: Combined Integration of Chiplets on Active Interposer with Bare Dice in a Multi-Chip-Module for Heterogeneous and Scalable High Performance Compute Nodes  
*Pierre-Yves Martinez, Université Grenoble Alpes, CEA-LIST, France*

**TH2.1**  
BEOL Compatible Dual-Gate Ultra Thin-Body W-Doped Indium-Oxide Transistor with $I_{on}=370\mu A/\mu m$, $SS=73mV/dec$ and $I_{on}/I_{off}$ ratio > $4x10^9$  
*Wriddhi Chakraborty, University of Notre Dame, USA*

**TH3.1**  
First Monolithic Integration of 3D Complementary FET (CFET) on 300mm Wafers  
*Cujith Subramanian, imec, Belgium*

**TH3.2**  
3D Sequential Low Temperature Top Tier Devices Using Dopant Activation with Excimer Laser Anneal and Strained Silicon as Performance Boosters  
*Anne Vandoren, imec, Belgium*

**TH3.3**  
28nm FDSOI CMOS Technology (FEOL and BEOL) Thermal Stability for 3D Sequential Integration: Yield and Reliability Analysis  
*Camila Cavalcante, CEA-Leti, France*
EG2 Executive Session - Robust Computing

Session Chairs: Carlos Tokunaga (Intel)

| Live Event       | June-18 08:00 PDT / June-18 17:00 CET / June-19 00:00 JST (1 hour) |
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What is an Executive Session?

**CC1.1** A Performance-Flexible Energy-Optimized Automotive-Grade Cortex-R4F SoC through combined AVS/ABB/Bias-in-Memory-Array Closed-Loop Regulation in 28nm FD-SOI
Ricardo Gomez Gomez, STMicroelectronics, France

**CC1.2** A SCA-Resistant AES Engine in 14nm CMOS with Time/Frequency-Domain Leakage Suppression Using Non-linear Digital LDO Cascaded with Arithmetic Countermeasures
Raghavan Kumar, Intel, USA

**CC1.3** A 0.26% BER, $10^{28}$ Challenge-Response Machine-Learning Resistant Strong-PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection
Vikram Suresh, Intel, USA

**CC1.4** A 435MHz, 2.5Mbps/W Side-Channel-Attack Resistant Crypto-Processor for Secure RSA-4K Public-Key Encryption in 14nm CMOS
Raghavan Kumar, Intel, USA

**CC2.1** A Proactive Voltage-Droop-Mitigation System in a 7nm Hexagon™ Processor
Vijay Kiran Kalyanam, Qualcomm Technologies, USA

**CC2.4** UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in Designs with Large Clock Distribution Delays in 65nm CMOS
Xun Sun, University of Washington, USA

**CC2.5** Low-Clock-Power Digital Standard Cell IPs for High-Performance Graphics/AI Processors in 10nm CMOS
Steven Hsu, Intel, USA

**LT** Do You Really Know What Is In Your Computer? Perspectives on Verifiable Supply Chains
Andrew “bunnie” Huang, Singapore
What is an Executive Session?

**CA1.1**  A 3.0 TFLOPS 0.62V Scalable Processor Core for High Compute Utilization AI Training and Inference  
Sae Kyu Lee, IBM T. J. Watson Research Center, USA

**CA1.2**  A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS  
Phil Knag, Intel, USA

**CA1.5**  A 3mm² Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception Using Parallel Gibbs Sampling in 16nm  
Glenn G. Ko, Harvard University, USA

**CA3.3**  A Probabilistic Self-Annealing Compute Fabric based on 560 Hexagonally Coupled Ring Oscillators for Solving Combinatorial Optimization Problems  
Ibrahim Ahmed, University of Minnesota, USA

**JFS4.1**  SOT-MRAM Based Analog in-Memory Computing for DNN Inference  
Jonas Doevenspeck, imec, ESAT-Katholieke Universiteit Leuven, Belgium

**JFS4.3**  An All-Weights-on-Chip DNN Accelerator in 22nm ULL Featuring 24×1 Mb eRRAM  
Zhehong Wang, University of Michigan, USA

**JFS4.5**  A Mixed-Signal Time-Domain Generative Adversarial Network Accelerator with Efficient Subthreshold Time Multiplier and Mixed-signal On-chip Training for Low Power Edge Devices  
Zhengyu Chen, Northwestern University, USA
EG4 Executive Session - Sensing Interfaces and Building Blocks

Session Chairs: Carolina Mora Lopez (imec)

What is an Executive Session?

**CB1.1** A 785nW Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring
Peng Wang, University of Virginia, USA

**CB3.3** A 200μW Eddy Current Displacement Sensor with 6.7nm\textsubscript{rms} Resolution
Matheus Pimenta, Cypress Semiconductor, Ireland

**CB3.4** A 0.72nW, 1Sample/s Fully Integrated pH Sensor with 65.8LSB/pH Sensitivity
Yihan Zhang, Columbia University, USA

**CB3.5** An 8-Element Frequency-Selective Acoustic Beamformer and Bitstream Feature Extractor with 60 Mel-Frequency Energy Features Enabling 95% Speech Recognition Accuracy
Seungjong Lee, University of Michigan, USA

**CB4.1** A −105dB THD 88dB-SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation
Jiannan Huang, University of California San Diego, USA

**CB4.2** A 4.3fJ/conversion-step 6440µm\textsuperscript{2} All-Dynamic Capacitance-to-Digital Converter with Energy-Efficient Charge Reuse
Haoming Xin, Eindhoven University of Technology, Netherlands

**CP1.3** Sample and Average Common-Mode Feedback in a 101nW Acoustic Amplifier
Rohit Rothe, University of Michigan, USA

**JFS5.3** A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-g Measurement Capability and Low Bias Instability
Xiaoliang Li, Carnegie Mellon University, USA
EG5 Executive Session -
Devices and Circuits for Advanced Communications

Session Chairs: Kamel Benaissa (Texas Instruments)

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**CF2.5** 315GHz Self-Synchronizing Minimum Shift Keying Receiver in 65nm CMOS

*Ibukun Momson,* University of Texas at Dallas, USA

**CW1.1** A 4x112 Gb/s ADC-DSP Based Multistandard Receiver in 7nm FinFET

*Haidang Lin,* Rambus, USA

**CW1.2** A 25-50Gb/s 2.22pJ/b NRZ RX with Dual-Bank and 3-tap Speculative DFE for Microprocessor Application in 7nm FinFET

*Yang You,* IBM, USA

**CW2.3** Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20GS/s 5b ENOB Analog-to-Digital Converter and 5GHz Phase Interpolator

*Sung-Jin Kim,* Stanford University, USA

**CW2.4** A 28mW 32Gb/s/pin 16-QAM Single-Ended Transceiver for High-Speed Memory Interface

*Jieqiong Du,* University of California Los Angeles, USA

**JFS2.1** Hardware-Software Co-integration for Configurable 5G mmWave Systems

*Alberto Valdes-Garcia,* IBM, USA

**JFS2.2** Beyond 5G & Technologies: A Cross-Domain Vision

*Eric Mercier,* Université Grenoble Alps, CEA-Leti, France

**JFS2.5** FinFET with Contact Over Active-Gate for 5G Ultra-Wideband Applications

*Ali Razavi,* GlobalFoundries, USA
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Session Chairs: Shimeng Yu (Georgia Institute of Technology), Hang-Ting Lue (Macronix International)

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- **What is an Executive Session?**

- **CM2.2**
  Dual-Port Field-Free SOT-MRAM Achieving 90MHz Read and 60MHz Write Operations Under 55nm CMOS Technology and 1.2V Supply Voltage
  
  *Masanori Natsui*, Tohoku University, Japan

- **JFS4.2**
  Compact Probabilistic Poisson Neuron Based on Back-Hopping Oscillation in STT-MRAM for All-Spin Deep Spiking Neural Network
  
  *Ming-Hung Wu*, National Chiao Tung University, Taiwan

- **TM3.1**
  Scalability of Quad Interface p-MTJ for 1X nm STT-MRAM with 10ns Low Power Write Operation, 10 years Retention and Endurance > 10^{11}
  
  *Sadahiko Miura*, Tohoku University, Japan

- **TM3.2**
  Reliability Demonstration of Reflow Qualified 22nm STT-MRAM for Embedded Memory Applications
  
  *Chia-Yu Wang*, TSMC, Taiwan

- **TM3.3**
  Fast Switching of STT-MRAM to Realize High Speed Applications
  
  *Tae Young Lee*, GlobalFoundries, Singapore

- **TM3.4**
  A Reliable TDDB Lifetime Projection Model Verified Using 40Mb STT-MRAM Macro at Sub-ppm Failure Rate to Realize Unlimited Endurance for Cache Applications
  
  *Vinayak Bharat Naik*, GlobalFoundries, Singapore

- **TMFS.1**
  Recent Progresses in STT-MRAM and SOT-MRAM for Next Generation MRAM
  
  *Tetsuo Endoh*, Tohoku University, Japan

- **TMFS.3**
  CMOS Compatible Process Integration of SOT-MRAM with Heavy-Metal Bi-Layer Bottom Electrode and 10ns Field-Free SOT Switching with STT Assist
  
  *Noriyuki Sato*, Intel, USA

- **TMFS.4**
  Deterministic and Field-Free Voltage-Controlled MRAM for High Performance and Low Power Applications
  
  *Yueh Chang Wu*, imec, Belgium
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**CF2.1**
A 29% PAE 1.5bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked PLL  
Yuncheng Zhang, Tokyo Institute of Technology, Japan

**CF2.2**
A 28GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation  
Jian Pang, Tokyo Institute of Technology, Japan

**CF2.3**
A 293/440 GHz Push-Push Double Feedback Oscillators with 5.0/-3.9dBm Output Power and 2.9/0.6% DC-to-RF Efficiency in 65nm CMOS  
Dzuhri Radityo Utomo, Korea Advanced Institute of Science and Technology, Republic of Korea

**CF2.4**
A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-Gmax Gain Boosting Technique  
Dae-Woong Park, imec, Republic of Korea

**CW2.1**
A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ Calibration for Memory Interfaces  
Yong-Un Jeong, Seoul National University, Republic of Korea

**CW2.2**
A 0.1pJ/b/dB 28Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler  
Moon-Chul Choi, Seoul National University, Republic of Korea

**JFS2.3**
A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring 7nm EUV Process Technology  
Minjung Jin, Samsung Electronics, Republic of Korea

**JFS2.4**
Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture  
Chen Sun, National University of Singapore, Singapore

**JFS2.6**
An RF Transceiver with Full Digital Interface Supporting 5G New Radio FR1 with 3.84Gbps DL/1.92Gbps UL and Dual-Band GNSS in 14nm FinFET CMOS  
Sangwook Han, Samsung Electronics, Republic of Korea

**JFS2.7**
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Chen-Chien Kao, National Taiwan University, Taiwan
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Session Chairs: Peide Ye (Purdue University), Masaharu Kobayashi (University of Tokyo)

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*Chien-Ping Wang*, National Tsing Hua University, Taiwan

**TN1.2** Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry  
*Chia-Che Chung*, National Taiwan University, Taiwan

**TN1.3** Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFET for Advanced Hardware Security  
*Jianguo Yang*, Institute of Microelectronics of the Chinese Academy of Sciences, China

**TN1.4** A Bias and Correlation-Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking  
*Kai Ni*, Rochester Institute of Technology, USA

**TN1.5** 1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy  
*Xu Bai*, NEC, Japan

**TN1.6** Proposal and Experimental Demonstration of Reservoir Computing Using Hf$_{0.5}$Zr$_{0.5}$O$_2$/Si FeFETs for Neuromorphic Applications  
*Eishin Nako*, University of Tokyo, Japan

**TN1.7** High On-Current 2D nFET of 390μA/μm at $V_{DS} = 1$V using Monolayer CVD MoS$_2$ without Intentional Doping  
*Ang-Sheng Chou*, TSMC, Taiwan

**TN1.8** Ultrahigh Responsivity and Tunable Photogain BEOL Compatible MoS$_2$ Phototransistor Array for Monolithic 3D Image Sensor with Block-Level Sensing Circuits  
*Chih-Chao Yang*, Taiwan Semiconductor Research Institute, Taiwan
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Zheng Guo, Intel, USA

CM1.2  A 29.2Mb/mm² Ultra High Density SRAM Macro Using 7nm FinFET Technology with Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit  
Yoshisato Yokoyama, Renesas Electronics, Japan

CM1.3  Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1R1W 8T-bitcell SRAM in 10nm FinFET CMOS  
Jaydeep Kulkarni, Intel, USA

CM1.5  A 7nm Fin-FET 4.04-Mb/mm² TCAM with Improved Electromigration Reliability Using Far-Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier  
Makoto Yabuuchi, Renesas Electronics, Japan

CM2.3  A 28nm 1.5Mb Embedded 1T2R RRAM with 14.8 Mb/mm² Using Sneaking Current Suppression and Compensation Techniques  
Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China

CM2.4  A 22nm 96Kx144 RRAM Macro with a Self-Tracking Reference and a Low Ripple Charge Pump to Achieve a Configurable Read Window and a Wide Operating Voltage Range  
Chung-Cheng Chou, TSMC, Taiwan

CM3.1  A 28nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation  
Hoyoung Shin, Samsung Electronics, Republic of Korea

JFS5.2  A 1.8Gb/s/pin 16Tb NAND Flash Memory Multi-Chip Package with F-Chip of Toggle 4.0 Specification for High Performance and High Capacity Storage Systems  
Daehoon Na, Samsung Electronics, Republic of Korea
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<td>TC1.1 Enabling Multiple-Vt Device Scaling for CMOS Technology Beyond 7nm Node</td>
<td>Vincent Chang, TSMC, Taiwan</td>
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<td>TC2.1 Surface Ga-boosted Boron-doped Si$<em>{0.5}$Ge$</em>{0.5}$ using In-situ CVD Epitaxy: Achieving 1.1 x 10$^{21}$ cm$^{-3}$ Active Doping Concentration and 5.7 x 10$^{-9}$ Ω-cm$^2$ Contact Resistivity</td>
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<td>Jishen Zhang, National University of Singapore, Singapore</td>
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<td>Jie Deng, Qualcomm Technologies, USA</td>
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# EH6 Executive Session - Si Photonics and DTCO

**Session Chairs:** Ted Letavic (GlobalFoundries), Mitsura Takenaka (University of Tokyo)

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**JFS1.1** TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s Optical I/O  
*Invited*  
Chen Sun, Ayar Labs, USA

**JFS1.2** High-Temperature Operation of Chip-Scale Silicon-Photonic Transceiver  
*Invited*  
Daisuke Okamoto, PETRA, Japan

**JFS1.3** A Monolithically Integrated Silicon Photonics 8x8 Switch in 90nm SOI CMOS  
Jonathan Proesel, IBM T. J. Watson Research Center, USA

**JFS1.4** III/V-on-Bulk-Si Technology for Commercially Viable Photonics-Integrated VLSI  
Dongjae Shin, Samsung Advanced Institute of Technology, Republic of Korea

**JFS3.1** Heterogeneous System-Level Package Integration – Trends and Challenges  
*Invited*  
Frank Lee, TSMC, Taiwan

**THL.3** An Optically Sampled ADC in 3D Integrated Silicon-Photonics/65nm CMOS  
Nandish Mehta, University of California, Berkeley, USA
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**Chair**

H.S. Philip Wong  
Stanford University

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# JSAP Executive Committee

**Chair**

Tadahiro Kuroda  
The University of Tokyo

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# VLSI Symposia 2020

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### Circuits

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