Welcome to the VLSI Symposia 2020
40th Anniversary

The 2020 Symposia on VLSI Technology & Circuits celebrates its 40th year with a virtual conference and the central theme of “The Next 40 Years of VLSI for Ubiquitous Intelligence.” This week-long virtual conference features a fully overlapped program pushing the state-of-the-art in Technology and Circuits, packed with more than 200 contributed technical presentations, technology and circuit demonstrations, 3 short courses, our “Friday” Forum and a “Luncheon” talk that will be offered on-demand in the conference website.

In addition to the on-demand sessions, the VLSI Symposia on Technology and Circuits will also feature an exciting program of live events, as summarized below. This includes 2 plenary sessions, 4 panel discussions, 3 workshops, and 25 Executive Sessions. The goal of Executive Sessions in the VLSI Symposia is to foster a discussion about the current state and future of the field. They will include 2-minute summaries of relevant papers that have been presented at VLSI Symposia 2020 on the topic, along with 35 minutes of discussion among the authors and session chairs on key challenges and opportunities. All conference participants are encouraged to join these meetings and contribute with insight and questions.

Thank you for your support of the Symposia, especially during this unprecedented pandemic time. We hope you enjoy the Symposia and wish you and your loved ones continued good health.
Overview of On-Demand Content

On-Demand Technology, Circuits, and Joint Sessions are similar to typical paper sessions at previous Symposia on VLSI Technology and Circuits. The 2-page paper abstracts, presentation slides, and 20-minute video presentations are provided for your convenience “on-demand” anytime between June 14 (starting at 9:00am PDT) and June 27 (ending at 11:59pm PDT). Early on-demand access for short courses and the forum begins on June 8 at 9:00am PDT.

While viewing a recorded presentation, you can ask questions by typing them in the "Q&A box", stating first the paper number and then your question. Your question will be directed to the session chairs and authors to respond.

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<td>FF Tech/Circuits for Edge Intelligence</td>
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<td>TF2 Ferroelectric Memory &amp; Caps</td>
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<td>June-19 to June-27</td>
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# Overview of Live Content

All live events (except Young Professionals event) will be available for on-demand access the day after event until June-27

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<td>P4 SSCS/EDS Diversity Panel: Cultivating Engineering Confidence in COVID-19 Times</td>
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<td>PFF Forum E-Pitch &amp; Q/A</td>
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<td>EG2 Robust Computing</td>
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<td>EG3 AI/ML</td>
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<td>10:00</td>
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<td>EG4 Sensing Interfaces &amp; Building Blocks</td>
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<td>11:00</td>
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<td>EG5 Devices &amp; Circuits for Adv Comm</td>
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<td>12:00</td>
<td>23:00</td>
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<td>EDS/SSCS Young Professionals Event</td>
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PDT: Pacific Daylight Time (e.g., Los Angeles)
CET: Central European Time (e.g., Netherlands)
JST: Japan Standard Time (e.g., Japan, South Korea)

**What is an Executive Session?**

**Moderated Panels**

**Executive Sessions**

**Traditional Sessions**

**Workshop Panel**

**Webex**

**Monday June-15**
- PL1 Joint Plenary 1
- EA1 Advanced CMOS (1)
- EA2 Sensor Systems
- EC1 Memory (2)
- EC2 Analog Building Blocks
- EC3 Adaptive Systems
- PWS1 Technology & Circuits for ML Workshop
- ED1 Heterogeneous Integration (1)
- ED2 Power

**Tuesday June-16**
- P4 SSCS/EDS Diversity Panel: Cultivating Engineering Confidence in COVID-19 Times
- P1 Technology Panel
- P3 Circuits Panel
- PWS2 Metrology Workshop
- EF1 Ferroelectrics
- EF2 Adv Clocking & Data Converters

**Wednesday June-17**
- PL2 Joint Plenary 2
- PWS3 Quantum Computing Workshop
- EF3 Ultra Low Energy Systems
- PWS4 Young Professionals Event

**Thursday June-18**
- PL2 Joint Plenary 2
- EG1 Heterogeneous Integration (2)
- EG2 Robust Computing
- EG3 AI/ML
- EG4 Sensing Interfaces & Building Blocks
- EG5 Devices & Circuits for Adv Comm
- EDS/SSCS Young Professionals Event

**Overview of Live Content**

- **Traditional Sessions**
  - Executive Sessions
  - Moderated Panels

- **What is an Executive Session?**

- **Webex**
NEW!!! What is an Executive Session?

This year’s Virtual Symposia introduces new live Executive Sessions to foster live discussions and complement the On-Demand Sessions. The Executive Sessions feature 2-minute summaries of papers assigned to each executive session, along with 35 minutes of discussion among the authors and session chairs on key challenges and opportunities. All conference participants are encouraged to join these meetings and contribute with insights and questions.

There are a total of 25 live 50-minute executive sessions. Every On-Demand Technology, Circuits, and Joint Session paper as well as the Luncheon Talk is assigned to one Executive Session. Papers from each on-demand session may be mapped to several executive sessions.

Example mapping:
VLSI Symposia 2020 - Virtual Program

SC1 Technology Short Course - Future of Scaling for Logic and Memory

SC1.1 - Nanosheet Transistor as a Replacement of FinFET for Future Nodes: Device Advantages & Specific Process Elements
Nicolas Loubet, IBM, USA

SC1.2 - On-Die Interconnect Challenges and Opportunities for Future Technology Nodes
Mauro Kobrinsky, Intel, USA

SC1.3 - Challenges and Prospects of Memory Scaling
Gwan-Hyeb Koh, Samsung Electronics, Republic of Korea

SC1.4 - Ferroelectric Hafnium Oxide: From Memory to Emerging Applications
Uwe Schroeder, NaMLab gGmbH, Germany

SC1.5 - EUV Lithography and Its Application to Logic and Memory Devices
Anthony Yan, ASML, USA

SC1.6 - Emerging Technologies for TSV-free Monolithic 3DIC
Chang-Hong Shen, Taiwan Semiconductor Research Institute, Taiwan

SC1.7 - In situ BEOL Transistors and Oxide Electronics
Suman Datta, University of Notre Dame, USA

SC1.8 - Layer Transfer Technology for Heterogeneous Material Integration
Tatsuro Maeda, National Institute of Advanced Industrial Science and Technology, Japan

SC2 Joint Short Course - Heterogeneous Integration – To Boldly Go Where No Moore Has Gone Before

Session Chairs: Alvin Loke (TSMC), Vijay Narayanan (IBM), Kazuhiro Endo (AIST), Makoto Nagata (Kobe University)

SC2.1 - Chiplet Meets the Real World: Benefits and Limits of Chiplet Designs
Samuel Naffziger, AMD, USA

SC2.2 - Heterogeneous System Partitioning and the 3D Interconnect Technology Landscape
Eric Beyne, imec, Belgium

SC2.3 - Back-End Based Chiplet Integration Solutions & Roadmap
Key Chung, SPIL R&D, Taiwan

SC2.4 - Heterogeneous Integration for AI Architectures
Avind Kumar & Mukta Farooq, IBM Research, USA

SC2.5 - Heterogeneous Integration of Chiplets for Sensors
Marco Del Sarto, STMicroelectronics, Italy

SC2.6 - Chiplet-to-Chiplet Communication Circuits for 2.5D/3D Integration Technologies
Kenny C.H. Hsieh, TSMC, Taiwan

SC2.7 - Performance-Driven Design Methodology and Tools for 2.5D/3D Multi-Die Integration
Rajesh Gupta, Synopsys, USA

SC2.8 - Generic Design Strategies and Considerations for 2.5D and 3D Stacked IC Designs
Ki Chul Chun, Samsung Electronics, Republic of Korea

SC3 Circuits Short Course - Trends and Advancements in Circuit Design

Session Chairs: Xin Zhang (IBM), Minkyu Je (KAIST)

SC3.1 - Topologies and Design Techniques of Switched-Capacitor Converters
Wing-Hung Ki, Hong Kong University of Science and Technology, China

SC3.2 - The Noise-Shaping SAR ADC Technique: The Best of Both Worlds
Michael Flynn, University of Michigan, USA

SC3.3 - Next-Generation Readout of Resistor-Based Sensors
Kolf Makinwa, Delft University of Technology, Netherlands

SC3.4 - Time Reference and Frequency Generation
Jae-Yoon Sim, POSTECH, Republic of Korea

SC3.5 - Low-Power and Digitally-Intensive RF Transceiver Design for IoT Applications
Yao-Hong Liu, imec, Netherlands

SC3.6 - Advances and Trends in High-Speed Serial Links for High-Density IO Applications
Mounir Meghelli, IBM, USA

SC3.7 - Adaptive Circuit & System Design Techniques
Thomas Burd, AMD, USA

SC3.8 - Trends and Design Considerations for Emerging Memories and In-Memory Computing
Yih Wang, TSMC, Taiwan

FF - "Friday" Forum

Session Chairs: Kamel Benaissa (Texas Instruments), Ron Kapusta (Analog Devices), Kazuuki Tomoda (Sony Semiconductor Solutions), Kouichi Kanda (Fujitsu Laboratories)

FF.1 - Edge Intelligence – Technologies, Circuits, Architectures
Ali Keshavarzi, Stanford University, USA

FF.2 - Intelligent Edge – It’s Not Just Technology, It’s About Responsible Society
Gowri Chindalore, NXP Semiconductors, USA

FF.3 - Heterogeneous Integration Technology Trends at the Edge
Chih Hang Tung, TSMC, Taiwan

FF.4 - Self Powered SOCs for the Intelligent Edge
Benton Calhoun, University of Virginia, USA

FF.5 - CMOS and Beyond CMOS Technologies for Edge Intelligence
Myung Hee Na, imec, Belgium

FF.6 - Low Power Wireless Networking for the Edge
Thomas Watteyne, Analog Devices, USA

FF.7 - Smart Vision Sensor
Hayato Wakabayashi, Sony Semiconductor Solutions, Japan

FF.8 - Efficient Machine Learning at the Edge
David Blaauw, University of Michigan, USA

FF.9 - Security in Edge Devices
Hannes Tschofenig, Arm, USA

Luncheon Talk

Session Chair: Brian Ginsburg (Texas Instruments)

Do You Really Know What Is In Your Computer? Perspectives on Verifiable Supply Chains
Andrew "bunnie" Huang, Singapore

Panel

P2 Joint Panel - 40 Years of VLSI to Enable the Future of Computing

Organizers: Igor Arsovski (Marvell), Greg Yeric (Arm), Ted Letavic (GlobalFoundries), Munehiro Tada (NEC)
Moderator: Stephen Kossoney, AMD, USA

Asad Abidi, University of California, Los Angeles, USA
Tao-Jae King Liu, University of California, Berkeley, USA
Akira Matsuzawa, Tokyo Institute of Technology, Japan
Charlie Sodini, Massachusetts Institute of Technology, USA
Naveen Verma, Princeton University, USA

Plenary Sessions

PL1 - Plenary 1

Session Chairs: Brian Ginsburg (Texas Instruments), Katsura Miyashita (Toshiba)

PL1.1 (Plenary) - Silicon is Greener: Why Innovation in Circuits is Needed for Sustainability
Jennifer Lloyd, Analog Devices, USA

PL1.2 (Plenary) - 5G Evolution and 6G
Takehiro Nakamura, NTT Docomo, Japan

PL2 - Plenary 2

Session Chairs: Tomas Palacios (MIT), Yusuke Oike (Sony Semiconductor Solutions)

PL2.1 (Plenary) - The Future of Compute: How the Data Transformation is Reshaping VLSI
Michael Mayberry, Intel, USA

PL2.2 (Plenary) - Empowering Next-Generation Applications through FLASH Innovation
Shigeo (Jeff) Ohshima, Kioxia, Japan
## Joint Focus Sessions

### JFS1 - Silicon Photonics

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<td>JFS1.1</td>
<td>(Invited) - TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s Optical I/O</td>
<td>Chen Sun, Ayar Labs, USA</td>
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<tr>
<td>JFS1.2</td>
<td>(Invited) - High-Temperature Operation of Chip-Scale Silicon-Photonic Transceiver</td>
<td>Daisuke Okamoto, PETRA, Japan</td>
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<td>JFS1.3</td>
<td>A Monolithically Integrated Silicon Photonics 8x8 Switch in 90nm SOI CMOS</td>
<td>Jonathan Proesel, IBM T. J. Watson Research Center, USA</td>
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<td>JFS1.4</td>
<td>III-V-on-Bulk Si Technology for Commercially Viable Photonics-Integrated VLSI</td>
<td>Dongjae Shin, Samsung Advanced Institute of Technology, Republic of Korea</td>
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<tr>
<td>JFS1.5</td>
<td>O-Band GeSi Quantum-Confined Stark Effect Electro-Absorption Modulator</td>
<td>Clement Porret, imec, Belgium</td>
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### JFS2 - 5G/mm-Wave

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<td>JFS2.1</td>
<td>(Invited) - Hardware-Software Co-integration for Configurable 5G mmWave Systems</td>
<td>Alberto Valdes-Garcia, IBM, USA</td>
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<td>JFS2.2</td>
<td>(Invited) - Beyond 5G &amp; Technologies : A Cross-Domain Vision</td>
<td>Eric Mercier, Université Grenoble Alpes, CEA-Leti, France</td>
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<td>JFS2.3</td>
<td>A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring 7nm EUV Process Technology</td>
<td>Minjung Jin, Samsung Electronics, Republic of Korea</td>
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<td>JFS2.4</td>
<td>Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture</td>
<td>Chen Sun, National University of Singapore, Singapore</td>
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<td>JFS2.5</td>
<td>FinFET with Contact Over Active-Gate for 5G Ultra-Wideband Applications</td>
<td>Ali Razavi, GlobalFoundries, USA</td>
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<td>JFS2.6</td>
<td>An RF Transceiver with Full Digital Interface Supporting 5G New Radio FRT with 3.84Gbps DL/1.92Gbps UL and Dual-Band GNSS in 14nm FinFET CMOS</td>
<td>Sangwook Han, Samsung Electronics, Republic of Korea</td>
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<td>JFS2.7</td>
<td>A 1.96Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems</td>
<td>Chen-Chien Kao, National Taiwan University, Taiwan</td>
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### JFS3 - STCO/DTCO

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<td>(Invited) - Heterogeneous System-Level Package Integration – Trends and Challenges</td>
<td>Frank Lee, TSMC, Taiwan</td>
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<td>JFS3.2</td>
<td>(Invited) - Can We Ever Get to a 100nm Tall Library? Power Rail Design for 1nm Technology Node</td>
<td>Victor Moroz, Synopsys, USA</td>
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<td>JFS3.3</td>
<td>Bursed Powered SRAM DTCO and System-Level Benchmarking in N3</td>
<td>Shafrir Salahuddin, imec, Belgium</td>
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<td>JFS3.4</td>
<td>Local Variation-Aware Transistor Design through Comprehensive Analysis of Various Vdd/Temperatures Using Sub-7nm Advanced FinFET Technology</td>
<td>Soyoun Kim, Samsung Electronics, Republic of Korea</td>
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### JFS4 - Devices and Circuits for AI/ML

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<td>JFS4.1</td>
<td>SOT-MRAM Based Analog In-Memory Computing for DNN Inference</td>
<td>Jonas Doevenespeck, imec, ESAT-Katholieke Universiteit Leuven, Belgium</td>
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<td>JFS4.2</td>
<td>Compact Probabilistic Poisson Neuron Based on Back-Hopping Oscillation in STT-MRAM for All-Spin Deep Spiking Neural Network</td>
<td>Ming-Hung Wu, National Chiao Tung University, Taiwan</td>
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<td>JFS4.3</td>
<td>An All-Weights-on-Chip UNN Controller in 22nm ULL Featuring 24x1 Mb eMRAM</td>
<td>Zhehong Wang, University of Michigan, USA</td>
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<td>JFS4.4</td>
<td>PNPU: A 146.52TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping</td>
<td>Sangeyoek Kim, Korea Advanced Institute of Science and Technology, Republic of Korea</td>
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<td>JFS4.5</td>
<td>A Mixed-Signal Time-Domain Generative Adversarial Network Accelerator with Efficient Subthreshold Time Multiplier and Mixed-signal On-chip Training for Low Power Edge</td>
<td>Zhengchu Chen, Northwestern University, USA</td>
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### JFS5 - Heterogeneous Integration

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<td>JFS5.1</td>
<td>Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry, Multi-Tier Complementary Carbon Nanotube Logic and Resistive RAM at a 130 nm Node</td>
<td>Tathagata Srinamit, Massachusetts Institute of Technology, USA</td>
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<td>JFS5.2</td>
<td>A 1.8Gb/s/16b 16T NAND Flash Memory Multi-Chip Package with F-Chip of Toggle</td>
<td>Daehoon Na, Samsung Electronics, Republic of Korea</td>
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<td>JFS5.3</td>
<td>A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-q Measurement Capability and Low Bias Instability</td>
<td>Xiaoliang Li, Carnegie Mellon University, USA</td>
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<td>JFS5.4</td>
<td>A 3D-Stacked Cortex-M0 SoC with 20.3Gbps/mm2 7.1mW/mm2 Simultaneous Wireless Inter-Tier Data and Power Transfer</td>
<td>Benjamin Fletcher, University of Southampton, United Kingdom</td>
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<td>JFS5.5</td>
<td>Heterogeneous Power Delivery for 7nm High-Performance Chiplet-Based Processors Using Integrated Passive Device and In-Package Voltage Regulator</td>
<td>Alan Roth, TSMC, USA</td>
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<td>CB1.4</td>
<td>1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-chip with Dynamic Incremental-SAR Acquisition</td>
<td>Jun Wang, University of California San Diego, USA</td>
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<td>CB1.5</td>
<td>(Invited) - High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at 11.72um Pitch for Neuronal Network Analysis</td>
<td>Yuri Kato, Sony Semiconductor Solutions, Japan</td>
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<td>CB2.1</td>
<td>(Invited) - A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR</td>
<td>Tuan Thanh Ta, Toshiba, Japan</td>
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<td>CB3.4</td>
<td>A 0.72nW, 1T/sample Fully Integrated pH Sensor with 65.6LSb/pH Sensitivity</td>
<td>Yihan Zhang, Columbia University, USA</td>
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<td>CP3.6</td>
<td>A Domain-Bootstrapping 12V GaN Driver for Driving an On-Chip 950V 6GaN Power Switch for 96% High Efficiency</td>
<td>Hsuan-Yu Chen, National Chiao Tung University, Taiwan</td>
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<td>JFS1.4</td>
<td>III-V-on-Bulk Si Technology for Commercially Viable Photonics-Integrated VLSI</td>
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<td>TM2.2</td>
<td>A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing</td>
<td>Weiwei Wan, Stanford University, USA</td>
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<td>TN1.3</td>
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### CA3 - Digital Systems

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<td>CA3.1 (invited) - Managing Chip Design Complexity in the Domain-Specific SoC Era</td>
<td>Yunsup Lee, SiFive, USA</td>
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<td>CA3.2 - 17.3GCUPS Pruning-Based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing</td>
<td>Xiao Wu, University of Michigan, Sequal, USA</td>
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<tr>
<td>CA3.3 - A Probabilistic Self-Annealing Compute Fabric based on 560 Hexagonally Coupled Ring Oscillators for Solving Combinatorial Optimization Problems</td>
<td>Ibrahim Ahmed, University of Minnesota, USA</td>
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<td>CA3.4 - MANA: A Monolithic Adiabatic InIntegration Architecture Microprocessor Using 1.42J/op Superconductor Josephson Junction Devices</td>
<td>Christopher Ayala, Yokohama National University, Japan</td>
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<td>CA3.5 - 32GHz 6.5mW Gate-Level-Useripled 4-bit Processor using Superconductor Single-Flux-Quantum Logic</td>
<td>Koki Ishida, Kyushu University, Japan</td>
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### CB1 - Biomedical Sensors

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<td>CB1.1 - A 785mV Modular (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring</td>
<td>Peng Wang, University of Virginia, USA</td>
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<td>CB1.2 - An Artificial Iris ASIC with High Voltage Liquid Crystal Driver, 10mA Light Range Detector and 40mA Blink Detector for LCD Flicker Removal</td>
<td>Bogdan Raducanu, imec, Belgium</td>
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<td>CB1.3 - A Packaged Ingestible Bio-Pill with 15-Pixel Multiplexed Fluorescence Nucleic-Acid Sensor and Bi-Directional Wireless Interface for In-vivo Bio-Molecular Sensing</td>
<td>Chengjie Zhu, Princeton University, USA</td>
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<td>CB1.4 - 1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-Chip with Dynamic Incremental-SAR Acquisition</td>
<td>Jun Wang, University of California San Diego, USA</td>
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<td>CB1.5 (invited) - High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at 11.72um Pitch for Neurological Network Analysis</td>
<td>Yuri Kato, Sony Semiconductor Solutions, Japan</td>
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### CB2 - Image Sensor & Imaging Techniques

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<td>CB2.1 (invited) - A 2D-SPAD Array and Read-Out APE for Next-Generation Solid-State LIDAR</td>
<td>Tran Thanh Ta, Toshiba, Japan</td>
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<td>CB2.2 - A 36-Channel SPAD-Integrated Scanning LiDAR Sensor with Multi-Event Histogramming TDC and Embedded Interface Filter</td>
<td>Hyeongseok Seo, Sungkyunkwan University, Republic of Korea</td>
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<td>CB2.3 - A 3.0µW@5fps QVGA Self-Controlled Wake-Up Imager with On-Chip Motion Detection, Auto-Exposure and Object Recognition</td>
<td>Arnaud Verdant, CEA-LET-MINATEC, France</td>
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<td>CB2.4 - A Low Noise Read-Out IC with Gate Driver for Full Front Display Area Optical Fingerprint Sensors</td>
<td>Yongil Kwon, Samsung Electronics, Republic of Korea</td>
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<td>CB2.5 - An Always-On 4x Compressive VGA CMOS Image with 51µ/pixel and &gt;32dB PSNR</td>
<td>Wenda Zhao, The University of Texas at Austin, USA</td>
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### CB3 - Physical Sensors

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<td>CB3.1 - A 50.7dB-DR Finger-Resistance Extractable Multi-Touch Sensor IC Achieving Finger-Classification Accuracy of 97.7% on 6.7-inch Capacitive Touch Screen Panel</td>
<td>Tae-Gyun Song, Korea Advanced Institute of Science and Technology, Republic of Korea</td>
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<td>CB3.2 - A Pressure Sensing System with 20.75mHg (30) Inaccuracy for Battery-Powered Low Power IoT Applications</td>
<td>Seok Hyeon Jeong, University of Michigan, USA</td>
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<td>CB3.3 - A 200µW Eddy Current Displacement Sensor with 6.7nm Resolution</td>
<td>Mathews Pimenta, Cypress Semiconductor, USA</td>
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<td>CB3.4 - A 0.72nW, 1Sample/s Fully Integrated pH Sensor with 65.8LSB/pH Sensitivity</td>
<td>Yihan Kuo, Columbia University, USA</td>
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<td>CB3.5 - An 8-Element Frequency-Sensitive Acoustic Beamformer and Bitstream Feature Extractor with 60 Mel-Frequency Energy Features Enabling 95% Speech Recognition Accuracy</td>
<td>Seungjung Lee, University of Michigan, USA</td>
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### CB4 - Front-Ends for Sensor Interfaces

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<td>CB4.1 - A ~105dB THD 88dB-SNR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation</td>
<td>Jiannan Huang, University of California San Diego, USA</td>
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<td>CB4.2 - A 4.3A/conversion-step 6440µm All-Dynamic Capacitance-to-Digital Converter with Energy-Efficient Charge Reuse</td>
<td>Haoming Xin, Eindhoven University of Technology, Netherlands</td>
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<td>CB4.3 - A 0.5V, 6.2µW, 0.059mm² Sinusoidal Current Generator IC with 0.088% THD for Bio-Impedance Sensing</td>
<td>Kwanta Kim, Korea Advanced Institute of Science and Technology, Republic of Korea</td>
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<td>CB4.4 - A Portable NMR System with 50kHz IF, 10µs Dead Time, and Frequency Tracking</td>
<td>Sungjin Hong, University of Texas at Austin, USA</td>
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CC1 - Circuits for Security and Safety

Session Chairs: Rob Atkin (Arm), Mototsugu Hamada (University of Tokyo)

CC1.1 - A Performance-Flexible Energy-Optimized Automotive-Grade Cortex-R4F SoC through combined AVS/ABB/Bias-in-Memory-Array Closed-Loop Regulation in 28nm FD-SOI
Ricardo Gomez Gomez, STMicroelectronics, France

CC1.2 - A Self-Resilient AES Engine in 14nm CMOS with Time/Frequency-Domain Leakage Suppression Using Non-linear Digital LDO Cascaded with Arithmetic Countermeasures
Raghavan Kumar, Intel, USA

CC1.3 - A 0.26% BER, 10^7 Challenge-Response Machine-Learning Resistant Strong-PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection
Vikram Suresh, Intel, USA

CC1.4 - A 435MHz, 2.5Mbps Side-Channel-Attack Resistant Crypto-Processor for Secure BSA-4k Public-Key Encryption in 14nm CMOS
Raghavan Kumar, Intel, USA

CC2 - Adaptive Clocking and Power Delivery

Session Chairs: Paul Whatmough (Arm), Makoto Takayami (University of Tokyo)

CC2.1 - A Proactive Voltage-Drop-Mitigation System in a 7nm Hexagon™ Processor
Vijay Kiran Kalyanam, Qualcomm Technologies, USA

CC2.2 - An Autonomous Reconfigurable Power Delivery Network (RPDN) for Many-Core SoCs Featuring Dynamic Current Steering
Khondker Ahmed, Intel, USA

CC2.3 - Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting
Massimo Ailoto, National University of Singapore, Singapore

CC2.4 - UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in Designs with Large Clock Distribution Delays in 65nm CMOS
Sun Xun, University of Washington, USA

CC2.5 - Low-Clock-Power Digital Standard Cell IPs for High-Performance Graphics/AI Processors in 10nm CMOS
Steven Hsu, Intel, USA

CD1 - High-Speed Data Converters

Session Chairs: Stacy Ho (MediaTek), Tomohiro Nezuka (MIRI Technologies)

CD1.1 - A 1G/5is to 1G/5is Ringamp-Based Pipelined ADC with Dynamic reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm
Benjamin Hershberg, imec, Belgium

CD1.2 - A 10-bit 100MS/s SAR ADC with Always-on Reference Ripple Cancellation
Xiuuan Tang, University of Texas at Austin, USA

CD1.3 - An 8b 1G/5s 2.55M SAR-Flash ADC with Complementary Dynamic Amplifiers
Dong-Ryeol Oh, Korea Advanced Institute of Science and Technology.

CD1.4 - A 177Mw 1G/5s NRZ DAC with Switching-Glitch Compensation Achieving > 84dBc SFDR and < -77dBc IM3
Hung-Yi Huang, National Cheng Kung University, Taiwan

CD1.5 - A Compact 14G/s 8-bit Switched-Capacitor DAC in 16nm FinFET CMOS
Pietro Caraglio, Stanford University, USA

CD2 - Data Converter Techniques

Session Chairs: Ewout Martens (imec), Mitsuya Fukazawa (Renesas Electronics)

CD2.1 - A 440µW, 109.8dB DR, 106.5dB SNDR Discrete-Time Zoom ADC with a 20kHz BW
Efrain Eland, Deft University of Technology, Netherlands

CD2.2 - A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved Second-Order 2 ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS
Dongyang Jiang, University of Macau, Macao

CD2.3 - A 10.4MHz 50MHz-BW 80dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp
Kai Xing, University of Macau, China

CD2.4 - A 1G/5s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9dB FoMs
Yitian Lyu, MICAS-Katholieke Universiteit Leuven, Belgium

CD2.5 - A SAR ADC with Reduced kT/C Noise by Decoupling Noise PSD and BW
Zhuo Li, Zhejiang University, University of Texas at Austin, China

CF1 - Advanced PLLs

Session Chairs: Christoph Sandner (Infineon), Kenichi Okada (Tokyo Institute of Technology)

CF1.1 - Embedded PLL Phase Noise Measurement Based on a PFD/CP MASH 1-1-1 ΔΣ Time-to-Digital Converter in 7nm CMOS
Mao-Hsuan Chou, TSMC, Taiwan

CF1.2 - A Fast Locking 5.8-7.2GHz Fractional-N Synthesizer with Sub-2µs Settling Time in 22nm FDSOI
Jeffrey Prinzie, Katholieke Universiteit Leuven, Belgium

CF1.3 - A 4GHz 0.73ps_integrated-Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring PLL with a Jitter-Tracking DLL-Assisted DTC
Jaejoong Jung, Samsung Electronics, Republic of Korea

CF1.4 - A 3.3GHz 101f_integrated-Jitter, -250.3dB FOM Fractional-N DPLL with Phase Error Detection Accomplished in Fully Differential Voltage Domain
Lianbo Wu, ETH Zürich, Switzerland

CF1.5 - A 3.2-3.8GHz Calibration-Free Harmonic-Mixed-Based Dual-Frequency Fractional-N PLL Achieving ~66dBc Worst-Case In-Band Fractional Spur
Masaru Osada, University of Tokyo, Japan

CF2 - RF & mm-Wave Circuits

Session Chairs: Mike Chen (University of Southern California), Ho-Jin Song (POSTECH)

CF2.1 - A 29% PAE 1.5bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked PLL
Yuncheng Zhang, Tokyo Institute of Technology, Japan

CF2.2 - A 28GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation
Jian Pang, Tokyo Institute of Technology, Japan

CF2.3 - A 293/2440GHz Push-Push Double Feedback Oscillators with 5.0/-3.8dBm Output Power and 2.9% 6% DC-to-RF Efficiency in 65nm CMOS
Dae-Woong Park, imec, Republic of Korea

CF2.4 - A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-Cascode Technique
Dae-Woong Park, imec, Republic of Korea

CF2.5 - 315GHz Self-Synchronizing Minimum Shift Keying Receiver in 65nm CMOS
Ibukun Momson, University of Texas at Dallas, USA

CF3 - IoT and Wireless Receivers

Session Chairs: Aline Zolfaghari (Broadcom), Chun-Huat Heng (National University of Singapore)

CF3.1 - A 17MOPS-36GOPS Adaptive Versatile IoT Node with 15,000x Peak-to-Idle Power Reduction, 207ns Wake-Up Time and 1.3TOPS/W ML Efficiency
Ivan Miro-Panades, Université Grenoble Alpes, CEA, LIST, France

CF3.2 - (Invited) - Industrial IoT with Crystal-Free Mote-on-Chip
Thomas Watteyne, Inria, France

CF3.3 - A Multi-channel MEMS-Less −99dBm 260GHz Bit-level Duty Cycled Wakeup Receiver
Anjana Disanayake, University of Virginia, USA

CF3.4 - A 4.4µW −92/-90.3dBm Sensitivity Dual-mode BLE/Wi-Fi Wake-Up Receiver
Po-Han Peter Wang, University of California San Diego, USA

CF3.5 - A 920MHz 16-FSK Receiver Achieving a Sensitivity of −103dBm at 0.6mW via an Integrated N-Path Filter Bank
Ali Nikoofard, University of California San Diego, USA

CF4 - Low Power Oscillators

Session Chairs: Danielle Griffith (Texas Instruments), Yoji Bando (Socionext)

CF4.1 - A 8.7ppm/°C, 694nW, One-Point Calibrated RC Oscillator Using a Nonlinearity-Aware Dual-Phase-Locked Loop and DSM-Controlled Frequency-Locked Loops
Giorgio Cristiano, ETH Zürich, Switzerland

CF4.2 - A 0.5V 60kHz 18.8fJ/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 98.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop
Daniel Truesdell, University of Virginia, USA

CF4.3 - A 9.8pJ/cycle 8ppm/°C DFLL-based Wakeup Timer Enabled by a Time-Domain Trimming and an Embedded Temperature Sensing
Ming Ding, imec, Netherlands
CM1 - Advanced SRAM Design
Session Chairs: Igor Arsovski (Marvell), Tsung-Yung Jonathan Chang (TSMC)
CM1.1 - A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 173mV VMIN Reduction with Negligible Power Overhead
Zheng Guo, Intel, USA
CM1.2 - A 29m2/bit Ultra High Density SRAM Macro Using 7nm FinFET Technology with Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit
Yoshisato Yokoyama, Renesas Electronics, Japan
CM1.3 - Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1T1W 8t-bitcell SRAM in 10nm FinFET CMOS
Jaydeep Kulkarni, Intel, USA
CM1.4 - 2X-Bandwidth Burst 8T-SRAM for Memory Bandwidth Limited Workloads
Charles Augustine, Intel, USA
CM1.5 - A 7nm FinFET 4.04-Mb/mm² TCAM with Improved Electromigration Reliability Using Far-Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier
Makoto Yabuuchi, Renesas Electronics, Japan

CM2 - Emerging Memory Design
Session Chairs: Seung Kang (Qualcomm Technologies), Makoto Miyamura (NEC)
CM2.1 - A 14.7m2/mm² 28nm FDSOI STT-MRAM with Current Starved Read Path, 502/1 Sigma Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference
El Mehdi Boujamaa, Arm, France
CM2.2 - Dual-Port Field-Free SST-MRAM Achieving 90Gb/s Read and 60MHz Write Operations Under 55nm CMOS Technology and 1.2V Supply Voltage
Masanori Natsui, Tohoku University, Japan
CM2.3 - A 28nm 1.5Mb Embedded 1T2R SRAM with 14.8Mbit/s Using Snaking Current Suppression and Compensation Techniques
Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China
CM2.4 - A 22nm 98kx144 RRAM Macro with a Self-Tracking Reference and a Low Ripple Charge Pump to Achieve a Configurable Read Window and a Wide Operating Voltage Range
Chung-Cheng Chou, TSMC, Taiwan

CM3 - Energy Efficient Memory Design
Session Chairs: John Wu (AMD), Kyomin Sohn (Samsung Electronics)
CM3.1 - A 28nm 10Gb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation
Hoyoung Shin, Samsung Electronics, Republic of Korea
CM3.2 - A 65nm 16Gb SRAM with 13T5pW Leakage at 0.9V for Wireless IoT Sensor Nodes
Shourya Gupta, University of Virginia, USA
CM3.3 - 1.03pW Ultra-Low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors
Jingcheng Wang, University of Michigan, USA
CM3.4 - Z-PIM: An Energy-Efficient Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision
Ji-Hoon Kim, Korea Advanced Institute of Science and Technology, Republic of Korea

CP1 - Amplifiers
Session Chairs: Hylas Lam (Analog Devices), Kuan-Dar Chen (MediaTek)
CP1.1 - A 107.8dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier
Huanzhang Zhang, Delft University of Technology, Netherlands
CP1.2 - An 80, 1.4W, 0.0024% THD+N Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Mode Achieving Low Standby Quiescent Current of 565µA
Ji-Hun Lee, Korea Advanced Institute of Science and Technology, Republic of Korea
CP1.3 - Sample and Average Common-Mode Feedback in a 101nW Acoustic Amplifier
Rohit Roth, University of Michigan, USA
CP1.4 - A 0.0046mm² 6.7uW Three-Stage Amplifier Capable of Driving 0.5-to-1.9nF Capacitive Load with >0.68MHB GBW without Compensation Zero
Hongseok Shin, Korea Advanced Institute of Science and Technology, Republic of Korea

CP2 - Voltages References and Wireless Power
Session Chairs: Patrick Mercier (California San Diego), Sung-Wan Hong (Sookmyung Women’s University)
CP2.1 - A Single-Term Switched Capacitor CMOS Bandgap Reference with a 3d inaccuracy of ±0.02%, ±0.12% for Battery Monitoring Applications
Jun-Ho Boo, Sogang University, Republic of Korea
CP2.2 - A 0.25-V, 5.3-pW Voltage Reference with 25µV/°C Temperature Coefficient, 140µV/Lp Noise Sensitivity and 2,200µm² Area in 180nm CMOS
Longyan Lin, National University of Singapore, Singapore
CP2.3 - A 6.75Mbit Wireless Power Transfer System Enabling Perpendicular Wireless Powering with Efficiency Increase from 0.02% to 48.2% by Adaptive Magnetic Field Adder IC Integrating Shared Coupling Coefficient Sensor
Hao Gu, University of Tokyo, Japan
CP2.4 - A 120-330V, Sub-µA, 4-Channel Driver for Microbotic Actuators with Wireless-Optical Power Delivery and Over 99% Current Efficiency
Jan Rentmeister, Dartmouth College, USA

CP3 - Power Converters
Session Chairs: Xiao Zhang (IBM), Po-Hung Chen (National Chiao Tung University)
CP3.1 - An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching
Dong Yan, University of Texas at Dallas, USA
CP3.2 - Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 85nm CMOS
Xun Sun, University of Washington, USA
CP3.3 - An N-Path Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting Achieving 13.9x Power Extraction Improvement
Loai Salem, University of California Santa Barbara, USA
CP3.4 - A 4V-0.55V Input Fully Integrated Switched-Capacitor Converter Enabling Dynamic Voltage Domain Stacking and Achieving 80.1% Average Efficiency
Tim Thielemans, MICAS-Katholieke Universiteit Leuven, Belgium
CP3.5 - A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency
Xiaosen Liu, Intel, USA
CP3.6 - A Domino Bootstrapping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 96% High Efficiency
Hsuan-Yu Chen, National Chiao Tung University, Taiwan

CW1 - Ultra-High-Speed Wireline
Session Chairs: Jon Proesel (IBM), Jri Lee (National Taiwan University)
CW1.1 - A 4x112 Gb/s ADC-DSP Based Multistandard Receiver in 7nm FinFET
Haidang Lin, Microsoft, USA
CW1.2 - A 25-50Gb/s 4.22ppb NRZ RX with Dual-Bank and 3-tap Speculative DFE for Microprocessor Application in 7nm FinFET CMOS
Yang You, IBM, USA
CW1.3 - A 4-to-16GHz Active Poly Phase Filter Quadrature Clock Generator with Phase Error Correction in 5nm CMOS
Wei-Chih Chen, TSMC, Taiwan

CW2 - Wireline Techniques
Session Chairs: Parag Upadhyaya (Xilinx), C. Patrick Yue (Hong Kong University of Science and Technology)
CW2.1 - A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ Calibration for Memory Interfaces
Yong-Jn Jeong, Seoul National University, Republic of Korea
CW2.2 - A 0.1pJ/µJ 32Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler
Moon-Chul Choi, Seoul National University, Republic of Korea
CW2.3 - Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20Gb/s 5b ENOB Analog-to-Digital Converter and 5Ghz Phase Interpolator
Sung-Jin Kim, Stanford University, USA
CW2.4 - A 28mW 32Gb/s/pin 16-QAM Single-Ended Transceiver for High-Speed Memory Interface
Jieqiong Du, University of California Los Angeles, USA
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<td>Arindam Mallik (imec), Nadine Collaert (imec)</td>
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<td>Prospects of Analog In-Memory Computing – An Overview</td>
<td>Boris Murmann, Stanford University, USA</td>
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<td>Designing Material Systems and Algorithms for Analog Computing</td>
<td>Robert L. Bruce, IBM Research, USA</td>
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<td>Monolithically Integrated RRAM-based Analog/ Mixed-Signal In-Memory Computing for Energy-Efficient Deep Learning</td>
<td>Jae-Sun Seo, Arizona State University, USA</td>
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<td>Compute-in-Memory Circuit and Device Technologies: Trends and Prospects</td>
<td>Jaydeep Kulkarni, University of Texas at Austin, USA</td>
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<td>WS1.5</td>
<td>Analog Computing for Machine Learning – An Ideal Case for Co-Optimization of System and Device Technology</td>
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<td>System and Architecture Level Considerations in Leveraging Mixed-Signal Techniques for ML at the Edge</td>
<td>Mahesh Mehendale, Texas Instruments, USA</td>
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<td>Know Where You Are Going; Metrology In the New Age of Semiconductor Manufacturing</td>
<td>Tom Larson (Nova Measuring Instruments), Gosia Jurczak (Lam Research)</td>
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<td>Tom Larson, Nova Measuring Instruments, USA</td>
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<td>Manufacturing Process Challenges and Requirements for Metrology in Semiconductor Memory Devices</td>
<td>Keiji Suzuki, Kioxia, Japan</td>
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<td>WS2.3</td>
<td>Metrology with Angstrom Accuracy Required by Logic IC Manufacturing – Challenges From R&amp;D to High Volume Manufacturing and Solutions in the AI Era</td>
<td>Yi Hung Lin, TSMC, Taiwan</td>
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<td>Dimensional Metrology Overview, Trends and Upcoming Challenges</td>
<td>Philippe Leray, imec, Belgium</td>
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<td>Defect Inspection: A Trio of Trends for the 2020s</td>
<td>Mark Shirey, KLA, USA</td>
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<td>WS2.6</td>
<td>Enabling Modern Semiconductor Manufacturing With Materials Metrology</td>
<td>Kavita Shah, Nova Measuring Instruments, USA</td>
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<td>Opportunities and Challenges for Lab-based Characterization for Emerging Technologies</td>
<td>Markus Kuhn, Intel, USA</td>
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<td>Quantum Computers for Electrical Engineers</td>
<td>Maud Vinet (CEA-Leti), Iuliana Radu (imec)</td>
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<td>3D Integration and Challenges for Scaling</td>
<td>William Oliver, Massachusetts Institute of Technology, USA</td>
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<td>WS3.2</td>
<td>Superconducting Qubits: How Technology/ Processing/ Materials Impact Coherence Time and How Design Impacts Gate Fidelity</td>
<td>Doug McClure, IBM, USA</td>
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<td>Si Based Qubits: Technology and Material Impact on Performance</td>
<td>Iuliana Radu, imec, Belgium</td>
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<td>WS3.4</td>
<td>Architectures Challenges for Si Spin Qubits</td>
<td>Maud Vinet, CEA-Leti, France</td>
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<td>WS3.5</td>
<td>Cryogenic CMOS for Control of Transmon Qubits</td>
<td>Joseph Bardin, Google AI Quantum &amp; University of Massachusetts Amherst, USA</td>
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### EB2 Executive Session - Intelligent Computing

**June-15 19:00 PDT / June-16 04:00 CET / June-16 11:00 JST (1 hour)**

**Session Chairs:** Zhengya Zhang (University of Michigan), Vinayak Honkote (Intel)

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<td>An Ultra-Low Latency 7.8-13.6 pJ/b Reconfigurable Neural Network-Assisted Polar Decoder with Multi-Code Length Support</td>
<td>Chieh-Fang Teng, National Taiwan University, Taiwan</td>
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<td>CA1.4</td>
<td>A 4.45mA Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices</td>
<td>Dongseok Im, Korea Advanced Institute of Science and Technology, Republic of Korea</td>
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<td>A 1200x1200 8-Edges/Vertex FPGA-Based Motion-Planning Accelerator for Dual-Arm-Robot Manipulation Systems</td>
<td>Takashi Oshima, Hitachi, Japan</td>
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<td>CA3.1 (Invited)</td>
<td>Managing Chip Design Complexity in the Domain-Specific SoC Era</td>
<td>Yunsup Lee, SiFive, USA</td>
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<td>CA3.4</td>
<td>MANA: A Monolithic Adiabatic Integration Architecture Microprocessor Using 1.4zJ/op Superconductor Josephson Junction Devices</td>
<td>Christopher Ayala, Yokohama National University, Japan</td>
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<td>32GHz 6.5mW Gate-Level-Pipelined 4-bit Processor using Superconductor Single-Flux-Quantum Logic</td>
<td>Koki Ishida, Kyushu University, Japan</td>
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<td>CM3.4</td>
<td>Z-PIM: An Energy-Efficient Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision</td>
<td>Ji-Hoon Kim, Korea Advanced Institute of Science and Technology, Republic of Korea</td>
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<td>JF3.4</td>
<td>PNPU: A 146.52TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping</td>
<td>Sangyeob Kim, Korea Advanced Institute of Science and Technology, Republic of Korea</td>
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### Tuesday June-16

**PSC1 Technology Short Course E-Pitch & Q/A Panel**

**Future of Scaling for Logic and Memory**

**June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)**

**Session Chairs:** Nimul Ramaswamy (Micron), Kazuhiko Endo (AIST)

- Nicolas Loubet, IBM, USA
- Mauro Kobrinisky, Intel, USA
- Gwan-Hyeob Koh, Samsung Electronics, Republic of Korea
- Uwe Schroeder, NaMLab gGmbH, Germany
- Anthony Yen, ASML, USA
- Chang-Hong Shen, Taiwan Semiconductor Research Institute, Taiwan
- Suman Datta, University of Notre Dame, USA
- Tatsuo Maeda, National Institute of Advanced Industrial Science and Technology, Japan

**PSC2 Joint Short Course E-Pitch & Q/A Panel**

**Heterogeneous Integration – To Boldly Go Where No Moore Has Gone Before**

**June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)**

**Session Chairs:** Vijay Narayanan (IBM), Alvin Loke (TSMC)

- Samuel Naftziger, AMD, USA
- Eric Beyne, imec, Belgium
- Key Chung, SPIL R&D, Taiwan
- Arvind Kumar & Mukta Farooq, IBM Research, USA
- Marco Del Sarto, STMicroelectronics, Italy
- Kenny C.H. Hsieh, TSMC, Taiwan
- Rajesh Gupta, Synopsys, USA
- Ki Chul Chun, Samsung Electronics, Republic of Korea

**PSC3 Circuits Short Course E-Pitch & Q/A Panel**

**Trends and Advancements in Circuit Design**

**June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)**

**Session Chairs:** Xin Zhang (IBM), Minkyu Je (KAIST)

- Wing-Hung Ki, Hong Kong University of Science and Technology, China
- Michael Flynn, University of Michigan, USA
- Koff Makanwa, Delft University of Technology, Netherlands
- Jae-Yoon Sim, POSTECH, Republic of Korea
- Yao-Hong Liu, imec, Netherlands
- Mourir Meghelli, IBM, USA
- Thomas Burd, AMD, USA
- Yih Wang, TSMC, Taiwan

**P4 SSCS/EDS-Sponsored Diversity Panel - Cultivating Engineering Confidence**

**June-16 08:00 PDT / June-16 17:00 CET / June-17 00:00 JST (1 hour)**

**Session Chairs:** Nadine Collaert (imec), Carolina Mora Lopez (imec)

- Susan Feindt, Analog Devices, USA
- Danielle Griffith, Texas Instruments, USA
- Makoto Ikeda, University of Tokyo, Japan
- Myung-Hee Na, imec, Belgium
EC1 Executive Session - Memory (2)
June-16 09:00 PDT / June-16 18:00 CET / June-17 01:00 JST (1 hour)

Session Chairs: Gosia Jurczak (Lam Research)

CM1.4 - 2X-Bandwidth Burst ST-RAM for Memory Bandwidth Limited Workloads
Charles Augustine, Intel, USA

CM2.1 - A 14.7mV/μm² 28nm FDSOI STT-MRAM with Current Starved Read Path, 52Ω/Sigma Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference
El Mehdi Boujamaa, Arm, France

CM3.2 - A 65nm 16kb SRAM with 131.5pW Leakage at 0.9V for Wireless IoT Sensor Nodes
Shourya Gupta, University of Virginia, USA

CM3.3 - 1.03pJ/Write Ultra-Low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors
Jingcheng Wang, University of Michigan, USA

JFS3.3 - Buried Powered SRAM DTCO and System-Level Benchmarking in N3
Shairfe Salahuddin, imec, Belgium

TF1.2 - A Novel Dual Ferroelectric Layer Based MFMIS FeFET with Optimal Stack Tuning Toward Low Power and High-Speed NVM for Neuromorphic Applications
Tarek Ali, Fraunhofer IPMS Center Nanoelectronic Technologies, Germany

TF2.4 - Nanosecond Laser Anneal (NLA) for Si-Implanted HfO₂ Ferroelectric Memories Integrated in Rack-End Of Line (BEOL)
Laurent Grenouillet, CEA-LETI-MINATEC, France

TF2.7 - Probing the Evolution of Electrically Active Defects in Doped Ferroelectric HfO₂ During Wake-Up and Fatigue
Emilio Carrijo, Intel, USA

TM1.4 - Understanding of Tunable Selector Performance in Si-Ge-As-Se OTS Devices by Extended Percolation Cluster Model Considering Operation Scheme and Material Design
Sohchi Kabuyanagi, Kioxia, imec, Japan

TM2.1 - A SiO₂ RRAM-Based Hardware with Spike Frequency Adaptation for Power-Saving Continual Learning in Convolutional Neural Networks
Irene Munoz-Martin, Politecnico di Milano, Italy

TMFS.2 (Invited) - Magnetic Random Access Memories (MRAM) Beyond Information Storage
Ricardo Sousa, Université Grenoble Alpes / CEA / CNRS, Spintec, France

EC2 Executive Session - Analog Building Blocks
June-16 09:00 PDT / June-16 18:00 CET / June-17 01:00 JST (1 hour)

Session Chairs: Ewout Martens (imec)

CD1.2 - A 10-bit 100MS/s SAR ADC with Always-on Reference Ripple Cancellation
Xuexuan Tang, University of Texas at Austin, USA

CD1.5 - A Compact 140GS/s 8-bit Switched-Capacitor DAC in 16nm FinFET CMOS
Pietro Caragiolo, Stanford University, USA

CD2.1 - A 440μW, 109.8dB DR, 106.5dB SNDR Discrete-Time Zoom ADC with a 20kHz BW
Efraim Eland, Delft University of Technology, Netherlands

CF1.2 - A Fast Locking 5.8-7.2 GHz FMCW Radar Antenna with Sub-2μs Settling Time in 22nm FDSOI
Jeffrey Prinzte, Katholieke Universiteit Leuven, Belgium

CF1.4 - A 3.3-V 101fA/mm² Jitter -0.25dB POM Fractional-N DPLL with Phase Error Detection Accomplished in Fully Differential Voltage Domain
Lianbo Wu, ETH Zurich, Switzerland

CF3.5 - A 16-12b A/D Converter Achieving a Sensitivity of -103dBm at 0.5mW via an Integrated N-Path Filter Bank
Ali Nikoofard, University of California San Diego, USA

CP1.1 - A -107.8dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier
Huajun Zhang, Delft University of Technology, Netherlands

CP3.5 - A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency
Xiaose Li, Intel, USA

JFSS.4 - A 3D-Stacked Cortex-M0 SoC with 20.3Gbps/mm² 7.1mW/mm² Simultaneous Wireless Inter-Tier Data and Power Transfer
Benjamin Fletcher, University of Southampton, United Kingdom

EC3 Executive Session - Adaptive Systems
June-16 10:00 PDT / June-16 19:00 CET / June-17 02:00 JST (1 hour)

Session Chairs: Bora Nikolic (University of California, Berkeley)

CC2.2 - An Autonomous Reconfigurable Power Delivery Network (RPDN) for Many-Core SoCs Featuring Dynamic Current Steering
Khondker Ahmed, Intel Coporation, USA

CD1.1 - A 1MgS/i to 1Gsgs Ringamp-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm
Benjamin Hershberg, imec, Belgium

CD2.4 - A 1G/s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9dB FoM
Yitan Lyu, MICAS-Katholieke Universiteit Leuven, Belgium

CP3.1 - An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Integrated N-Path Filter Bank
Ali Nikoofard, University of California San Diego, USA

CP3.5 - A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency
Xiaose Li, Intel, USA

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Benjamin Fletcher, University of Southampton, United Kingdom

Session Chairs: Nadine Colaert (imec)

Moderator: Arindam Mallik, imec, Belgium

WS1.1 - Prospects of Analog In-Memory Computing – An Overview
Boris Murmann, Stanford University, USA

WS1.2 - Designing Material Systems and Algorithms for Analog Computing
Robert L. Bruce, IBM Research, USA

WS1.3 - Monolithically Integrated RRAM-Based Analog/Mixed-Signal In-Memory Computing for Energy-Efficient Deep Learning
Jae-Seo Seo, Arizona State University, USA

WS1.4 - Compute-In-Memory Circuit and Device Technologies: Trends and Prospects
Jaydeep Kulkarni, University of Texas at Austin, USA

WS1.5 - Analog Computing for Machine Learning – An Ideal Case for Co-Optimization of System and Device Technology
Arindam Mallik, imec, Belgium

WS1.6 - System and Architecture Level Considerations in Leveraging Mixed-Signal Techniques for ML at the Edge
Mahesh Mehendale, Texas Instruments, USA

PWS1 Workshop 1 Panel and Q&A - Analog Computing Technologies and Circuits for Efficient Machine Learning Hardware
June-16 10:00 PDT / June-16 19:00 CET / June-17 02:00 JST (1 hour)

Session Chairs: Nadine Colaert (imec)

Moderator: Arindam Mallik, imec, Belgium

WS1.1 - Prospects of Analog In-Memory Computing – An Overview
Boris Murmann, Stanford University, USA

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WS1.6 - System and Architecture Level Considerations in Leveraging Mixed-Signal Techniques for ML at the Edge
Mahesh Mehendale, Texas Instruments, USA

P1 Technology Panel - Memory and Logic Technology Divergence: Will AI/ML bring them back together?
June-16 17:00 PDT / June-17 02:00 CET / June-17 09:00 JST (1 hour)

Organizers: Greg Yeric (Arm), Hiroshi Morikoa (Socionext)

Moderator: Gary Bronner, Rambus, USA
Subramanian Iyer, University of California, Los Angeles, USA
Steve Pawlowski, Micron, USA
Vivienne Sze, Massachusetts Institute of Technology, USA
Keh-Chung Wang, Macronix International, Taiwan
Zhao Wang, Facebook, Japan
## PWS2 Workshop 2 Panel and Q&A - Know Where You Are Going; Metrology In the New Age of Semiconductor Manufacturing

**June-16 19:00 PDT / June-17 04:00 CET / June-17 11:00 JST (1 hour)**

**Session Chairs:** Gosia Jurczuk (Lam Research), Takaaki Tsunomura (Tokyo Electron)  
**Moderator:** Tom Larson, Nova Measuring Instruments

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<td>Introduction to Metrology Workshop</td>
<td>Tom Larson, Nova Measuring Instruments</td>
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<td>WS2.2</td>
<td>Manufacturing Process Challenges and Requirements for Metrology in Semiconductor Memory Devices</td>
<td>Keiji Suzuki, Kioxia</td>
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<td>WS2.3</td>
<td>Metrology with Angstrom Accuracy Required by Logic IC Manufacturing – Challenges From R&amp;D to High Volume Manufacturing and Solutions in the AI Era</td>
<td>Yi Hung Lin, TSMC</td>
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<td>WS2.4</td>
<td>Dimensional Metrology Overview, Trends and Upcoming Challenges</td>
<td>Philippe Leray, imec</td>
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<td>WS2.5</td>
<td>Defect Inspection: A Trio of Trends for the 2020s</td>
<td>Mark Shirley, KLA</td>
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<td>WS2.6</td>
<td>Enabling Modern Semiconductor Manufacturing With Materials Metrology</td>
<td>Kavita Shah, Nova Measuring Instruments</td>
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<td>WS2.7</td>
<td>Opportunities and Challenges for Lab-based Characterization for Emerging Technologies</td>
<td>Markus Kuhn, Intel</td>
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## Wednesday, June 17

### PFF Forum E-Pitch & Q/A Panel

**June-17 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)**

**Session Chairs:** Gosia Jurczak (Lam Research), Takaaki Tsunomura (Tokyo Electron)  
**Moderator:** Tom Larson, Nova Measuring Instruments

### PL2 - Plenary 2

**SELECT June-17 08:00 PDT / June-17 17:00 CET / June-18 00:00 JST OR June-17 17:00 PDT / June-18 02:00 CET / June-18 09:00 JST (2 hours)**

**Session Chairs:** Tomas Palacios (MIT), Yuuuke Ohike (Sony Semiconductor Solutions)

- **PL2.1 (Plenary) - The Future of Compute: How the Data Transformation is Reshaping VLSI**  
  Michael Mayberry, Intel, USA

- **PL2.2 (Plenary) - Empowering Next-Generation Applications through FLASH Innovation**  
  Shigeo (Jeff) Ohshima, Kioxia, Japan

### EE1 Executive Session - Ultra Low Energy Systems

**June-17 10:00 PDT / June-17 19:00 CET / June-18 02:00 JST (1 hour)**

**Session Chairs:** Danielle Griffith (Texas Instruments)

- **CF3.2 (Invited) - Industrial IoT with Crystal-Free Mote-on-Chip**  
  Thomas Watteyne, Inria, France

- **CF3.3 - A Multichannel, MEMS-Less ~99dBm 260nW Bit-level Duty Cycled Wakeup Receiver**  
  Anjana Dissanayake, University of Virginia, USA

- **CF3.4 - A 4.44W ~92/90.3dBm Sensitivity Dual-mode BLE/ Wi-Fi Wake-Up Receiver**  
  Po-Han Peter Wang, University of California San Diego, USA

- **CF4.1 - A 8.7 ppm/°C, 694nW, One-Point Calibrated RC Oscillator Using a Nonlinearity-Aware Dual Phase-Locked Loop and DSM-Controlled Frequency-Locked Loops**  
  Giorgio Cristiano, ETH Zurich, Switzerland

- **CF4.2 - A 0.8 pJ/ cycle 8ppm/°C DFLL-based Wakeup Timer Enabled by a Time-Domain Trimming and an Embedded Temperature Sensing**  
  Ming Ding, imec, Netherlands

### PWS3 Workshop 3 Panel and Q&A - Quantum Computers for Electrical Engineers

**June-17 10:00 PDT / June-17 19:00 CET / June-18 02:00 JST (1 hour)**

**Session Chairs:** Maud Vinet (CEA-Leti)

**Moderator:** Iuliana Radu, imec, Belgium

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<td>Bruna Paz, CEA-Leti-MINATEC, France</td>
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<td>Toward Long-Coherence-Time Si Spin Qubit: The Origin of Low-Frequency Noise in Cryo-CMOS</td>
<td>Hiroshi Oka, National Institute of Advanced Industrial Science and Technology, Japan</td>
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<td>William Oliver, Massachusetts Institute of Technology</td>
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<td>Superconducting Qubits: How Technology/ Processing/ Materials Impact Coherence Time and How Design Impacts Gate Fidelity</td>
<td>Doug McClure, IBM, USA</td>
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<td>WS3.7</td>
<td>Si Based Qubits: Technology and Material Impact on Performance</td>
<td>Iuliana Radu, imec, Belgium</td>
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<td>WS3.4</td>
<td>Architectures Challenges for Si Spin Qubits</td>
<td>Maud Vinet, CEA-Leti, France</td>
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<td>WS3.5</td>
<td>Cryo-CMOS Components for Quantum Tech</td>
<td>Joseph Bardin, Google AI Quantum &amp; University of Massachusetts Amherst, USA</td>
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**EF1 Executive Session - Ferroelectrics**

**June 17 19:00 PDT / June 18 04:00 CET / June 18 11:00 JST (1 hour)**

Session Chairs: Sunan Datta (University of Notre Dame), Byoung-Hun Lee (Gwangju Institute of Science & Technology)

**TF1.1 - FeFET Memory Featuring Large Memory Window and Robust Endurance of Long-Pulse Cycling by Interface Engineering Using High-k AON**

Chu-Yu Chan, National Tsing Hua University, Taiwan

**TF1.2 - Re-Examination of Vt Window and Reliability in HfO2 FeFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation**

Reika Ichihara, Kioxia Corporation, Japan

**TF1.3 - Hot Electrons as the Dominant Source of Degradation for Sub-5nm HfO2 FeFETs**

Ava Tan, University of California, Berkeley, USA

**TF1.4 - A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation**

Kai Ni, Rochester Institute of Technology, USA

**TF1.5 - Asymmetric Polarization Response of Electrons and Holes in Si FeFETs: Demonstration of Absolute Polarization Hysteresis Loop and Inversion Hole Density Over 2×10^{17} cm^{-2}**

Kasidit Toprasertpong, University of Tokyo, Japan

**TF2.1 - SiO2 Compatible 1T1C FeRAM Memory Array Based on Ferroelectric HfOx(Zr0.5Ti0.5)O2**

Jun Okuno, Sony Semiconductor Solutions, Japan

**TF2.2 - Improved State Stability of HfO2 Ferroelectric Tunnel Junction by Template-Induced Crystalization and Remote Scavenging for Efficient In-Memory Reinforcement Learning**

Shosuke Fuji, Kioxia, Japan

**TF2.5 - Fast Thermal Quenching on the Ferroelectric Al: HfO2 Thin Film with Record Polarization Density and Flash Memory Application**

Changhwan Choi, Hanyang University, Republic of Korea

**TF2.6 - Multi-Probe Characterization of Ferroelectric/Dielectric Interface by C-V, P-V and Conductance Methods**

Jungang Li, Purdue University, USA

**TF2.8 - Atomic-Scale Imaging of Polarization Switching in an (Anti)-Ferroelectric Memory Material: Zirconia (ZrO2)**

Sarah Lombardo, MSEE, Georgia Institute of Technology, USA

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**Thursday, June 18**

**EG1 Executive Session - Heterogeneous Integration (2)**

**June 18 08:00 PDT / June 18 17:00 CET / June 19 00:00 JST (1 hour)**

Session Chairs: Bill En (AMD)

**JF1.5 - O-Band GeSi Quantum-Confined Stark Effect Electro-Absorption Modulator Integrated in a 220nm Silicon Photonics Platform**

Clement Porret, imec, Belgium

**TH1.2 - 3D Heterogeneous Package Integration of AmMagnetic Core Inductor: 89%-Efficiency Buck Converter with Backside Power Delivery Network**

Xiao Sun, imec, Belgium

**TH1.4 - ExaNoDe: Combined Integration of Chiplets on Active Interposer with Bare Dice in a Multi-Chip-Module for Heterogeneous and Scalable High Performance Nodes**

Pierre-Yves Martinez, Université Grenoble Alpes, CEA-LIST, France

**TH2.1 - BEOL Compatible Dual-Gate Ultra Thin-Body W-Doped Indium-Oxide Transistor with l_{on} > 370µm, SS > 73mV/dec and T_{on}/T_{off} ratio > 4x10^2**

Wniddi Chakraborty, University of Notre Dame, USA

**TH3.1 - First Monolithic Integration of 3D Complementary FET (CFET) on 300mm Wafers**

Sujith Subramanian, imec, Belgium

**TH3.2 - 3D Sequential Low Temperature Top Tier Devices Using Dopant Activation with Excimer Laser Anneal and Strained Silicon as Performance Boosters**

Anne Vandooren, imec, Belgium

**TH3.3 - 28nm FDSOI CMOS Technology (FEOL and BEOL) Thermal Stability for 3D Sequential Integration: Yield and Reliability Analysis**

Camila Cavalcante, CEFET-Let, France

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**EG2 Executive Session - Robust Computing**

**June 18 08:00 PDT / June 18 17:00 CET / June 19 00:00 JST (1 hour)**

Session Chairs: Carlos Tokunaga (Intel)

**CC1.1 - Performance-Flexible Energy-Optimized Automotive-Grade Cortex-R4F SoC Through Combined AVS/ABB-Bias-in-Memory-Army Closed-Loop Regulation in 28nm FD-SOI**

Ricardo Gomez Gomez, STMicroelectronics, France

**CC1.2 - A SCA-Resistant AES Engine in 14nm CMOS with Time/Frequency-Domain Leakage Suppression Using Non-linear Digital LDO Cascaded with Arithmetic Countermeasures**

Raghavan Kumar, Intel, USA

**CC1.3 - A 0.26% BER, 10^{25} Challenge-Response Machine-Learning Resistant Strong-PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection**

Vikram Suresh, Intel, USA

**CC1.4 - A 435MHz, 2.58Gbps Side-Channel-Attack Resistant Crypto-Processor for Secure RSA-4K Public-Key Encryption in 14nm CMOS**

Raghavan Kumar, Intel, USA

**CC2.1 - A Proactive Voltage-Drop-Mitigation System in a 7nm Hexagon™ Processor**

Vijay Kiran Kalyanam, Qualcomm Technologies, USA

**CC2.2 - UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in Designs with Large Clock Distribution Delays in 65nm CMOS**

Xun Sun, University of Washington, USA

**CC2.3 - Low-Clock-Power Digital Standard Cell IPs for High-Performance Graphics/Al Processors in 10nm CMOS**

Steven Hsu, Intel, USA

**Luncheon - Do You Really Know What Is In Your Computer? Perspectives on Verifiable Supply Chains**

Andrew "bunnie" Huang, Singapore

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**EG3 Executive Session - AI/ML**

**June 18 09:00 PDT / June 18 18:00 CET / June 19 01:00 JST (1 hour)**

Session Chairs: Paul Whatmough (ARM)

**CA1.1 - A 3.0 TFLOPS 0.62V Scalable Processor Core for High Compute Utilization AI Training**

Sae Kyu Lee, IBM T. J. Watson Research Center, USA
EH2 Executive Session - High Speed Circuits, Systems, and Devices
June-18 17:00 PDT / June-19 02:00 CET / June-19 09:00 JST (1 hour)

Session Chairs: Parag Upadhyaya (Xilinx), Ho-Jin Song (POSTECH)

CF2.1 - A 29% PAE 1.8bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked PLL
Yuncheng Zhang, Tokyo Institute of Technology, Japan

CF2.2 - A 2.8GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation
Jian Pang, Tokyo Institute of Technology, Japan

CF2.3 - A 293/440 GHz Push-Push Double Feedback Oscillators with 5.0/-3.9dBm Output Power and 2.9/0.6% DC-to-RF Efficiency in 65nm CMOS
Dzuhn Rاديyo Utomo, Korea Advanced Institute of Science and Technology, Republic of Korea

CF2.4 - A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-Gmox Gain Boosting Technique
Dae-Woong Park, imec, Republic of Korea

CW2.1 - A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 5-Point ZQ Calibration for Memory Interfaces
Yong-Un Jeong, Seoul National University, Republic of Korea

CW2.2 - A 0.1pJ/b dB 28Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler
Moon-Chul Choi, Seoul National University, Republic of Korea

JFS2.3 - A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring 7nm EUV Process Technology
Minjung Jin, Samsung Electronics, Republic of Korea

JFS2.4 - Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implanted-Induced Strain Relaxation and Comb-like Device Architecture
Chen Sun, National University of Singapore, Singapore

JFS2.5 - An RF Transceiver with Full Digital Interface Supporting 5G New Radio FRT with 3.84Gbps DL/1.92Gbps UL and Multi-Band GNSS in 14nm FinFET CMOS
Sangwook Han, Samsung Electronics, Republic of Korea

JFS2.7 - A 1.96Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems
Chen-Chien Kao, National Taiwan University, Taiwan

EH3 Executive Session - New Devices and Applications
June-18 18:00 PDT / June-19 03:00 CET / June-19 10:00 JST (1 hour)

Session Chairs: Peide Ye (Purdue University), Masaharu Kobayashi (University of Tokyo)

TN1.1 - Hair-Like Nanostructure Based Ion Detector Using 16nm FinFET Technology
Chien-Ping Wang, National Tsing Hua University, Taiwan

TN1.2 - Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry
Chia-Che Chung, National Taiwan University, Taiwan

TN1.3 - Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFET for Advanced Hardware Security
Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China

TN1.4 - A Bias and Correlation-Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking
Kai Ni, Rochester Institute of Technology, USA

TN1.5 - A 1.9x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy
Xu Bai, NEC, Japan

TN1.6 - Proposal and Experimental Demonstration of Reservoir Computing Using HfO2/ZN2O3/SiFeFETs for Neuromorphic Applications
Eishin Nako, University of Tokyo, Japan

TN1.7 - High On-Current 2D nFET of 390μA/μm at VDD = 1V using Monolayer CVD MoS2
Ang-Sheng Chou, TSMC, Taiwan

TN1.8 - Ultrahigh Responsivity and Tunable Photogain BEOL Compatible MoS2 Phototransistor Array for Monolithic 3D Image Sensor with Block-Level Sensing Circuits
Chih-Chao Yang, Taiwan Semiconductor Research Institute, Taiwan

EH4 Executive Session - Memory (3)
June-18 18:00 PDT / June-19 03:00 CET / June-19 10:00 JST (1 hour)

Session Chairs: Seung Kang (Qualcomm Technologies), Taung-Yung Jonathan Chang (TSMC)

CM1.1 - A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 175mV VMIN Reduction with Negligible Power Overhead
Zheng Guo, Intel, USA

CM1.2 - A 29.2Mb/mm² Ultra High Density SRAM Macro Using 7nm FinFET Technology with Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit
Yoshisato Yokoyama, Renesas Electronics, Japan

CM1.3 - Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 16T1W 6T-bitcell SRAM in 10nm FinFET CMOS
Jaydeep Kulkarni, Intel, USA

CM1.4 - A 7nm FinFET 4.04-Mb/mm² TCAM with Improved Electromigration Reliability Using Far-Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier
Makoto Yabuuchi, Renesas Electronics, Japan

CM2.3 - A 28nm 1.5Mb Embedded 1T2R RRAM with 14.8 Mb/mm² Using Sneaking Current Suppression and Compensation Techniques
Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China

CM2.4 - A 22nm 96Kx144 RRAM Macro with a Self-Tracking Reference and a Low Ripple Charge Pump to Achieve a Configurable Read Window and a Wide Operating Voltage Range
Chung-Cheng Chou, TSMC, Taiwan

CM3.1 - A 28nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation
Moon-Chul Choi, Seoul National University, Republic of Korea

CM3.2 - A 1.8Gb/spin 16T NAND Flash Memory Multi-Chip Package with F-Chip of Toggle 4.0 Specification for High Performance and High Capacity Storage Systems
Daehoon Na, Samsung Electronics, Republic of Korea

CM4.1 - A 22nm 3D-Stacked 2T2R 128kx128 MTCMOS SRAM with On-Chip 128Gb/256Gb Flash Memory, 128Gb DRAM, and 128Gb 3D-NAND
Ang-Sheng Chou, TSMC, Taiwan

CM4.2 - A 7nm 4.04-Mb/mm² TCAM Using High-Density, 1R1W 8T-bitcell SRAM in 10nm FinFET CMOS
Jaydeep Kulkarni, Intel, USA

CM4.3 - A 1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Oscillator Phase under Sub-Harmonic Injection Locking
Kai Ni, Rochester Institute of Technology, USA

CM4.4 - A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 175mV VMIN Reduction with Negligible Power Overhead
Zheng Guo, Intel, USA

CM4.5 - A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 5-Point ZQ Calibration for Memory Interfaces
Yong-Un Jeong, Seoul National University, Republic of Korea

CM4.6 - A 0.1pJ/b dB 28Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler
Moon-Chul Choi, Seoul National University, Republic of Korea

CM4.7 - A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring 7nm EUV Process Technology
Minjung Jin, Samsung Electronics, Republic of Korea
### JFS3.4 - Local Variation-Aware Transistor Design through Comprehensive Analysis of Various Vdd/Temperatures Using Sub-7nm Advanced FinFET Technology

Soyoun Kim, Samsung Electronics, Republic of Korea

### TC1.1 - Enabling Multiple-Vt Device Scaling for CMOS Technology Beyond 7nm Node

Vincent Chang, TSMC, Taiwan

### TC1.3 - Cold CMOS as a Power-Performance-Reliability Booster for Advanced FinFETs

H. L. Chiang, TSMC, Taiwan

### TC2.1 - Surface Ga-boosted Boron-doped Si_{0.5}Ge_{0.5} using In-situ CVD Epitaxy: Achieving 1.1 × 10^{21} cm^{-3} Active Doping Concentration and 5.7 × 10^{-10} Ω·cm² Contact Resistivity

Haiwen Xu, National University of Singapore, Singapore

### TC2.3 - First Demonstration of 4-Stacked Ge_{0.915}Sn_{0.085} Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels

Yu-Shiang Huang, National Taiwan University, Taiwan

### TC3.4 - Record Low Contact Resistivity to Ge:B (8.1x10^{-10}Ω·cm²) and GeSn:B (4.1x10^{-10}Ω·cm²) with Optimized [B] and [Sn] by In-situ CVD Doping

Fang-Liang Lu, National Taiwan University, Taiwan

### TC3.5 - High Quality N+/P Junction of Ge Substrate Prepared by Initiated CVD Doping Process

Jaehwan Kim, KAIST, Republic of Korea

### JFS1.1 (Invited) - TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s

Chen Sun, Ayar Labs, USA

### JFS1.2 (Invited) - High-Temperature Operation of Chip-Scale Silicon-Photonic Transceiver

Daisuke Okamoto, PETRA, Japan

### JFS1.3 - A Monolithically Integrated Silicon Photonics 8x8 Switch in 90nm SOI CMOS

Jonathan Proesel, IBM T. J. Watson Research Center, USA

### JFS1.4 - III/V-on-Bulk-Si Technology for Commercially Viable Photonics-Integrated VLSI

Dongiae Shin, Samsung Advanced Institute of Technology, Republic of Korea

### JFS3.1 (Invited) - Heterogeneous System-Level Package Integration – Trends and Challenges

Frank Lee, TSMC, Taiwan

### JFS3.2 - First Demonstration of 4-Stacked Ge_{0.915}Sn_{0.085} Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels

Yu-Shiang Huang, National Taiwan University, Taiwan

### JFS3.3 - Record Low Contact Resistivity to Ge:B (8.1x10^{-10}Ω·cm²) and GeSn:B (4.1x10^{-10}Ω·cm²) with Optimized [B] and [Sn] by In-situ CVD Doping

Fang-Liang Lu, National Taiwan University, Taiwan

### JFS3.5 - High Quality N+/P Junction of Ge Substrate Prepared by Initiated CVD Doping Process

Jaehwan Kim, KAIST, Republic of Korea

### THL.1 - 5G and AI Integrated High Performance Mobile SoC Process-Design Co-Development and Production with 7nm EUV FinFET Technology

Jie Deng, Qualcomm Technologies, USA

### JFS1.1 (Invited) - TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s

Chen Sun, Ayar Labs, USA

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### JFS1.3 - A Monolithically Integrated Silicon Photonics 8x8 Switch in 90nm SOI CMOS

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Dongiae Shin, Samsung Advanced Institute of Technology, Republic of Korea

### JFS3.1 (Invited) - Heterogeneous System-Level Package Integration – Trends and Challenges

Frank Lee, TSMC, Taiwan

### JFS3.2 (Invited) - First Demonstration of 4-Stacked Ge_{0.915}Sn_{0.085} Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels

Yu-Shiang Huang, National Taiwan University, Taiwan

### JFS3.3 - Record Low Contact Resistivity to Ge:B (8.1x10^{-10}Ω·cm²) and GeSn:B (4.1x10^{-10}Ω·cm²) with Optimized [B] and [Sn] by In-situ CVD Doping

Fang-Liang Lu, National Taiwan University, Taiwan

### JFS3.5 - High Quality N+/P Junction of Ge Substrate Prepared by Initiated CVD Doping Process

Jaehwan Kim, KAIST, Republic of Korea

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### End of Program