PROGRAM AT A GLANCE

Welcome to the 2020 Symposia on VLSI Technology and Circuits

The Next 40 Years of VLSI for Ubiquitous Intelligence

40th Anniversary

The 2020 Symposia on VLSI Technology & Circuits celebrates its 40th year with a virtual conference and the central theme of "The Next 40 Years of VLSI for Ubiquitous Intelligence". This week-long virtual conference features a fully overlapped program pushing the state-of-the-art in Technology and Circuits, packed with over 200 contributed technical presentations, technology and circuit demonstrations, 3 short courses, our “Friday” Forum and a “Luncheon Talk" that will be offered on-demand from the conference websites. These materials will be available for viewing at your convenience between June 14 to June 27 with the short courses and forum offering early access starting on June 8.

In addition to the on-demand sessions, the VLSI Symposia on Technology and Circuits will also feature an exciting program of live streaming events. This includes 2 plenary sessions, 4 panel discussions, 3 workshops, and 25 Executive Sessions. The goal of Executive Sessions in the VLSI Symposia is to foster a discussion about the current state and future of the field. They will include 2-minute summaries of relevant papers that have been presented at VLSI Symposia 2020 on the topic, along with 35 minutes of discussion among the authors and session chairs on key challenges and opportunities. All conference participants are encouraged to join these meetings and contribute with insight and questions.

Thank you for your support of the Symposia, especially during this unprecedented pandemic time. We hope you enjoy the Symposia and wish you and your family continued good health.

The Organizing Committee

VLSI Symposia in a Nutshell

PDT	Live Streaming *Watch at scheduled times*	On-Demand *Watch pre-recorded videos at your convenience*	Papers & Slides Download *See email sent to paid attendees*
June 8 (Mon)		Early Access for • All 3 Short Courses • Forum	• Papers & slides of Joint Focus, Technology & Circuits Session papers • Slides of all 3 Short Courses • Slides of Forum
June 9 (Tue)			
June 10 (Wed)			
June 11 (Thu)			
June 12 (Fri)			
June 13 (Sat)			
June 14 (Sun)			
June 15 (Mon)	• Plenary 1 Session • Exeuctive Sessions EA & EB		
June 16 (Tue)	• All Short Courses Summary & Q&A • Executive Sessions EC & ED • 3 Panels - Technology, Circuits, Diversity • Workshop - Technology/Circuits for ML • Workshop - Metrology		
June 17 (Wed)	• Plenary 2 • Executive Sessions EE & EF • Forum Summary & Q&A • Workshop - Quantum Computing	• All 3 Short Courses • Forum • Joint Focus Sessions • Technology Sessons • Circuits Sessions • Joint Panel • Demo Session • Luncheon Talk • All Workshops • Full Recordings of All Live Events (available day after Live Event) except Young Professionals Mentoring	
June 18 (Thu)	• Executive Sessions EG & EH • Young Professionals Mentoring		
June 19 (Fri)			
June 20 (Sat)			
June 21 (Sun)			
June 22 (Mon)			
June 23 (Tue)			
June 24 (Wed)			
June 25 (Thu)			
June 26 (Fri)			
June 27 (Sat)			
June 28 (Sun)			
June 29 (Mon)			

On-Demand Content

On-Demand Technology, Circuits, and Joint Sessions are similar to typical paper sessions at previous Symposia on VLSI Technology and Circuits. The 2-page paper abstracts, presentation slides, and 20-minute video presentations are provided for your convenience "on-demand" anytime between June 14 (starting at 9:00am PDT) and June 27 (ending at 11:59pm PDT). Early on-demand access for short courses and the forum begins on June 8 at 9:00am PDT.

While viewing a recorded presentation, you can ask questions by typing your them in the "Q&A box", stating first the paper number and then your question. Your question will be directed to the session chairs and authors to respond.

Short Courses & Forum	Technology Sessions		Joint Focus Sessions	Circuits Sessions		
SC1 Future of Scaling for Logic/Memory	THL Highlight Session	TH3 Si Technologies for 3D Integration	JFS1 Silicon Photonics	CA1 Machine Learning	CC2 Adapt Clocking & Power Delivery	CM2 Emerging Memory Design
SC2 Heterogeneous Integration	TC1 Advanced Si CMOS Devices	TM1 NAND/NOR/PCM	JFS2 5G/mm-Wave	CA2 Visual Processing & AI	CD1 High-Speed Data Converters	CM3 Energy Efficient Memory Design
SC3 Trends/Advances in Circuit Design	TC2 Ge and SiGe Devices	TM2 RRAM	JFS3 STCO/DTCO	CA3 Digital Systems	CD2 Data Converter Techniques	CP1 Amplifiers
FF Tech/Circuits for Edge Intelligence	TC3 Advanced Processing	TM3 STT MRAM	JFS4 Devices & Circuits for AI/ML	CB1 Biomedical Sensors	CF1 Advanced PLLs	CP2 Volt References & Wireless Power
Workshops	TF1 FeFETs	TMFS MRAM Future - Beyond STT	JFS5 Heterogeneous Integration	CB2 Image Sensor & Techniques	CF2 RF & mm-Wave Circuits	CP3 Power Converters
WS1 Analog Compute Tech/Circ for ML	TF2 Ferroelectric Memory & Caps	TN1 New Devices & Applications	Other Events	CB3 Physical Sensors	CF3 IoT and Wireless Receivers	CW1 Ultra-High-Speed Wireline
WS2 Semiconductor Metrology	TH1 3D Packaging	TN2 Quantum Computing	DEMOS	CB4 Front-Ends for Sensor Interfaces	CF4 Low Power Oscillators	CW2 Wireline Techniques
WS3 Quantum Computing	TH2 Semiconducting Oxides for 3D	P2 Joint Panel	Luncheon Talk	CC1 Circuits for Security & Safety	CM1 Advanced SRAM Design	

	Session	Available
On-Demand Sessions	Short Courses & Forum	June-08 to June-27
	Technology, Joint Focus & Circuits Sessions	June-14 to June-27
	P2 Joint Panel	
	Demo Session	
	Luncheon Talk	
	Workshops	
Full Recording of Live Events (available day after event)	PL1 Plneary	June-16 to June-27
	Executive Sessions EA & EB	
	PSC1-3 Short Courses Summaries and Q&A	June-17 to June-27
	Executive Sessions EC & ED	
	P1, P3, P4 Panels	
	PWS1-2 Workshop Summaries and Q&A	
	PL2 Plenary	June-18 to June-27
	PFF Forum Summary and Q&A	
	Executive Sessions EE & EF	
	PWS3 Workshop Summaries and Q&A	

Live Streaming Content

All live events (except Young Professionals event) will be available for on-demand access the day after event until June-27

PDT Pacific Daylight Time (e.g., Los Angeles)
CET Central European Time (e.g., Netherlands)
JST Japan Standard Time (e.g., Japan, South Korea)

Traditional Sessions | Moderated Panels | Executive Sessions | Workshop Panel | What is an Executive Session? | Webex

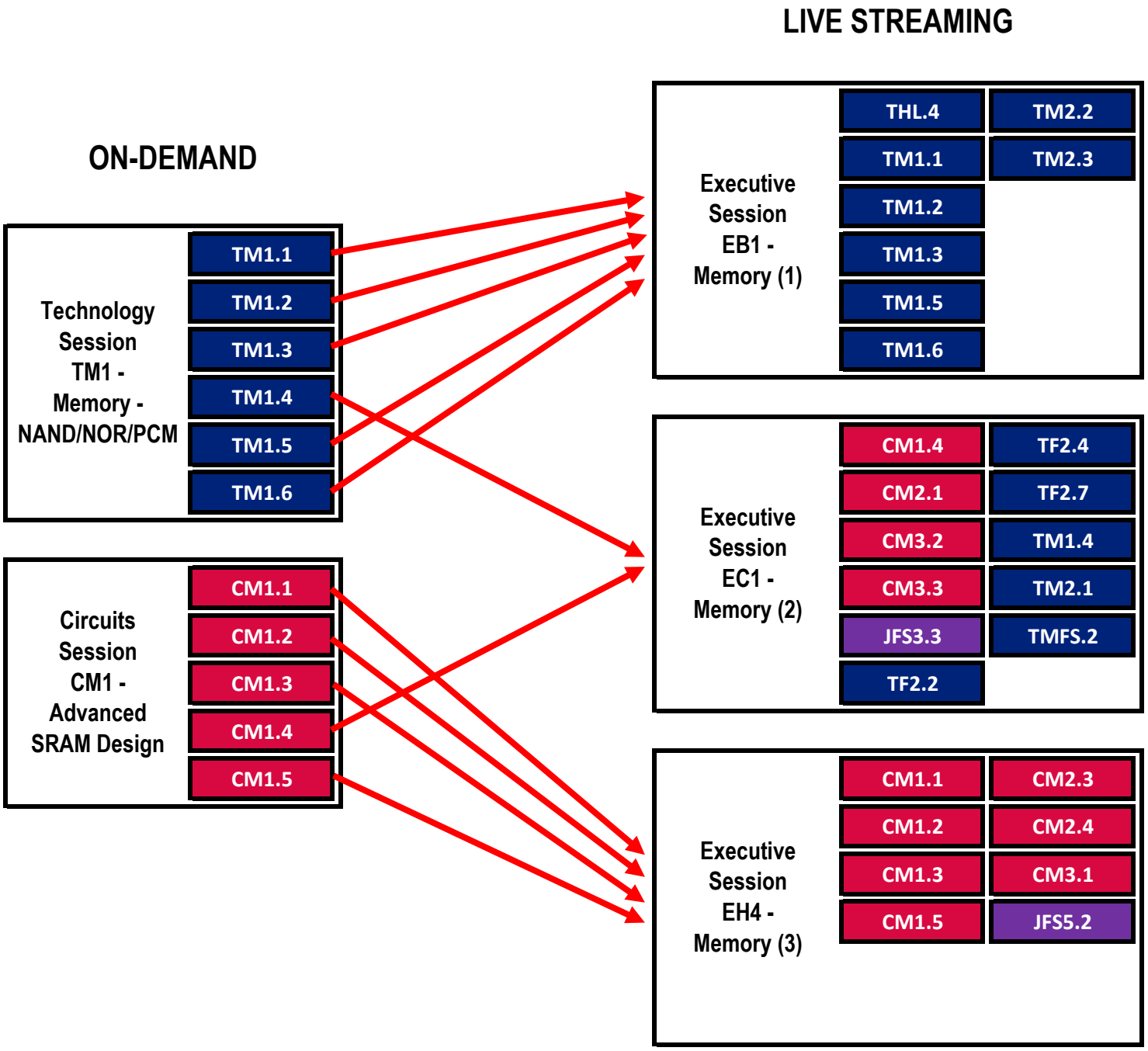
PDT	CET	JST	Monday June-15	Tuesday June-16	Wednesday June-17	Thursday June-18
06:00 to 07:00	15:00 to 16:00	22:00 to 23:00		PSC1 Tech SC Summary & Q/A; PSC2 Joint SC Summary & Q/A; PSC3 Circuit SC Summary & Q/A	PFF Forum E-Pitch & Q/A	
08:00 to 09:00	17:00 to 18:00	00:00 to 01:00 next day	PL1 Joint Plenary 1	P4 SSCS/EDS Diversity Panel: Cultivating Engineering Confidence in COVID-19 Times	PL2 Joint Plenary 2	EG1 Heterogeneous Integration (2); EG2 Robust Computing
09:00 to 10:00	18:00 to 19:00	01:00 to 02:00 next day		10-minute break; EC1 Memory (2); EC2 Analog Building Blocks		10-minute break; EG3 AI/ML; EG4 Sensing Interfaces & Building Blocks
10:00 to 10:50	19:00 to 19:50	02:00 to 02:50 next day	10-minute break; EA1 Advanced CMOS (1); EA2 Sensor Systems	10-minute break; EC3 Adaptive Systems; PWS1 Technology & Circuits for ML Workshop	10-minute break; EE1 Ultra Low Energy Systems; PWS3 Quantum Computing Workshop	10-minute break; EG5 Devices & Circuits for Adv Comm; EDS/SSCS Young Professionals Event
17:00 to 18:00	02:00 to 03:00 next day	09:00 to 10:00 next day	PL1 Joint Plenary 1	P1 Technology Panel; P3 Circuits Panel	PL2 Joint Plenary 2	EH1 MRAM; EH2 High Speed Circuits, Systems & Devices
18:00 to 19:00	03:00 to 04:00 next day	10:00 to 11:00 next day		10-minute break; ED1 Heterogeneous Integration (1); ED2 Power		10-minute break; EH3 New Devices & Applications; EH4 Memory (3)
19:00 to 19:50	04:00 to 04:50 next day	11:00 to 11:50 next day	10-minute break; EB1 Memory (1); EB2 Intelligent Computing	10-minute break; ED3 3D Packaging; ED4 Sensors; PWS2 Metrology Workshop	10-minute break; EF1 Ferroelectrics; EF2 Adv Clocking & Data Converters	10-minute break; EH5 Advanced CMOS (2); EH6 Si Photonics & DTCO

NEW!!! What is an Executive Session?

This year's Virtual Symposia introduces new live Executive Sessions to foster live discussions and complement the On-Demand Sessions. The Executive Sessions feature 2-minute summaries of papers assigned to each executive session, along with 35 minutes of discussion among the authors and session chairs on key challenges and opportunities. All conference participants are encouraged to join these meetings and contribute with insights and questions.

There are a total of 25 live 50-minute executive sessions. Every On-Demand Technology, Circuits, and Joint Session paper as well as the Luncheon Talk is assigned to one Executive Session. Papers from each on-demand session may be mapped to several executive sessions.

Example mapping:



VLSI Symposia 2020 - Virtual Program

On Demand Presentations

Short Courses & Forum

SC1 Technology Short Course - Future of Scaling for Logic and Memory

Session Chairs: Nirmal Ramaswamy (Micron), Vijay Narayanan (IBM), Kazuhiko Endo (AIST)

SC1.1 - Nanosheet Transistor as a Replacement of FinFET for Future Nodes: Device Advantages & Specific Process Elements	Nicolas Loubet, IBM, USA
SC1.2 - On-Die Interconnect Challenges and Opportunities for Future Technology Nodes	Mauro Kobrinsky, Intel, USA
SC1.3 - Challenges and Prospects of Memory Scaling	Gwan-Hyeob Koh, Samsung Electronics, Republic of Korea
SC1.4 - Ferroelectric Hafnium Oxide: From Memory to Emerging Applications	Uwe Schroeder, NaMLab gGmbH, Germany
SC1.5 - EUV Lithography and Its Application to Logic and Memory Devices	Anthony Yen, ASML, USA
SC1.6 - Emerging Technologies for TSV-free Monolithic 3DIC	Chang-Hong Shen, Taiwan Semiconductor Research Institute, Taiwan
SC1.7 - In situ BEOL Transistors and Oxide Electronics	Suman Datta, University of Notre Dame, USA
SC1.8 - Layer Transfer Technology for Heterogeneous Material Integration	Tatsuro Maeda, National Institute of Advanced Industrial Science and Technology, Japan

SC2 Joint Short Course - Heterogeneous Integration – To Boldly Go Where No Moore Has Gone Before

Session Chairs: Alvin Loke (TSMC), Vijay Narayanan (IBM), Kazuhiko Endo (AIST), Makoto Nagata (Kobe University)

SC2.1 - Chiplet Meets the Real World: Benefits and Limits of Chiplet Designs	Samuel Naffziger, AMD, USA
SC2.2 - Heterogeneous System Partitioning and the 3D Interconnect Technology Landscape	Eric Beyne, imec, Belgium
SC2.3 - Back-End Based Chiplet Integration Solutions & Roadmap	Key Chung, SPIL R&D, Taiwan
SC2.4 - Heterogeneous Integration for AI Architectures	Arvind Kumar & Mukta Farooq, IBM Research, USA
SC2.5 - Heterogeneous Integration of Chiplets for Sensors	Marco Del Sarto, STMicroelectronics, Italy
SC2.6 - Chiplet-to-Chiplet Communication Circuits for 2.5D/3D Integration Technologies	Kenny C.H. Hsieh, TSMC, Taiwan
SC2.7 - Performance-Driven Design Methodology and Tools for 2.5D/3D Multi-Die Integration	Rajesh Gupta, Synopsys, USA
SC2.8 - Generic Design Strategies and Considerations for 2.5D and 3D Stacked IC Designs	Ki Chul Chun, Samsung Electronics, Republic of Korea

SC3 Circuits Short Course - Trends and Advancements in Circuit Design

Session Chairs: Xin Zhang (IBM), Minkyu Je (KAIST)

SC3.1 - Topologies and Design Techniques of Switched-Capacitor Converters	Wing-Hung Ki, Hong Kong University of Science and Technology, China
SC3.2 - The Noise-Shaping SAR ADC Technique: The Best of Both Worlds	Michael Flynn, University of Michigan, USA
SC3.3 - Next-Generation Readout of Resistor-Based Sensors	Kofi Makinwa, Delft University of Technology, Netherlands
SC3.4 - Time Reference and Frequency Generation	Jae-Yoon Sim, POSTECH, Republic of Korea
SC3.5 - Low-Power and Digitally-Intensive RF Transceiver Design for IoT Applications	Yao-Hong Liu, imec, Netherlands
SC3.6 - Advances and Trends in High-Speed Serial Links for High-Density IO Applications	Mounir Meghelli, IBM, USA
SC3.7 - Adaptive Circuit & System Design Techniques	Thomas Burd, AMD, USA
SC3.8 - Trends and Design Considerations for Emerging Memories and In-Memory Computing	Yih Wang, TSMC, Taiwan

FF - "Friday" Forum

Session Chairs: Kamel Benaissa (Texas Instruments), Ron Kapusta (Analog Devices), Kazuyuki Tomida (Sony Semiconductor Solutions), Kouichi Kanda (Fujitsu Laboratories)

FF.1 - Edge Intelligence – Technologies, Circuits, Architectures	Ali Keshavarzi, Stanford University, USA
FF.2 - Intelligent Edge – It's Not Just Technology, it's About Responsible Society	Gowri Chindalore, NXP Semiconductors, USA
FF.3 - Heterogeneous Integration Technology Trends at the Edge	Chih Hang Tung, TSMC, Taiwan
FF.4 - Self Powered SOCs for the Intelligent Edge	Benton Calhoun, University of Virginia, USA
FF.5 - CMOS and Beyond CMOS Technologies for Edge Intelligence	Myung Hee Na, imec, Belgium
FF.6 - Low Power Wireless Networking for the Edge	Thomas Watteyne, Analog Devices, USA
FF.7 - Smart Vision Sensor	Hayato Wakabayashi, Sony Semiconductor Solutions, Japan
FF.8 - Efficient Machine Learning at the Edge	David Blaauw, University of Michigan, USA
FF.9 - Security in Edge Devices	Hannes Tschofenig, Arm, USA

Luncheon Talk

Session Chair: Brian Ginsburg (Texas Instruments)

Do You Really Know What Is In Your Computer? Perspectives on Verifiable Supply Chains	Andrew "bunnie" Huang, Singapore

Panel

P2 Joint Panel - 40 Years of VLSI to Enable the Future of Computing

Organizers: Igor Arsovski (Marvell), Greg Yeric (Arm), Ted Letavic (GlobalFoundries), Munehiro Tada (NEC)

Moderator: Stephen Kosonocky, AMD, USA
Asad Abidi, University of California, Los Angeles, USA
Tsu-Jae King Liu, University of California, Berkeley, USA
Akira Matsuzawa, Tokyo Institute of Technology, Japan
Charlie Sodini, Massachusetts Institute of Technology, USA
Naveen Verma, Princeton University, USA

Plenary Sessions

PL1 - Plenary 1

Session Chairs: Brian Ginsburg (Texas Instruments), Katsura Miyashita (Toshiba)

PL1.1 (Plenary) - Silicon is Greener: Why Innovation in Circuits is Needed for Sustainability	Jennifer Lloyd, Analog Devices, USA
PL1.2 (Plenary) - 5G Evolution and 6G	Takehiro Nakamura, NTT Docomo, Japan

PL2 - Plenary 2

Session Chairs: Tomas Palacios (MIT), Yusuke Oike (Sony Semiconductor Solutions)

PL2.1 (Plenary) - The Future of Compute: How the Data Transformation is Reshaping VLSI	Michael Mayberry, Intel, USA
PL2.2 (Plenary) - Empowering Next-Generation Applications through FLASH Innovation	Shigeo (Jeff) Ohshima, Kioxia, Japan

Joint Focus Sessions

JFS1 - Silicon Photonics	
Session Chairs: Ted Letavic (GlobalFoundries), Bryan Casper (Intel), Mitsuru Takenaka (University of Tokyo), Hisakatsu Yamaguchi (Fujitsu Laboratories)	
JFS1.1 (Invited) - TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s Optical I/O	Chen Sun, Ayar Labs, USA
JFS1.2 (Invited) - High-Temperature Operation of Chip-Scale Silicon-Photonic Transceiver	Daisuke Okamoto, PETRA, Japan
JFS1.3 - A Monolithically Integrated Silicon Photonics 8×8 Switch in 90nm SOI CMOS	Jonathan Proesel, IBM T. J. Watson Research Center, USA
JFS1.4 - III/V-on-Bulk-Si Technology for Commercially Viable Photonics-Integrated VLSI	Dongjae Shin, Samsung Advanced Institute of Technology, Republic of Korea
JFS1.5 - O-Band GeSi Quantum-Confined Stark Effect Electro-Absorption Modulator Integrated in a 220nm Silicon Photonics Platform	Clement Porret, imec, Belgium
JFS2 - 5G/mm-Wave	
Session Chairs: Kamel Benaissa (Texas Instruments), Amin Arbabian (Stanford University), Aaron Thean (National University of Singapore), Wei Deng (Tsinghua University)	
JFS2.1 (Invited) - Hardware-Software Co-integration for Configurable 5G mmWave Systems	Alberto Valdes-Garcia, IBM, USA
JFS2.2 (Invited) - Beyond 5G & Technologies : A Cross-Domain Vision	Eric Mercier, Université Grenoble Alps, CEA-Leti, France
JFS2.3 - A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring 7nm EUV Process Technology	Minjung Jin, Samsung Electronics, Republic of Korea
JFS2.4 - Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture	Chen Sun, National University of Singapore, Singapore
JFS2.5 - FinFET with Contact Over Active-Gate for 5G Ultra-Wideband Applications	Ali Razavieh, GlobalFoundries, USA
JFS2.6 - An RF Transceiver with Full Digital Interface Supporting 5G New Radio FR1 with 3.84Gbps DL/1.92Gbps UL and Dual-Band GNSS in 14nm FinFET CMOS	Sangwook Han, Samsung Electronics, Republic of Korea
JFS2.7 - A 1.96Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems	Chen-Chien Kao, National Taiwan University, Taiwan
JFS3 - STCO/DTCO	
Session Chairs: Seung-Chul Song (Qualcomm Technologies), Keiichi Maekawa (Renesas Electronics)	
JFS3.1 (Invited) - Heterogeneous System-Level Package Integration – Trends and Challenges	Frank Lee, TSMC, Taiwan
JFS3.2 (Invited) - Can We Ever Get to a 100nm Tall Library? Power Rail Design for 1nm Technology Node	Victor Moroz, Synopsys, USA
JFS3.3 - Buried Powered SRAM DTCO and System-Level Benchmarking in N3	Shairfe Salahuddin, imec, Belgium
JFS3.4 - Local Variation-Aware Transistor Design through Comprehensive Analysis of Various Vdd/Temperatures Using Sub-7nm Advanced FinFET Technology	Soyoun Kim, Samsung Electronics, Republic of Korea
JFS4 - Devices and Circuits for AI/ML	
Session Chairs: Edith Beigne (Facebook), Vijay Narayanan (IBM), Nicky Lu (Etron Technology), Huaqiang Wu (Tsinghua University)	
JFS4.1 - SOT-MRAM Based Analog in-Memory Computing for DNN Inference	Jonas Doevenspeck, imec, ESAT-Katholieke Universiteit Leuven, Belgium
JFS4.2 - Compact Probabilistic Poisson Neuron Based on Back-Hopping Oscillation in STT-MRAM for All-Spin Deep Spiking Neural Network	Ming-Hung Wu, National Chiao Tung University, Taiwan
JFS4.3 - An All-Weights-on-Chip DNN Accelerator in 22nm ULL Featuring 24×1 Mb eRRAM	Zhehong Wang, University of Michigan, USA
JFS4.4 - PNPU: A 146.52TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping	Sangyeob Kim, Korea Advanced Institute of Science and Technology, Republic of Korea
JFS4.5 - A Mixed-Signal Time-Domain Generative Adversarial Network Accelerator with Efficient Subthreshold Time Multiplier and Mixed-signal On-chip Training for Low Power Edge	Zhengyu Chen, Northwestern University, USA
JFS5 - Heterogeneous Integration	
Session Chairs: Carlos Tokunaga (Intel), Greg Yeric (Arm), Masanao Yamaoka (Hitachi), Tetsu Tanaka (Tohoku University)	
JFS5.1- Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry: Multi-Tier Complementary Carbon Nanotube Logic and Resistive RAM at a 130 nm Node	Tathagata Srimani, Massachusetts Institute of Technology, USA
JFS5.2 - A 1.8Gb/s/pin 16Tb NAND Flash Memory Multi-Chip Package with F-Chip of Toggle 4.0 Specification for High Performance and High Capacity Storage Systems	Daehoon Na, Samsung Electronics, Republic of Korea
JFS5.3 - A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-g Measurement Capability and Low Bias Instability	Xiaoliang Li, Carnegie Mellon University, USA
JFS5.4 - A 3D-Stacked Cortex-M0 SoC with 20.3Gbps/mm2 7.1mW/mm2 Simultaneous Wireless Inter-Tier Data and Power Transfer	Benjamin Fletcher, University of Southampton, United Kingdom
JFS5.5 - Heterogeneous Power Delivery for 7nm High-Performance Chiplet-Based Processors Using Integrated Passive Device and In-Package Voltage Regulator	Alan Roth, TSMC, USA
DEMO SESSION	
Session Chairs: Rob Aitken (Arm), Vijay Narayanan (IBM), Tomohiro Takahashi (Sony Semiconductor Solutions), Koji Hamada (Micron) *5-minute videos by participating authors*	
CB1.4 - 1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-Chip with Dynamic Incremental-SAR Acquisition	Jun Wang, University of California San Diego, USA
CB1.5 (Invited) - High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at 11.72µm Pitch for Neuronal Network Analysis	Yuri Kato, Sony Semiconductor Solutions, Japan
CB2.1 (Invited) - A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR	Tuan Thanh Ta, Toshiba, Japan
CB3.4 - A 0.72nW, 1Sample/s Fully Integrated pH Sensor with 65.8LSB/pH Sensitivity	Yihan Zhang, Columbia University, USA
CC2.3 - Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting	Massimo Alioto, National University of Singapore, Singapore
CP3.6 - A Domino Bootstrapping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 96% High Efficiency	Hsuan-Yu Chen, National Chiao Tung University, Taiwan
JFS1.4 - III/V-on-Bulk-Si Technology for Commercially Viable Photonics-Integrated VLSI	Dongjae Shin, Samsung Advanced Institute of Technology, Republic of Korea
JFS2.1 (Invited) - Hardware-Software Co-integration for Configurable 5G mmWave Systems	Alberto Valdes-Garcia, IBM, USA
JFS5.3 - A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-g Measurement Capability and Low Bias Instability	Xiaoliang Li, Carnegie Mellon University, USA
TM2.2 - A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing	Weier Wan, Stanford University, USA
TN1.3 - Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFET for Advanced Hardware Security	Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China

Technology Sessions

THL - Highlight Session

Session Chairs: Gosia Jurczak (Lam Research), Munehiro Tada (NEC)

THL.1 - 5G and AI Integrated High Performance Mobile SoC Process-Design Co-Development and Production with 7nm EUV FinFET Technology	Jie Deng, Qualcomm Technologies, USA
THL.2 - GaN and Si Transistors on 300mm Si(111) enabled by 3D Monolithic Heterogeneous Integration	Han Wui Then, Intel, USA
THL.3 - An Optically Sampled ADC in 3D Integrated Silicon-Photonics/65nm CMOS	Nandish Mehta, University of California, Berkeley, USA
THL.4 - A Monolithic 3D Integration of RRAM Array with Oxide Semiconductor FET for In-Memory Computing in Quantized Neural Network AI Applications	Jixuan Wu, University of Tokyo, Japan
THL.5 - Improved Air Spacer Co-Integrated with Self-Aligned Contact (SAC) and Contact Over Active Gate (COAG) for Highly Scaled CMOS Technology	Kangguo Cheng, IBM, USA
THL.6 - Buried Power Rail Integration with Si FinFETs for CMOS Scaling Beyond the 5nm Node	Anshul Gupta, imec, Belgium

TC1 - Advanced Si CMOS Devices

Session Chairs: Paul Grudowski (NXP Semiconductors), Yuri Masuoka (Samsung Electronics)

TC1.1 - Enabling Multiple-Vt Device Scaling for CMOS Technology Beyond 7nm Node	Vincent Chang, TSMC, Taiwan
TC1.2 - 7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing	Sylvain Barraud, CEA-Leti-MINATEC, France
TC1.3 - Cold CMOS as a Power-Performance-Reliability Booster for Advanced FinFETs	H. L. Chiang, TSMC, Taiwan
TC1.4 - All-Operation-Regime Characterization and Modeling of Drain Current Variability in Junctionless and Inversion-Mode FDSOI Transistors	Daphnée Bosch, CEA-Leti-MINATEC, France

TC2 - Ge and SiGe Devices

Session Chairs: Benjamin Colombeau (Applied Materials), Yee Chia Yeo (TSMC)

TC2.1 - Surface Ga-boosted Boron-doped $Si_{0.5}Ge_{0.5}$ using In-situ CVD Epitaxy: Achieving 1.1 × $10^{21}cm^{-3}$ Active Doping Concentration and 5.7× 10^{-10} Ω-cm^2 Contact Resistivity	Haiwen Xu, National University of Singapore, Singapore
TC2.2 - Addressing Key Challenges for SiGe-pFin Technologies: Fin Integrity, Low-D_{it} Si-cap-free Gate Stack and Optimizing the Channel Strain	Hiroaki Arimura, imec, Belgium
TC2.3 - First Demonstration of 4-Stacked $Ge_{0.915}Sn_{0.085}$ Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels	Yu-Shiang Huang, National Taiwan University, Taiwan
TC2.4 - Vertical Heterojunction $Ge_{0.92}Sn_{0.08}$/Ge GAA Nanowire pMOSFETs: Low SS of 67mV/dec, Small DIBL of 24mV/V and Highest $G_{m,ext}$ of 870μS/μm	Mingshan Liu, Forschungszentrum Juelich, Germany
TC2.5 - Structural and Electrical Demonstration of SiGe Cladded Channel for PMOS Stacked Nanosheet Gate-All-Around Devices	Shogo Mochizuki, IBM Research, USA

TC3 - Advanced Processing

Session Chairs: Yue Liang (Nvidia), Takaaki Tsunomura (Tokyo Electron)

TC3.1 - Materials Technology Co-Optimization of Self-Aligned Gate Contact for Advanced CMOS Technology Nodes	Ashish Pal, Applied Materials, USA
TC3.2 - Selective Enablement of Dual Dipoles for Near Bandedge Multi-V_t Solution in High Performance FinFET and Nanosheet Technologies	Ruqiang Bao, IBM Research, USA
TC3.3 - Composite Interconnects for High-Performance Computing Beyond the 7nm Node	Suketu Parikh, Applied Materials, USA
TC3.4 - Record Low Contact Resistivity to Ge:B ($8.1x10^{-10}$Ω-cm^2) and GeSn:B ($4.1x10^{-10}$Ω-cm^2) with Optimized [B] and [Sn] by In-situ CVD Doping	Fang-Liang Lu, National Taiwan University, Taiwan
TC3.5 - High Quality N+/P Junction of Ge Substrate Prepared by Initiated CVD Doping Process	Jaehwan Kim, Korea Advanced Institute of Science and Technology, Republic of Korea
TC3.6 - Ultra-low ρ_c Extraction for Recessed and Non-Recessed Contacts: Generalized Transmission Line Model	Jishen Zhang, National University of Singapore, Singapore

TF1 - FeFETs

Session Chairs: Suman Datta (University of Notre Dame), Byoung-Hun Lee (Gwangju Institute of Science and Technology)

TF1.1 - FeFET Memory Featuring Large Memory Window and Robust Endurance of Long-Pulse Cycling by Interface Engineering Using High-k AlON	Chi-Yu Chan, National Tsing Hua University, Taiwan
TF1.2 - Re-Examination of V_{th} Window and Reliability in HfO_2 FeFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation	Reika Ichihara, Kioxia, Japan
TF1.3 - Hot Electrons as the Dominant Source of Degradation for Sub-5nm HZO FeFETs	Ava Tan, University of California, Berkeley, USA
TF1.4 - A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation	Kai Ni, Rochester Institute of Technology, USA
TF1.5 - Asymmetric Polarization Response of Electrons and Holes in Si FeFETs: Demonstration of Absolute Polarization Hysteresis Loop and Inversion Hole Density Over $2×10^{13}$ cm^{-2}	Kasidit Toprasertpong, University of Tokyo, Japan

TF2 - Ferroelectric Memory and Capacitors

Session Chairs: Nirmal Ramaswamy (Micron), Shosuke Fujii (Kioxia)

TF2.1 - SoC Compatible 1T1C FeRAM Memory Array Based on Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$	Jun Okuno, Sony Semiconductor Solutions, Japan
TF2.2 - A Novel Dual Ferroelectric Layer Based MFMFIS FeFET with Optimal Stack Tuning Toward Low Power and High-Speed NVM for Neuromorphic Applications	Tarek Ali, Fraunhofer IPMS Center Nanoelectronic Technologies, Germany
TF2.3 - Improved State Stability of HfO_2 Ferroelectric Tunnel Junction by Template-Induced Crystallization and Remote Scavenging for Efficient In-Memory Reinforcement Learning	Shosuke Fujii, Kioxia, Japan
TF2.4 - Nanosecond Laser Anneal (NLA) for Si-Implanted HfO_2 Ferroelectric Memories Integrated in Back-End Of Line (BEOL)	Laurent Grenouillet, CEA-Leti-MINATEC, France
TF2.5 - Fast Thermal Quenching on the Ferroelectric Al: HfO_2 Thin Film with Record Polarization Density and Flash Memory Application	Changhwan Choi, Hanyang University, Republic of Korea
TF2.6 - Multi-Probe Characterization of Ferroelectric/Dielectric Interface by C-V, P-V and Conductance Methods	Junkang Li, Purdue University, USA
TF2.7 - Probing the Evolution of Electrically Active Defects in Doped Ferroelectric HfO_2 During Wake-Up and Fatigue	Umberto Celano, imec, Belgium
TF2.8 - Atomic-Scale Imaging of Polarization Switching in an (Anti-)Ferroelectric Memory Material: Zirconia (ZrO_2)	Sarah Lombardo, MSE, Georgia Institute of Technology, USA

TH1 - 3D Packaging	
Session Chairs: Michael DeLaus (Analog Devices), Tetsu Tanaka (Tohoku University)	
TH1.1 - Low Temperature SoIC Bonding and Stacking Technology for 12/16-Hi High Bandwidth Memory (HBM)	C.H. Tsai, TSMC, Taiwan
TH1.2 - 3D Heterogeneous Package Integration of Air/Magnetic Core Inductor: 89%-Efficiency Buck Converter with Backside Power Delivery Network	Xiao Sun, imec, Belgium
TH1.3 - Bumpless Build Cube (BBCube): High-Parallelism, High-Heat-Dissipation and Low-Power Stacked Memory Using Wafer-Level 3D Integration Process	Norio Chujo, Tokyo Institute of Technology, IIR, WOW Alliance / Hitachi, Japan
TH1.4 - ExaNoDe: Combined Integration of Chiplets on Active Interposer with Bare Dice in a Multi-Chip-Module for Heterogeneous and Scalable High Performance Compute Nodes	Pierre-Yves Martinez, Université Grenoble Alpes, CEA-LIST, France
TH1.5 - Immersion in Memory Compute (ImMC) Technology	C.T. Wang, TSMC, Taiwan
TH1.6 - Low Temperature Cu/SiO_2 Hybrid Bonding with Metal Passivation	Demin Liu, National Chiao Tung University, Taiwan
TH2 - Semiconducting Oxides for 3D Integration	
Session Chairs: Willy Rachmady (Intel), Yoshitaka Sasago (Hitachi)	
TH2.1 - BEOL Compatible Dual-Gate Ultra Thin-Body W-Doped Indium-Oxide Transistor with I_{on}=370μA/μm, SS=73mV/dec and I_{on}/I_{off} ratio > $4x10^9$	Wriddhi Chakraborty, University of Notre Dame, USA
TH2.2 - Surrounding Gate Vertical-Channel FET with Gate Length of 40nm Using BEOL Compatible High-Thermal-Tolerance In-Al-Zn Oxide Channel	Hirokazu Fujiwara, Kioxia, Japan
TH2.3 - Amorphous IGZO TFTs featuring Extremely-Scaled Channel Thickness and 38nm Channel Length: Achieving Record High $G_{m,max}$ of 125 μS/μm at V_{DS} of 1V and I_{ON} of 350μA/μm	Subhranu Samanta, National University of Singapore, Singapore
TH3 - Si Technologies for 3D Integration	
Session Chairs: Bill En (AMD), Osbert Cheng (United Microelectronics)	
TH3.1 - First Monolithic Integration of 3D Complementary FET (CFET) on 300mm Wafers	Sujith Subramanian, imec, Belgium
TH3.2 - 3D Sequential Low Temperature Top Tier Devices Using Dopant Activation with Excimer Laser Anneal and Strained Silicon as Performance Boosters	Anne Vandooren, imec, Belgium
TH3.3 - 28nm FDSOI CMOS Technology (FEOL and BEOL) Thermal Stability for 3D Sequential Integration: Yield and Reliability Analysis	Camila Cavalcante, CEA-Leti, France
TH3.4 - First Demonstration of Low Temperature (≤500°C) CMOS Devices Featuring Functional RO and SRAM Bitcells toward 3D VLSI Integration	Claire Fenouillet-Beranger, CEA-Leti-MINATEC, France
TH3.5 - Flexible and Transparent BEOL Monolithic 3DIC Technology for Human Skin Adaptable Internet of Things Chips	Ming-Hsuan Kao, Taiwan Semiconductor Research Institute, Taiwan
TM1 - Memory - NAND/NOR/PCM	
Session Chairs: Jixin Yu (Western Digital), Deoksin Kil (SK Hynix Semiconductor)	
TM1.1 - An Extremely Scaled Hemi-Cylindrical (HC) 3D NAND Device with Large V_t Memory Window (>10V) and Excellent 100K Endurance	Pei-Ying Du, Macronix International, Taiwan
TM1.2 - An Approach to Embedding Traditional Non-Volatile Memories into a Deep Sub-Micron CMOS	Chia-Sheng Lin, TSMC, Taiwan
TM1.3 - A Vertical 2T NOR (V2T) Architecture to Enable Scaling and Low-Power Solutions for NOR Flash Technology	Hang-Ting Lue, Macronix International, Taiwan
TM1.4 - Understanding of Tunable Selector Performance in Si-Ge-As-Se OTS Devices by Extended Percolation Cluster Model Considering Operation Scheme and Material Design	Shoichi Kabuyanagi, Kioxia, imec, Japan
TM1.5 - A No-Verification Multi-Level-Cell (MLC) Operation in Cross-Point OTS-PCM	Nanbo Gong, IBM T. J. Watson Research Center, USA
TM1.6 - Si Incorporation Into AsSeGe Chalcogenides for High Thermal Stability, High Endurance and Extremely Low V_{th} Drift 3D Stackable Cross-Point Memory	Huai-Yu Cheng, Macronix International, Taiwan
TM2 - Memory - RRAM	
Session Chairs: Shimeng Yu (Georgia Institute of Technology), Koji Hamada (Micron)	
TM2.1 - A SiO_x RRAM-Based Hardware with Spike Frequency Adaptation for Power-Saving Continual Learning in Convolutional Neural Networks	Irene Munoz-Martin, Politecnico di Milano, Italy
TM2.2 - A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing	Weier Wan, Stanford University, USA
TM2.3 - Industrially Applicable Read Disturb Model and Performance on Mega-Bit 28nm Embedded RRAM	Chang-Feng Yang, TSMC, Taiwan
TM3 - Memory - STT MRAM	
Session Chairs: Klaus Knobloch (Infineon), Masahiko Kanda (Toshiba Electronic Devices & Storage)	
TM3.1 - Scalability of Quad Interface p-MTJ for 1X nm STT-MRAM with 10ns Low Power Write Operation, 10 years Retention and Endurance > 10^{11}	Sadahiko Miura, Tohoku University, Japan
TM3.2 - Reliability Demonstration of Reflow Qualified 22nm STT-MRAM for Embedded Memory Applications	Chia-Yu Wang, TSMC, Taiwan
TM3.3 - Fast Switching of STT-MRAM to Realize High Speed Applications	Tae Young Lee, GlobalFoundries, Singapore
TM3.4 - A Reliable TDDB Lifetime Projection Model Verified Using 40Mb STT-MRAM Macro at Sub-ppm Failure Rate to Realize Unlimited Endurance for Cache Applications	Vinayak Bharat Naik, GlobalFoundries, Singapore
TMFS - MRAM Future - Opportunities Beyond STT	
Session Chairs: Franck Arnaud (STMicroelectronics), Hang-Ting Lue (Macronix International)	
TMFS.1 (Invited) - Recent Progresses in STT-MRAM and SOT-MRAM for Next Generation MRAM	Tetsuo Endoh, Tohoku University, Japan
TMFS.2 (Invited) - Magnetic Random Access Memories (MRAM) Beyond Information Storage	Ricardo Sousa, Université Grenoble Alpes / CEA / CNRS, Spintec, France
TMFS.3 - CMOS Compatible Process Integration of SOT-MRAM with Heavy-Metal Bi-Layer Bottom Electrode and 10ns Field-Free SOT Switching with STT Assist	Noriyuki Sato, Intel, USA
TMFS.4 - Deterministic and Field-Free Voltage-Controlled MRAM for High Performance and Low Power Applications	Yueh Chang Wu, imec, Belgium

TN1 - New Devices and Applications	
Session Chairs: Peide Ye (Purdue University), Masaharu Kobayashi (University of Tokyo)	
TN1.1 - Hair-Like Nanostructure Based Ion Detector by 16nm FinFET Technology	Chien-Ping Wang, National Tsing Hua University, Taiwan
TN1.2 - Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry	Chia-Che Chung, National Taiwan University, Taiwan
TN1.3 - Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFET for Advanced Hardware Security	Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China
TN1.4 - A Bias and Correlation-Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking	Kai Ni, Rochester Institute of Technology, USA
TN1.5 - 1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy	Xu Bai, NEC, Japan
TN1.6 - Proposal and Experimental Demonstration of Reservoir Computing Using $Hf_{0.5}Zr_{0.5}O_2$/Si FeFETs for Neuromorphic Applications	Eishin Nako, University of Tokyo, Japan
TN1.7 - High On-Current 2D nFET of 390μA/μm at V_{DS} = 1V using Monolayer CVD MoS_2 Without Intentional Doping	Ang-Sheng Chou, TSMC, Taiwan
TN1.8 - Ultrahigh Responsivity and Tunable Photogain BEOL Compatible MoS_2 Phototransistor Array for Monolithic 3D Image Sensor with Block-Level Sensing Circuits	Chih-Chao Yang, Taiwan Semiconductor Research Institute, Taiwan
TN1.9 - GaN PMIC Opportunities: Characterization of Analog and Digital Building Blocks in a 650V GaN-on-Si Platform	Wan Lin Jiang, University of Toronto, Canada
TN2 - Quantum Computing	
Session Chairs: Maud Vinet (CEA-Leti), Huaqiang Wu (Tsinghua University)	
TN2.1 - Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures Down to 100mK for Quantum Computing	Bruna Paz, CEA-Leti-MINATEC, France
TN2.2 - Toward Long-Coherence-Time Si Spin Qubit: The Origin of Low-Frequency Noise in Cryo-CMOS	Hiroshi Oka, National Institute of Advanced Industrial Science and Technology, Japan

Circuits Sessions

CA1 - Machine Learning

Session Chairs: Zhengya Zhang (University of Michigan), Sugako Otani (Renesas Electronics)

CA1.1 - A 3.0 TFLOPS 0.62V Scalable Processor Core for High Compute Utilization AI Training and Inference	Sae Kyu Lee, IBM T. J. Watson Research Center, USA
CA1.2 - A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS	Phil Knag, Intel, USA
CA1.3 - An Ultra-Low Latency 7.8-13.6 pJ/b Reconfigurable Neural Network-Assisted Polar Decoder with Multi-Code Length Support	Chieh-Fang Teng, National Taiwan University, Taiwan
CA1.4 - A 4.45ms Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices	Dongseok Im, Korea Advanced Institute of Science and Technology, Republic of Korea
CA1.5 - A 3mm^2 Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception Using Parallel Gibbs Sampling in 16nm	Glenn G. Ko, Harvard University, USA

CA2 - Visual Processing & AI

Session Chairs: Brian Zimmer (Nvidia), Yasuki Tanabe (Toshiba Electronic Devices & Storage)

CA2.1 - A 170μW Image Signal Processor Enabling Hierarchical Image Recognition for Intelligence at the Edge	Hyochan An, University of Michigan, USA
CA2.2 - A 0.05pJ/Pixel 70fps FHD 1Meps Event-Driven Visual Data Processing Unit	Somnath Paul, Intel, USA
CA2.3 - A 65nm Image Processing SoC Supporting Multiple DNN Models and Real-Time Computation-Communication Trade-Off via Actor-Critical Neuro-Controller	Ningyuan Cao, Georgia Institute of Technology, USA
CA2.4 - A Ray-Casting Accelerator in 10nm CMOS for Efficient 3D Scene Reconstruction in Edge Robotics and Augmented Reality Applications	Steven Hsu, Intel, USA
CA2.5 - A 1200x1200 8-Edges/Vertex FPGA-Based Motion-Planning Accelerator for Dual-Arm-Robot Manipulation Systems	Takashi Oshima, Hitachi, Japan

CA3 - Digital Systems

Session Chairs: Arijit Raychowdhury (Georgia Institute of Technology), Vinayak Honkote (Intel)

CA3.1 (Invited) - Managing Chip Design Complexity in the Domain-Specific SoC Era	Yunsup Lee, SiFive, USA
CA3.2 - 17.3GCUPS Pruning-Based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing	Xiao Wu, University of Michigan, Sequal, USA
CA3.3 - A Probabilistic Self-Annealing Compute Fabric based on 560 Hexagonally Coupled Ring Oscillators for Solving Combinatorial Optimization Problems	Ibrahim Ahmed, University of Minnesota, USA
CA3.4 - MANA: A Monolithic Adiabatic iNtegration Architecture Microprocessor Using 1.4zJ/op Superconductor Josephson Junction Devices	Christopher Ayala, Yokohama National University, Japan
CA3.5 - 32GHz 6.5mW Gate-Level-Pipelined 4-bit Processor using Superconductor Single-Flux-Quantum Logic	Koki Ishida, Kyushu University, Japan

CB1 - Biomedical Sensors

Session Chairs: Carolina Mora Lopez (imec), Takashi Tokuda (Tokyo Institute of Technology)

CB1.1 - A 785nW Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring	Peng Wang, University of Virginia, USA
CB1.2 - An Artificial Iris ASIC with High Voltage Liquid Crystal Driver, 10nA Light Range Detector and 40nA Blink Detector for LCD Flicker Removal	Bogdan Raducanu, imec, Belgium
CB1.3 - A Packaged Ingestible Bio-Pill with 15-Pixel Multiplexed Fluorescence Nucleic-Acid Sensor and Bi-Drectional Wireless Interface for In-vivo Bio-Molecular Sensing	Chengjie Zhu, Princeton University, USA
CB1.4 - 1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-Chip with Dynamic Incremental-SAR Acquisition	Jun Wang, University of California San Diego, USA
CB1.5 (Invited) - High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at 11.72μm Pitch for Neuronal Network Analysis	Yuri Kato, Sony Semiconductor Solutions, Japan

CB2 - Image Sensor & Imaging Techniques

Session Chairs: Neale Dutton (STMicroelectronics), Tomohiro Takahashi (Sony Semiconductor Solutions)

CB2.1 (Invited) - A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR	Tuan Thanh Ta, Toshiba, Japan
CB2.2 - A 36-Channel SPAD-Integrated Scanning LiDAR Sensor with Multi-Event Histogramming TDC and Embedded Interference Filter	Hyeongseok Seo, Sungkyunkwan University, Republic of Korea
CB2.3 - A 3.0μW@5fps QQVGA Self-Controlled Wake-Up Imager with On-Chip Motion Detection, Auto-Exposure and Object Recognition	Arnaud Verdant, CEA-Leti-MINATEC, France
CB2.4 - A Low Noise Read-Out IC with Gate Driver for Full Front Display Area Optical Fingerprint Sensors	Yongil Kwon, Samsung Electronics, Republic of Korea
CB2.5 - An Always-On 4x Compressive VGA CMOS Imager with 51pJ/pixel and >32dB PSNR	Wenda Zhao, The University of Texas at Austin, USA

CB3 - Physical Sensors

Session Chairs: Loic Sibeud (CEA-Leti), Yutaka Hirose (Panasonic)

CB3.1 - A 50.7dB-DR Finger-Resistance Extractable Multi-Touch Sensor IC Achieving Finger-Classification Accuracy of 97.7% on 6.7-inch Capacitive Touch Screen Panel	Tae-Gyun Song, Korea Advanced Institute of Science and Technology, Republic of Korea
CB3.2 - A Pressure Sensing System with ±0.75mmHg (3σ) Inaccuracy for Battery-Powered Low Power IoT Applications	Seok Hyeon Jeong, University of Michigan, USA
CB3.3 - A 200μW Eddy Current Displacement Sensor with 6.7nm$_{rms}$ Resolution	Matheus Pimenta, Cypress Semiconductor, Ireland
CB3.4 - A 0.72nW, 1Sample/s Fully Integrated pH Sensor with 65.8LSB/pH Sensitivity	Yihan Zhang, Columbia University, USA
CB3.5 - An 8-Element Frequency-Selective Acoustic Beamformer and Bitstream Feature Extractor with 60 Mel-Frequency Energy Features Enabling 95% Speech Recognition Accuracy	Seungjong Lee, University of Michigan, USA

CB4 - Front-Ends for Sensor Interfaces

Session Chairs: Samira Zali Asl (Ferric), Minkyu Je (KAIST)

CB4.1 - A −105dB THD 88dB-SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation	Jiannan Huang, University of California San Diego, USA
CB4.2 - A 4.3fJ/conversion-step 6440μm^2 All-Dynamic Capacitance-to-Digital Converter with Energy-Efficient Charge Reuse	Haoming Xin, Eindhoven University of Technology, Netherlands
CB4.3 - A 0.5V, 6.2μW, 0.059mm^2 Sinusoidal Current Generator IC with 0.088% THD for Bio-Impedance Sensing	Kwantae Kim, Korea Advanced Institute of Science and Technology, Republic of Korea
CB4.4 - A Portable NMR System with 50kHz IF, 10μs Dead Time, and Frequency Tracking	Sungjin Hong, University of Texas at Austin, USA

CC1 - Circuits for Security and Safety	
Session Chairs: Rob Aitken (Arm), Mototsugu Hamada (University of Tokyo)	
CC1.1 - A Performance-Flexible Energy-Optimized Automotive-Grade Cortex-R4F SoC through combined AVS/ABB/Bias-in-Memory-Array Closed-Loop Regulation in 28nm FD-SOI	Ricardo Gomez Gomez, STMicroelectronics, France
CC1.2 - A SCA-Resistant AES Engine in 14nm CMOS with Time/Frequency-Domain Leakage Suppression Using Non-linear Digital LDO Cascaded with Arithmetic Countermeasures	Raghavan Kumar, Intel, USA
CC1.3 - A 0.26% BER, 10^{28} Challenge-Response Machine-Learning Resistant Strong-PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection	Vikram Suresh, Intel, USA
CC1.4 - A 435MHz, 2.5Mbps/W Side-Channel-Attack Resistant Crypto-Processor for Secure RSA-4K Public-Key Encryption in 14nm CMOS	Raghavan Kumar, Intel, USA
CC2 - Adaptive Clocking and Power Delivery	
Session Chairs: Paul Whatmough (Arm), Makoto Takamiya (University of Tokyo)	
CC2.1 - A Proactive Voltage-Droop-Mitigation System in a 7nm Hexagon™ Processor	Vijay Kiran Kalyanam, Qualcomm Technologies, USA
CC2.2 - An Autonomous Reconfigurable Power Delivery Network (RPDN) for Many-Core SoCs Featuring Dynamic Current Steering	Khondker Ahmed, Intel, USA
CC2.3 - Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting	Massimo Alioto, National University of Singapore, Singapore
CC2.4 - UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in Designs with Large Clock Distribution Delays in 65nm CMOS	Xun Sun, University of Washington, USA
CC2.5 - Low-Clock-Power Digital Standard Cell IPs for High-Performance Graphics/AI Processors in 10nm CMOS	Steven Hsu, Intel, USA
CD1 - High-Speed Data Converters	
Session Chairs: Stacy Ho (MediaTek), Tomohiro Nezuka (MIRISE Technologies)	
CD1.1 - A 1MS/s to 1GS/s Ringamp-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm	Benjamin Hershberg, imec, Belgium
CD1.2 - A 10-bit 100MS/s SAR ADC with Always-on Reference Ripple Cancellation	Xiyuan Tang, University of Texas at Austin, USA
CD1.3 - An 8b 1GS/s 2.55mW SAR-Flash ADC with Complementary Dynamic Amplifiers	Dong-Ryeol Oh, Korea Advanced Institute of Science and Technology,
CD1.4 - A 177mW 10GS/s NRZ DAC with Switching-Glitch Compensation Achieving > 64dBc SFDR and < -77dBc IM3	Hung-Yi Huang, National Cheng Kung University, Taiwan
CD1.5 - A Compact 14GS/s 8-bit Switched-Capacitor DAC in 16nm FinFET CMOS	Pietro Caragiulo, Stanford University, USA
CD2 - Data Converter Techniques	
Session Chairs: Ewout Martens (imec), Mitsuya Fukazawa (Renesas Electronics)	
CD2.1 - A 440µW, 109.8dB DR, 106.5dB SNDR Discrete-Time Zoom ADC with a 20kHz BW	Efraïm Eland, Delft University of Technology, Netherlands
CD2.2 - A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved Second-Order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS	Dongyang Jiang, University of Macau, Macao
CD2.3 - A 10.4mW 50MHz-BW 80dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp	Kai Xing, University of Macau, China
CD2.4 - A 1GS/s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9dB FoMs	Yifan Lyu, MICAS-Katholieke Universiteit Leuven, Belgium
CD2.5 - A SAR ADC with Reduced kT/C Noise by Decoupling Noise PSD and BW	Zhelu Li, Zhejiang University, University of Texas at Austin, China
CF1 - Advanced PLLs	
Session Chairs: Christoph Sandner (Infineon), Kenichi Okada (Tokyo Institute of Technology)	
CF1.1 - Embedded PLL Phase Noise Measurement Based on a PFD/CP MASH 1-1-1 ΔΣ Time-to-Digital Converter in 7nm CMOS	Mao-Hsuan Chou, TSMC, Taiwan
CF1.2 - A Fast Locking 5.8−7.2 GHz Fractional-N Synthesizer with Sub-2µs Settling Time in 22nm FDSOI	Jeffrey Prinzie, Katholieke Universiteit Leuven, Belgium
CF1.3 - A 4GHz 0.73ps$_{rms}$-Integrated-Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring PLL with a Jitter-Tracking DLL-Assisted DTC	Jaehong Jung, Samsung Electronics, Republic of Korea
CF1.4 - A 3.3-GHz 101fs$_{rms}$-Jitter, −250.3dB FOM Fractional-N DPLL with Phase Error Detection Accomplished in Fully Differential Voltage Domain	Lianbo Wu, ETH Zürich, Switzerland
CF1.5 - A 3.2-to-3.8GHz Calibration-Free Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving −66dBc Worst-Case In-Band Fractional Spur	Masaru Osada, University of Tokyo, Japan
CF2 - RF & mm-Wave Circuits	
Session Chairs: Mike Chen (University of Southern California), Ho-Jin Song (POSTECH)	
CF2.1 - A 29% PAE 1.5bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked PLL	Yuncheng Zhang, Tokyo Institute of Technology, Japan
CF2.2 - A 28GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation	Jian Pang, Tokyo Institute of Technology, Japan
CF2.3 - A 293/440 GHz Push-Push Double Feedback Oscillators with 5.0/-3.9dBm Output Power and 2.9/0.6% DC-to-RF Efficiency in 65nm CMOS	Dzuhri Radityo Utomo, Korea Advanced Institute of Science and Technology, Republic of Korea
CF2.4 - A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-Gmax Gain Boosting Technique	Dae-Woong Park, imec, Republic of Korea
CF2.5 - 315GHz Self-Synchronizing Minimum Shift Keying Receiver in 65nm CMOS	Ibukun Momson, University of Texas at Dallas, USA
CF3 - IoT and Wireless Receivers	
Session Chairs: Alireza Zolfaghari (Broadcom), Chun-Huat Heng (National University of Singapore)	
CF3.1 - SamurAI: a 1.7MOPS-36GOPS Adaptive Versatile IoT Node with 15,000x Peak-to-Idle Power Reduction, 207ns Wake-Up Time and 1.3TOPS/W ML Efficiency	Ivan Miro-Panades, Université Grenoble Alpes, CEA, LIST, France
CF3.2 (Invited) - Industrial IoT with Crystal-Free Mote-on-Chip	Thomas Watteyne, Inria, France
CF3.3 - A Multichannel, MEMS-Less −99dBm 260nW Bit-level Duty Cycled Wakeup Receiver	Anjana Dissanayake, University of Virginia, USA
CF3.4 - A 4.4µW −92/−90.3dBm Sensitivity Dual-mode BLE/Wi-Fi Wake-Up Receiver	Po-Han Peter Wang, University of California San Diego, USA
CF3.5 - A 920MHz 16-FSK Receiver Achieving a Sensitivity of −103dBm at 0.6mW via an Integrated N-Path Filter Bank	Ali Nikoofard, University of California San Diego, USA
CF4 - Low Power Oscillators	
Session Chairs: Danielle Griffith (Texas Instruments), Yoji Bando (Socionext)	
CF4.1 - A 8.7ppm/°C, 694nW, One-Point Calibrated RC Oscillator Using a Nonlinearity-Aware Dual Phase-Locked Loop and DSM-Controlled Frequency-Locked Loops	Giorgio Cristiano, ETH Zürich, Switzerland
CF4.2 - A 0.5V 560kHz 18.8fJ/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop	Daniel Truesdell, University of Virginia, USA
CF4.3 - A 0.9pJ/cycle 8ppm/°C DFLL-based Wakeup Timer Enabled by a Time-Domain Trimming and an Embedded Temperature Sensing	Ming Ding, imec, Netherlands

CM1 - Advanced SRAM Design	
Session Chairs: Igor Arsovski (Marvell), Tsung-Yung Jonathan Chang (TSMC)	
CM1.1 - A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 175mV VMIN Reduction with Negligible Power Overhead	Zheng Guo, Intel, USA
CM1.2 - A 29.2Mb/mm² Ultra High Density SRAM Macro Using 7nm FinFET Technology with Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit	Yoshisato Yokoyama, Renesas Electronics, Japan
CM1.3 - Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1R1W 8T-bitcell SRAM in 10nm FinFET CMOS	Jaydeep Kulkarni, Intel, USA
CM1.4 - 2X-Bandwidth Burst 6T-SRAM for Memory Bandwidth Limited Workloads	Charles Augustine, Intel, USA
CM1.5 - A 7nm Fin-FET 4.04-Mb/mm² TCAM with Improved Electromigration Reliability Using Far-Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier	Makoto Yabuuchi, Renesas Electronics, Japan
CM2 - Emerging Memory Design	
Session Chairs: Seung Kang (Qualcomm Technologies), Makoto Miyamura (NEC)	
CM2.1 - A 14.7Mb/mm^2 28nm FDSOI STT-MRAM with Current Starved Read Path, 52Ω/Sigma Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference	El Mehdi Boujamaa, Arm, France
CM2.2 - Dual-Port Field-Free SOT-MRAM Achieving 90MHz Read and 60MHz Write Operations Under 55nm CMOS Technology and 1.2V Supply Voltage	Masanori Natsui, Tohoku University, Japan
CM2.3 - A 28nm 1.5Mb Embedded 1T2R RRAM with 14.8 Mb/mm^2 Using Sneaking Current Suppression and Compensation Techniques	Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China
CM2.4 - A 22nm 96Kx144 RRAM Macro with a Self-Tracking Reference and a Low Ripple Charge Pump to Achieve a Configurable Read Window and a Wide Operating Voltage Range	Chung-Cheng Chou, TSMC, Taiwan
CM3 - Energy Efficient Memory Design	
Session Chairs: John Wuu (AMD), Kyomin Sohn (Samsung Electronics)	
CM3.1 - A 28nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation	Hoyoung Shin, Samsung Electronics, Republic of Korea
CM3.2 - A 65nm 16kb SRAM with 131.5pW Leakage at 0.9V for Wireless IoT Sensor Nodes	Shourya Gupta, University of Virginia, USA
CM3.3 - 1.03pW/b Ultra-Low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors	Jingcheng Wang, University of Michigan, USA
CM3.4 - Z-PIM: An Energy-Efficient Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision	Ji-Hoon Kim, Korea Advanced Institute of Science and Technology, Republic of Korea
CP1 - Amplifiers	
Session Chairs: Hylas Lam (Analog Devices), Kuan-Dar Chen (MediaTek)	
CP1.1 - A −107.8dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier	Huajun Zhang, Delft University of Technology, Netherlands
CP1.2 - An 8Ω, 1.4W, 0.0024% THD+N Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Mode Achieving Low Standby Quiescent Current of 660µA	Ji-Hun Lee, Korea Advanced Institute of Science and Technology, Republic of Korea
CP1.3 - Sample and Average Common-Mode Feedback in a 101nW Acoustic Amplifier	Rohit Rothe, University of Michigan, USA
CP1.4 - A 0.0046mm^2 6.7µW Three-Stage Amplifier Capable of Driving 0.5-to-1.9nF Capacitive Load with >0.68MHz GBW without Compensation Zero	Hongseok Shin, Korea Advanced Institute of Science and Technology, Republic of Korea
CP2 - Voltages References and Wireless Power	
Session Chairs: Patrick Mercier (University of California San Diego), Sung-Wan Hong (Sookmyung Women's University)	
CP2.1 - A Single-Trim Switched Capacitor CMOS Bandgap Reference with a 3σ Inaccuracy of +0.02%, -0.12% for Battery Monitoring Applications	Jun-Ho Boo, Sogang University, Republic of Korea
CP2.2 - A 0.25-V, 5.3-pW Voltage Reference with 25µV/°C Temperature Coefficient, 140µV/V Line Sensitivity and 2,200µm^2 Area in 180nm	Longyan Lin, National University of Singapore, Singapore
CP2.3 - A 6.78MHz Wireless Power Transfer System Enabling Perpendicular Wireless Powering with Efficiency Increase from 0.02% to 48.2% by Adaptive Magnetic Field Adder IC Integrating Shared Coupling Coefficient Sensor	Hao Qiu, University of Tokyo, Japan
CP2.4 - A 120-330V, Sub-µA, 4-Channel Driver for Microrobotic Actuators with Wireless-Optical Power Delivery and Over 99% Current Efficiency	Jan Rentmeister, Dartmouth College, USA
CP3 - Power Converters	
Session Chairs: Xin Zhang (IBM), Po-Hung Chen (National Chiao Tung University)	
CP3.1 - An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching	Dong Yan, University of Texas at Dallas, USA
CP3.2 - Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 65nm CMOS	Xun Sun, University of Washington, USA
CP3.3 - An N-Path Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting Achieving 13.9x Power Extraction Improvement	Loai Salem, University of California Santa Barbara, USA
CP3.4 - A 4V-0.55V Input Fully Integrated Switched-Capacitor Converter Enabling Dynamic Voltage Domain Stacking and Achieving 80.1% Average Efficiency	Tim Thielemans, MICAS-Katholieke Universiteit Leuven, Belgium
CP3.5 - A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency	Xiaosen Liu, Intel, USA
CP3.6 - A Domino Bootstrapping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 96% High Efficiency	Hsuan-Yu Chen, National Chiao Tung University, Taiwan
CW1 - Ultra-High-Speed Wireline	
Session Chairs: Jon Proesel (IBM), Jri Lee (National Taiwan University)	
CW1.1 - A 4x112 Gb/s ADC-DSP Based Multistandard Receiver in 7nm FinFET	Haidang Lin, Microsoft, USA
CW1.2 - A 25-50Gb/s 2.22pJ/b NRZ RX with Dual-Bank and 3-tap Speculative DFE for Microprocessor Application in 7nm FinFET CMOS	Yang You, IBM, USA
CW1.3 - A 4-to-18GHz Active Poly Phase Filter Quadrature Clock Generator with Phase Error Correction in 5nm CMOS	Wei-Chih Chen, TSMC, Taiwan
CW2 - Wireline Techniques	
Session Chairs: Parag Upadhyaya (Xilinx), C. Patrick Yue (Hong Kong University of Science and Technology)	
CW2.1 - A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ Calibration for Memory Interfaces	Yong-Un Jeong, Seoul National University, Republic of Korea
CW2.2 - A 0.1pJ/b/dB 28Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler	Moon-Chul Choi, Seoul National University, Republic of Korea
CW2.3 - Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20GS/s 5b ENOB Analog-to-Digital Converter and 5GHz Phase Interpolator	Sung-Jin Kim, Stanford University, USA
CW2.4 - A 28mW 32Gb/s/pin 16-QAM Single-Ended Transceiver for High-Speed Memory Interface	Jieqiong Du, University of California Los Angeles, USA

Workshops

WS1 Workshop - Analog Computing Technologies and Circuits for Efficient Machine Learning Hardware	
Organizers: Aridam Mallik (imec), Nadine Collaert (imec)	
WS1.1 - Prospects of Analog In-Memory Computing – An Overview	Boris Murmann, Stanford University, USA
WS1.2 - Designing Material Systems and Algorithms for Analog Computing	Robert L. Bruce, IBM Research, USA
WS1.3 - Monolithically Integrated RRAM-based Analog/ Mixed-Signal In-Memory Computing for Energy-Efficient Deep Learning	Jae-Sun Seo, Arizona State University, USA
WS1.4 - Compute-in-Memory Circuit and Device Technologies: Trends and Prospects	Jaydeep Kulkarni, University of Texas at Austin, USA
WS1.5 - Analog Computing for Machine Learning – An Ideal Case for Co-Optimization of System and Device Technology	Arindam Mallik, imec, Belgium
WS1.6 - System and Architecture Level Considerations in Leveraging Mixed-Signal Techniques for ML at the Edge	Mahesh Mehendale, Texas Instruments, USA
WS2 Workshop - Know Where You Are Going; Metrology In the New Age of Semiconductor Manufacturing	
Organizers: Tom Larson (Nova Measuring Instruments), Gosia Jurczak (Lam Research)	
WS2.1 - Introduction to Metrology Workshop	Tom Larson, Nova Measuring Instruments, USA
WS2.2 - Manufacturing Process Challenges and Requirements for Metrology in Semiconductor Memory Devices	Keiji Suzuki, Kioxia, Japan
WS2.3 - Metrology with Angstrom Accuracy Required by Logic IC Manufacturing – Challenges From R&D to High Volume Manufacturing and Solutions in the AI Era	Yi Hung Lin, TSMC, Taiwan
WS2.4 - Dimensional Metrology Overview, Trends and Upcoming C'hallenges	Philippe Leray, imec, Belgium
WS2.5 - Defect Inspection: A Trio of Trends for the 2020s	Mark Shirey, KLA, USA
WS2.6 - Enabling Modern Semiconductor Manufacturing With Materials Metrology	Kavita Shah, Nova Measuring Instruments, USA
WS2.7 - Opportunities and Challenges for Lab-based Characterization for Emerging Technologies	Markus Kuhn, Intel, USA
WS3 Workshop - Quantum Computers for Electrical Engineers	
Organizers: Maud Vinet (CEA-Leti), Iuliana Radu (imec)	
WS3.1 - 3D Integration and Challenges for Scaling	William Oliver, Massachusetts Institute of Technology, USA
WS3.2 - Superconducting Qubits: How Technology/ Processing/ Materials Impact Coherence Time and How Design Impacts Gate Fidelity	Doug McClure, IBM, USA
WS3.3 - Si Based Qubits: Technology and Material Impact on Performance	Iuliana Radu, imec, Belgium
WS3.4 - Architectures Challenges for Si Spin Qubits	Maud Vinet, CEA-Leti, France
WS3.5 - Cryogenic CMOS for Control of Transmon Qubits	Joseph Bardin, Google AI Quantum & University of Massachusetts Amherst, USA

Live Sessions

Monday June-15

PL1 - Plenary 1

SELECT June-15 08:00 PDT / June-15 17:00 CET / June-16 00:00 JST OR June-15 17:00 PDT / June-16 02:00 CET / June-16 09:00 JST (2 hours)

Session Chairs: Brian Ginsburg (Texas Instruments), Katsura Miyashita (Toshiba)

PL1.1 (Plenary) - Silicon is Greener: Why Innovation in Circuits is Needed for Sustainability	Jennifer Lloyd, Analog Devices, USA
PL1.2 (Plenary) - 5G Evolution and 6G	Takehiro Nakamura, NTT Docomo, Japan

EA1 Executive Session - Advanced CMOS (1)

June-15 10:00 PDT / June-15 19:00 CET / June-16 02:00 JST (1 hour)

Session Chairs: Paul Grudowski (NXP Semiconductors)

TC1.2 - 7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing	Sylvain Barraud, CEA-Leti-MINATEC, France
TC1.4 - All-Operation-Regime Characterization and Modeling of Drain Current Variability in Junctionless and Inversion-Mode FDSOI Transistors	Daphnée Bosch, CEA-Leti-MINATEC, France
TC2.2 - Addressing Key Challenges for SiGe-pFin Technologies: Fin Integrity, Low-D_{it} Si-cap-free Gate Stack and Optimizing the Channel Strain	Hiroaki Arimura, imec, Belgium
TC2.4 - Vertical heterojunction $Ge_{0.92}Sn_{0.08}$/Ge GAA Nanowire pMOSFETs: Low SS of 67mV/dec, Small DIBL of 24mV/V and Highest $G_{m,ext}$ of 870μS/μm	Mingshan Liu, Forschungszentrum JuElich, Germany
TC2.5 - Structural and Electrical Demonstration of SiGe Cladded Channel for PMOS Stacked Nanosheet Gate-All-Around Devices	Shogo Mochizuki, IBM Research, USA
TC3.1 - Materials Technology Co-Optimization of Self-Aligned Gate Contact for Advanced CMOS Technology Nodes	Ashish Pal, Applied Materials, USA
TC3.2 - Selective Enablement of Dual Dipoles for Near Bandedge Multi-V_t Solution in High Performance FinFET and Nanosheet Technologies	Ruqiang Bao, IBM Research, USA
TC3.3 - Composite Interconnects for High-Performance Computing Beyond the 7nm Node	Suketu Parikh, Applied Materials, USA
THL.5 - Improved Air Spacer Co-Integrated with Self-Aligned Contact (SAC) and Contact Over Active Gate (COAG) for Highly Scaled CMOS Technology	Kangguo Cheng, IBM, USA
THL.6 - Buried Power Rail Integration with Si FinFETs for CMOS Scaling Beyond the 5nm Node	Anshul Gupta, imec, Belgium

EA2 Executive Session - Sensor Systems

June-15 10:00 PDT / June-15 19:00 CET / June-16 02:00 JST (1 hour)

Session Chairs: Neale Dutton (STMicroelectronics)

CA2.1 - A 170μW Image Signal Processor Enabling Hierarchical Image Recognition for Intelligence at the Edge	Hyochan An, University of Michigan, USA
CA2.2 - A 0.05pJ/Pixel 70fps FHD 1Meps Event-Driven Visual Data Processing Unit	Somnath Paul, Intel, USA
CA2.3 - A 65nm Image Processing SoC Supporting Multiple DNN Models and Real-Time Computation-Communication Trade-Off via Actor-Critical Neuro-Controller	Ningyuan Cao, Georgia Institute of Technology, USA
CA2.4 - A Ray-Casting Accelerator in 10nm CMOS for Efficient 3D Scene Reconstruction in Edge Robotics and Augmented Reality Applications	Steven Hsu, Intel, USA
CA3.2 - 17.3GCUPS Pruning-Based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing	Xiao Wu, University of Michigan, Sequal, USA
CB1.2 - An Artificial Iris ASIC with High Voltage Liquid Crystal Driver, 10nA Light Range Detector and 40nA Blink Detector for LCD Flicker Removal	Bogdan Raducanu, imec, Belgium
CB1.3 - A Packaged Ingestible Bio-Pill with 15-Pixel Multiplexed Fluorescence Nucleic-Acid Sensor and Bi-Drectional Wireless Interface for In-vivo Bio-Molecular Sensing	Chengjie Zhu, Princeton University, USA
CB2.3 - A 3.0μW@5fps QQVGA Self-Controlled Wake-Up Imager with On-Chip Motion Detection, Auto-Exposure and Object Recognition	Arnaud Verdant, CEA-Leti-MINATEC, France
CB3.2 - A Pressure Sensing System with ±0.75mmHg (3σ) Inaccuracy for Battery-Powered Low Power IoT Applications	Seok Hyeon Jeong, University of Michigan, USA
CB4.4 - A Portable NMR System with 50kHz IF, 10μs Dead Time, and Frequency Tracking	Sungjin Hong, University of Texas at Austin, USA

EB1 Executive Session - Memory (1)

June-15 19:00 PDT / June-16 04:00 CET / June-16 11:00 JST (1 hour)

Session Chairs: Jixin Yu (Western Digital), Deoksin Kil (SK Hynix Semiconductor)

THL.4 - A Monolithic 3D Integration of RRAM Array with Oxide Semiconductor FET for In-Memory Computing in Quantized Neural Network AI Applications	Jixuan Wu, University of Tokyo, Japan
TM1.1 - An Extremely Scaled Hemi-Cylindrical (HC) 3D NAND Device with Large V_t Memory Window (>10V) and Excellent 100K Endurance	Pei-Ying Du, Macronix International Co., Ltd., Taiwan
TM1.2 - An Approach to Embedding Traditional Non-Volatile Memories into a Deep Sub-Micron CMOS	Chia-Sheng Lin, TSMC, Taiwan
TM1.3 - A Vertical 2T NOR (V2T) Architecture to Enable Scaling and Low-Power Solutions for NOR Flash Technology	Hang-Ting Lue, Macronix International, Taiwan
TM1.5 - A No-Verification Multi-Level-Cell (MLC) Operation in Cross-Point OTS-PCM	Nanbo Gong, IBM T. J. Watson Research Center, USA
TM1.6 - Si Incorporation Into AsSeGe Chalcogenides for High Thermal Stability, High Endurance and Extremely Low V_{th} Drift 3D Stackable Cross-Point Memory	Huai-Yu Cheng, Macronix International, Taiwan
TM2.2 - A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing	Weier Wan, Stanford University, USA
TM2.3 - Industrially Applicable Read Disturb Model and Performance on Mega-Bit 28nm Embedded RRAM	Chang-Feng Yang, TSMC, Taiwan

EB2 Executive Session - Intelligent Computing June-15 19:00 PDT / June-16 04:00 CET / June-16 11:00 JST (1 hour)	
Session Chairs: Zhengya Zhang (University of Michigan), Vinayak Honkote (Intel)	
CA1.3 - An Ultra-Low Latency 7.8-13.6 pJ/b Reconfigurable Neural Network-Assisted Polar Decoder with Multi-Code Length Support	Chieh-Fang Teng, National Taiwan University, Taiwan
CA1.4 - A 4.45ms Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices	Dongseok Im, Korea Advanced Institute of Science and Technology, Republic of Korea
CA2.5 - A 1200x1200 8-Edges/Vertex FPGA-Based Motion-Planning Accelerator for Dual-Arm-Robot Manipulation Systems	Takashi Oshima, Hitachi, Japan
CA3.1 (Invited) - Managing Chip Design Complexity in the Domain-Specific SoC Era	Yunsup Lee, SiFive, USA
CA3.4 - MANA: A Monolithic Adiabatic iNtegration Architecture Microprocessor Using 1.4zJ/op Superconductor Josephson Junction Devices	Christopher Ayala, Yokohama National University, Japan
CA3.5 - 32GHz 6.5mW Gate-Level-Pipelined 4-bit Processor using Superconductor Single-Flux-Quantum Logic	Koki Ishida, Kyushu University, Japan
CM3.4 - Z-PIM: An Energy-Efficient Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision	Ji-Hoon Kim, Korea Advanced Institute of Science and Technology, Republic of Korea
JFS4.4 - PNPU: A 146.52TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping	Sangyeob Kim, Korea Advanced Institute of Science and Technology, Republic of Korea

Tuesday June-16

PSC1 Technology Short Course E-Pitch & Q/A Panel Future of Scaling for Logic and Memory June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)
Session Chairs: Nirmal Ramaswamy (Micron), Kazuhiko Endo (AIST)
Nicolas Loubet, IBM, USA
Mauro Kobrinsky, Intel, USA
Gwan-Hyeob Koh, Samsung Electronics, Republic of Korea
Uwe Schroeder, NaMLab gGmbH, Germany
Anthony Yen, ASML, USA
Chang-Hong Shen, Taiwan Semiconductor Research Institute, Taiwan
Suman Datta, University of Notre Dame, USA
Tatsuro Maeda, National Institute of Advanced Industrial Science and Technology, Japan

PSC2 Joint Short Course E-Pitch & Q/A Panel Heterogeneous Integration – To Boldly Go Where No Moore Has Gone Before June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)
Session Chairs: Vijay Narayanan (IBM), Alvin Loke (TSMC)
Samuel Naffziger, AMD, USA
Eric Beyne, imec, Belgium
Key Chung, SPIL R&D, Taiwan
Arvind Kumar & Mukta Farooq, IBM Research, USA
Marco Del Sarto, STMicroelectronics, Italy
Kenny C.H. Hsieh, TSMC, Taiwan
Rajesh Gupta, Synopsys, USA
Ki Chul Chun, Samsung Electronics, Republic of Korea

PSC3 Circuits Short Course E-Pitch & Q/A Panel Trends and Advancements in Circuit Design June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)
Session Chairs: Xin Zhang (IBM), Minkyu Je (KAIST)
Wing-Hung Ki, Hong Kong University of Science and Technology, China
Michael Flynn, University of Michigan, USA
Kofi Makinwa, Delft University of Technology, Netherlands
Jae-Yoon Sim, POSTECH, Republic of Korea
Yao-Hong Liu, imec, Netherlands
Mounir Meghelli, IBM, USA
Thomas Burd, AMD, USA
Yih Wang, TSMC, Taiwan

P4 SSCS/EDS-Sponsored Diversity Panel - Cultivating Engineering Confidence June-16 08:00 PDT / June-16 17:00 CET / June-17 00:00 JST (1 hour)
Session Chairs: Nadine Collaert (imec), Carolina Mora Lopez (imec)
Susan Feindt, Analog Devices, USA
Danielle Griffith, Texas Instruments, USA
Makoto Ikeda, University of Tokyo, Japan
Myung-Hee Na, imec, Belgium

EC1 Executive Session - Memory (2)	
June-16 09:00 PDT / June-16 18:00 CET / June-17 01:00 JST (1 hour)	
Session Chairs: Gosia Jurczak (Lam Research)	
CM1.4 - 2X-Bandwidth Burst 6T-SRAM for Memory Bandwidth Limited Workloads	Charles Augustine, Intel, USA
CM2.1 - A 14.7Mb/mm^2 28nm FDSOI STT-MRAM with Current Starved Read Path, 52Ω/Sigma Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference	El Mehdi Boujamaa, Arm, France
CM3.2 - A 65nm 16kb SRAM with 131.5pW Leakage at 0.9V for Wireless IoT Sensor Nodes	Shourya Gupta, University of Virginia, USA
CM3.3 - 1.03pW/b Ultra-Low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors	Jingcheng Wang, University of Michigan, USA
JFS3.3 - Buried Powered SRAM DTCO and System-Level Benchmarking in N3	Shairfe Salahuddin, imec, Belgium
TF2.2 - A Novel Dual Ferroelectric Layer Based MFMFIS FeFET with Optimal Stack Tuning Toward Low Power and High-Speed NVM for Neuromorphic Applications	Tarek Ali, Fraunhofer IPMS Center Nanoelectronic Technologies, Germany
TF2.4 - Nanosecond Laser Anneal (NLA) for Si-Implanted HfO_2 Ferroelectric Memories Integrated in Back-End Of Line (BEOL)	Laurent Grenouillet, CEA-Leti-MINATEC, France
TF2.7 - Probing the Evolution of Electrically Active Defects in Doped Ferroelectric HfO_2 During Wake-Up and Fatigue	Umberto Celano, imec, Belgium
TM1.4 - Understanding of Tunable Selector Performance in Si-Ge-As-Se OTS Devices by Extended Percolation Cluster Model Considering Operation Scheme and Material Design	Shoichi Kabuyanagi, Kioxia, imec, Japan
TM2.1 - A SiO_x RRAM-Based Hardware with Spike Frequency Adaptation for Power-Saving Continual Learning in Convolutional Neural Networks	Irene Munoz-Martin, Politecnico di Milano, Italy
TMFS.2 (Invited) - Magnetic Random Access Memories (MRAM) Beyond Information Storage	Ricardo Sousa, Université Grenoble Alpes / CEA / CNRS, Spintec, France
EC2 Executive Session - Analog Building Blocks	
June-16 09:00 PDT / June-16 18:00 CET / June-17 01:00 JST (1 hour)	
Session Chairs: Ewout Martens (imec)	
CD1.2 - A 10-bit 100MS/s SAR ADC with Always-on Reference Ripple Cancellation	Xiyuan Tang, University of Texas at Austin, USA
CD1.5 - A Compact 14GS/s 8-bit Switched-Capacitor DAC in 16nm FinFET CMOS	Pietro Caragiulo, Stanford University, USA
CD2.1 - A 440µW, 109.8dB DR, 106.5dB SNDR Discrete-Time Zoom ADC with a 20kHz BW	Efraïm Eland, Delft University of Technology, Netherlands
CF1.2 - A Fast Locking 5.8−7.2 GHz Fractional-N Synthesizer with Sub-2µs Settling Time in 22nm FDSOI	Jeffrey Prinzie, Katholieke Universiteit Leuven, Belgium
CF1.4 - A 3.3-GHz 101fs$_{rms}$-Jitter, −250.3dB FOM Fractional-N DPLL with Phase Error Detection Accomplished in Fully Differential Voltage Domain	Lianbo Wu, ETH Zürich, Switzerland
CF3.5 - A 920MHz 16-FSK Receiver Achieving a Sensitivity of −103dBm at 0.6mW via an Integrated N-Path Filter Bank	Ali Nikoofard, University of California San Diego, USA
CP1.1 - A −107.8dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier	Huajun Zhang, Delft University of Technology, Netherlands
CP3.5 - A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency	Xiaosen Liu, Intel, USA
JFS5.4 - A 3D-Stacked Cortex-M0 SoC with 20.3Gbps/mm2 7.1mW/mm2 Simultaneous Wireless Inter-Tier Data and Power Transfer	Benjamin Fletcher, University of Southampton, United Kingdom
EC3 Executive Session - Adaptive Systems	
June-16 10:00 PDT / June-16 19:00 CET / June-17 02:00 JST (1 hour)	
Session Chairs: Bora Nikolic (University of California, Berkeley)	
CC2.2 - An Autonomous Reconfigurable Power Delivery Network (RPDN) for Many-Core SoCs Featuring Dynamic Current Steering	Khondker Ahmed, Intel Coporation, USA
CD1.1 - A 1MS/s to 1GS/s Ringamp-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm	Benjamin Hershberg, imec, Belgium
CD2.4 - A 1GS/s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9dB FoMs	Yifan Lyu, MICAS-Katholieke Universiteit Leuven, Belgium
CF3.1 - SamurAI: a 1.7MOPS-36GOPS Adaptive Versatile IoT Node with 15,000x Peak-to-Idle Power Reduction, 207ns Wake-Up Time and 1.3TOPS/W ML Efficiency	Ivan Miro-Panades, University Grenoble Alpes, CEA, LIST, France
CP3.1 - An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching	Dong Yan, University of Texas at Dallas, USA
CP3.2 - Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 65nm CMOS	Xun Sun, University of Washington, USA
CP3.4 - A 4V-0.55V Input Fully Integrated Switched-Capacitor Converter Enabling Dynamic Voltage Domain Stacking and Achieving 80.1% Average Efficiency	Tim Thielemans, MICAS-Katholieke Universiteit Leuven, Belgium
PWS1 Workshop 1 Panel and Q&A - Analog Computing Technologies and Circuits for Efficient Machine Learning Hardware	
June-16 10:00 PDT / June-16 19:00 CET / June-17 02:00 JST (1 hour)	
Session Chairs: Nadine Collaert (imec)	
Moderator: Arindam Mallik, imec, Belgium	
WS1.1 - Prospects of Analog In-Memory Computing – An Overview	Boris Murmann, Stanford University, USA
WS1.2 - Designing Material Systems and Algorithms for Analog Computing	Robert L. Bruce, IBM Research, USA
WS1.3 - Monolithically Integrated RRAM-based Analog/ Mixed-Signal In-Memory Computing for Energy-Efficient Deep Learning	Jae-Sun Seo, Arizona State University, USA
WS1.4 - Compute-in-Memory Circuit and Device Technologies: Trends and Prospects	Jaydeep Kulkarni, University of Texas at Austin, USA
WS1.5 - Analog Computing for Machine Learning – An Ideal Case for Co-Optimization of System and Device Technology	Arindam Mallik, imec, Belgium
WS1.6 - System and Architecture Level Considerations in Leveraging Mixed-Signal Techniques for ML at the Edge	Mahesh Mehendale, Texas Instruments, USA
P1 Technology Panel - Memory and Logic Technology Divergence: Will AI/ML bring them back together?	
June-16 17:00 PDT / June-17 02:00 CET / June-17 09:00 JST (1 hour)	
Organizers: Greg Yeric (Arm), Hiroshi Morioka (Socionext)	
Moderator: Gary Bronner, Rambus, USA	
Suburamanian Iyer, University of California, Los Angeles, USA	
Steve Pawlowski, Micron, USA	
Vivienne Sze, Massachusetts Institute of Technology, USA	
Keh-Chung Wang, Macronix International, Taiwan	
Zhao Wang, Facebook, Japan	

P3 Circuits Panel - Human vs. Machine: The Future Role of AI/Machine Learning in Circuit Design June-16 17:00 PDT / June-17 02:00 CET / June-17 09:00 JST (1 hour)	
Organizers: Stacy Ho (MediaTek) , Yasuhiro Takai (Micron)	
Moderator: Chris Mangelsdorf, Analog Devices, USA	
Elad Alon, University of California, Berkeley, USA	
Linton Salmon, Semi Tech Associates, USA	
Nan Sun, University of Texas at Austin, USA	
David Wentzloff, University of Michigan, USA	
Kazuo Yano, Hitachi, Japan	
ED1 Executive Session - Heterogeneous Integration (1) **June-16 18:00 PDT / June-17 03:00 CET / June-17 10:00 JST (1 hour)**	
Session Chairs: Willy Rachmady (Intel), Osbert Cheng (UMC)	
JFS5.1- Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry: Multi-Tier Complementary Carbon Nanotube Logic and Resistive RAM at a 130 nm Node	Tathagata Srimani, Massachusetts Institute of Technology, USA
TH2.2 - Surrounding Gate Vertical-Channel FET with Gate Length of 40nm Using BEOL Compatible High-Thermal-Tolerance In-Al-Zn Oxide Channel	Hirokazu Fujiwara, Kioxia, Japan
TH2.3 - Amorphous IGZO TFTs featuring Extremely-Scaled Channel Thickness and 38nm Channel Length: Achieving Record High $G_{m,max}$ of 125 μS/μm at V_{DS} of 1V and I_{ON} of 350μA/μm	Subhranu Samanta, National University of Singapore, Singapore
TH3.4 - First Demonstration of Low Temperature (≤500°C) CMOS Devices Featuring Functional RO and SRAM Bitcells toward 3D VLSI Integration	Claire Fenouillet-Beranger, CEA-Leti-MINATEC, France
TH3.5 - Flexible and Transparent BEOL Monolithic 3DIC Technology for Human Skin Adaptable Internet of Things Chips	Ming-Hsuan Kao, Taiwan Semiconductor Research Institute, Taiwan
ED2 Executive Session - Power **June-16 18:00 PDT / June-17 03:00 CET / June-17 10:00 JST (1 hour)**	
Session Chairs: Hylas Lam (Analog Devices), Sung-Wan Hong (Sookmyung Women's University)	
CP1.2 - An 8Ω, 1.4W, 0.0024% THD+N Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Mode Achieving Low Standby Quiescent Current of 660μA	Ji-Hun Lee, Korea Advanced Institute of Science and Technology, Republic of Korea
CP1.4 - A 0.0046mm^2 6.7μW Three-Stage Amplifier Capable of Driving 0.5-to-1.9nF Capacitive Load with >0.68MHz GBW without Compensation Zero	Hongseok Shin, Korea Advanced Institute of Science and Technology, Republic of Korea
CP2.1 - A Single-Trim Switched Capacitor CMOS Bandgap Reference with a 3σ Inaccuracy of +0.02%, -0.12% for Battery Monitoring Applications	Jun-Ho Boo, Sogang University, Republic of Korea
CP2.2 - A 0.25-V, 5.3-pW Voltage Reference with 25μV/°C Temperature Coefficient, 140μV/V Line Sensitivity and 2,200μm^2 Area in 180nm	Longyan Lin, National University of Singapore, Singapore
CP2.3 - A 6.78MHz Wireless Power Transfer System Enabling Perpendicular Wireless Powering with Efficiency Increase from 0.02% to 48.2% by Adaptive Magnetic Field Adder IC	Hao Qiu, University of Tokyo, Japan
CP3.6 - A Domino Bootstrapping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 96% High Efficiency	Hsuan-Yu Chen, ECE, National Chiao Tung University, Taiwan
JFS3.2 (Invited) - Can We Ever Get to a 100nm Tall Library? Power Rail Design for 1nm Technology Node	Victor Moroz, Synopsys, USA
THL.2 - GaN and Si Transistors on 300mm Si(111) enabled by 3D Monolithic Heterogeneous Integration	Han Wui Then, Intel, USA
TN1.9 - GaN PMIC Opportunities: Characterization of Analog and Digital Building Blocks in a 650V GaN-on-Si Platform	Wan Lin Jiang, University of Toronto, Canada
ED3 Executive Session - 3D Packaging **June-16 19:00 PDT / June-17 04:00 CET / June-17 11:00 JST (1 hour)**	
Session Chairs: Michael Delaus (Analog Devices), Tetsu Tanaka (Tohoku University)	
JFS5.5 - Heterogeneous Power Delivery for 7nm High-Performance Chiplet-Based Processors Using Integrated Passive Device and In-Package Voltage Regulator	Alan Roth, TSMC, USA
TH1.1 - Low Temperature SoIC Bonding and Stacking Technology for 12/16-Hi High Bandwidth Memory (HBM)	C.H. Tsai, TSMC, Taiwan
TH1.3 - Bumpless Build Cube (BBCube): High-Parallelism, High-Heat-Dissipation and Low-Power Stacked Memory Using Wafer-Level 3D Integration Process	Norio Chujo, Tokyo Institute of Technology, IIR, WOW Alliance / Hitachi, Japan
TH1.5 - Immersion in Memory Compute (ImMC) Technology	C.T. Wang, TSMC, Taiwan
TH1.6 - Low Temperature Cu/SiO_2 Hybrid Bonding with Metal Passivation	Demin Liu, National Chiao Tung University, Taiwan
ED4 Executive Session - Sensors **June-16 19:00 PDT / June-17 04:00 CET / June-17 11:00 JST (1 hour)**	
Session Chairs: Ron Kapusta (Analog Devices), Tomohiro Takahashi (Sony Semiconductor Solutions)	
CB1.4 - 1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-Chip with Dynamic Incremental-SAR Acquisition	Jun Wang, University of California San Diego, USA
CB1.5 (Invited) - High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at	Yuri Kato, Sony Semiconductor Solutions Corporation, Japan
CB2.1 (Invited) - A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR	Tuan Thanh Ta, Toshiba Corp., Japan
CB2.2 - A 36-Channel SPAD-Integrated Scanning LiDAR Sensor with Multi-Event Histogramming TDC and Embedded Interference Filter	Hyeongseok Seo, Sungkyunkwan University, Republic of Korea
CB2.4 - A Low Noise Read-Out IC with Gate Driver for Full Front Display Area Optical	Yongil Kwon, Samsung Electronics, Republic of Korea
CB2.5 - An Always-On 4x Compressive VGA CMOS Imager with 51pJ/pixel and >32dB PSNR	Wenda Zhao, The University of Texas at Austin, USA
CB3.1 - A 50.7dB-DR Finger-Resistance Extractable Multi-Touch Sensor IC Achieving Finger-Classification Accuracy of 97.7% on 6.7-inch Capacitive Touch Screen Panel	Tae-Gyun Song, Korea Advanced Institute of Science and Technology, Republic of Korea
CB4.3 - A 0.5V, 6.2μW, 0.059mm^2 Sinusoidal Current Generator IC with 0.088% THD for Bio-Impedance Sensing	Kwantae Kim, Korea Advanced Institute of Science and Technology, Republic of Korea
CC2.3 - Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting	Massimo Alioto, National University of Singapore, Singapore

PWS2 Workshop 2 Panel and Q&A - Know Where You Are Going; Metrology In the New Age of Semiconductor Manufacturing **June-16 19:00 PDT / June-17 04:00 CET / June-17 11:00 JST (1 hour)**	
Session Chairs: Gosia Jurczak (Lam Research), Takaaki Tsunomura (Tokyo Electron)	
Moderator: Tom Larson, Nova Measuring Instruments	
WS2.1 - Introduction to Metrology Workshop	Tom Larson, Nova Measuring Instruments
WS2.2 - Manufacturing Process Challenges and Requirements for Metrology in Semiconductor Memory Devices	Keiji Suzuki, Kioxia
WS2.3 - Metrology with Angstrom Accuracy Required by Logic IC Manufacturing – Challenges From R&D to High Volume Manufacturing and Solutions in the AI Era	Yi Hung Lin, TSMC
WS2.4 - Dimensional Metrology Overview, Trends and Upcoming C'hallenges	Philippe Leray, imec
WS2.5 - Defect Inspection: A Trio of Trends for the 2020s	Mark Shirey, KLA
WS2.6 - Enabling Modern Semiconductor Manufacturing With Materials Metrology	Kavita Shah, Nova Measuring Instruments
WS2.7 - Opportunities and Challenges for Lab-based Characterization for Emerging Technologies	Markus Kuhn, Intel
Wednesday, June 17	
PFF Forum E-Pitch & Q/A Panel **June-17 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)**	
Session Chairs: Kamel Benaissa (Texas Instruments), Ron Kapusta (Analog Devices), Kazuyuki Tomida (Sony Semiconductor Solutions), Kouichi Kanda (Fujitsu Laboratories)	
Ali Keshavarzi, Stanford University, USA	
Gowri Chindalore, NXP Semiconductors, USA	
Chih Hang Tung, TSMC, Taiwan	
Benton Calhoun, University of Virginia, USA	
Myung Hee Na, imec, Belgium	
Thomas Watteyne, Analog Devices, USA	
Hayato Wakabayashi, Sony Semiconductor Solutions, Japan	
David Blaauw, University of Michigan, USA	
Hannes Tschofenig, Arm, USA	
PL2 - Plenary 2 **SELECT June-17 08:00 PDT / June-17 17:00 CET / June-18 00:00 JST OR June-17 17:00 PDT / June-18 02:00 CET / June-18 09:00 JST (2 hours)**	
Session Chairs: Tomas Palacios (MIT), Yusuke Oike (Sony Semiconductor Solutions)	
PL2.1 (Plenary) - The Future of Compute: How the Data Transformation is Reshaping VLSI	Michael Mayberry, Intel, USA
PL2.2 (Plenary) - Empowering Next-Generation Applications through FLASH Innovation	Shigeo (Jeff) Ohshima, Kioxia, Japan
EE1 Executive Session - Ultra Low Energy Systems **June-17 10:00 PDT / June-17 19:00 CET / June-18 02:00 JST (1 hour)**	
Session Chairs: Danielle Griffith (Texas Instruments)	
CF3.2 (Invited) - Industrial IoT with Crystal-Free Mote-on-Chip	Thomas Watteyne, Inria, France
CF3.3 - A Multichannel, MEMS-Less −99dBm 260nW Bit-level Duty Cycled Wakeup Receiver	Anjana Dissanayake, University of Virginia, USA
CF3.4 - A 4.4μW −92/−90.3dBm Sensitivity Dual-mode BLE/Wi-Fi Wake-Up Receiver	Po-Han Peter Wang, University of California San Diego, USA
CF4.1 - A 8.7ppm/°C, 694nW, One-Point Calibrated RC Oscillator Using a Nonlinearity-Aware Dual Phase-Locked Loop and DSM-Controlled Frequency-Locked Loops	Giorgio Cristiano, ETH Zürich, Switzerland
CF4.2 - A 0.5V 560kHz 18.8fJ/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop	Daniel Truesdell, University of Virginia, USA
CF4.3 - A 0.9pJ/cycle 8ppm/°C DFLL-based Wakeup Timer Enabled by a Time-Domain Trimming and an Embedded Temperature Sensing	Ming Ding, imec, Netherlands
CP2.4 - A 120-330V, Sub-μA, 4-Channel Driver for Microrobotic Actuators with Wireless-Optical Power Delivery and Over 99% Current Efficiency	Jan Rentmeister, Dartmouth College, USA
CP3.3 - An N-Path Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting Achieving 13.9x Power Extraction Improvement	Loai Salem, University of California Santa Barbara, USA
PWS3 Workshop 3 Panel and Q&A - Quantum Computers for Electrical Engineers **June-17 10:00 PDT / June-17 19:00 CET / June-18 02:00 JST (1 hour)**	
Session Chairs: Maud Vinet (CEA-Leti)	
Moderator: Iuliana Radu, imec, Belgium	
TN2.1 - Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures Down to 100mK for Quantum Computing	Bruna Paz, CEA-Leti-MINATEC, France
TN2.2 - Toward Long-Coherence-Time Si Spin Qubit: The Origin of Low-Frequency Noise in Cryo-CMOS	Hiroshi Oka, National Institute of Advanced Industrial Science and Technology, Japan
WS3.1 - 3D Integration and Challenges for Scaling	William Oliver, Massachusetts Institute of Technology
WS3.2 - Superconducting Qubits: How Technology/ Processing/ Materials Impact Coherence Time and How Design Impacts Gate Fidelity	Doug McClure, IBM, USA
WS3.3 - Si Based Qubits: Technology and Material Impact on Performance	Iuliana Radu, imec, Belgium
WS3.4 - Architectures Challenges for Si Spin Qubits	Maud Vinet, CEA-Leti, France
WS3.5 - Cryo-CMOS Components for Quantum Tech	Joseph Bardin, Google AI Quantum & University of Massaschusetts Amherst, USA

EF1 Executive Session - Ferroelectrics	
June-17 19:00 PDT / June-18 04:00 CET / June-18 11:00 JST (1 hour)	
Session Chairs: Suman Datta (University of Notre Dame), Byoung-Hun Lee (Gwangju Institute of Science & Technology)	
TF1.1 - FeFET Memory Featuring Large Memory Window and Robust Endurance of Long-Pulse Cycling by Interface Engineering Using High-k AlON	Chi-Yu Chan, National Tsing Hua University, Taiwan
TF1.2 - Re-Examination of V_{th} Window and Reliability in HfO_2 FeFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation	Reika Ichihara, Kioxia Corporation, Japan
TF1.3 - Hot Electrons as the Dominant Source of Degradation for Sub-5nm HZO FeFETs	Ava Tan, University of California, Berkeley, USA
TF1.4 - A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation	Kai Ni, Rochester Institute of Technology, USA
TF1.5 - Asymmetric Polarization Response of Electrons and Holes in Si FeFETs: Demonstration of Absolute Polarization Hysteresis Loop and Inversion Hole Density Over 2×10^{13} cm^{-2}	Kasidit Toprasertpong, University of Tokyo, Japan
TF2.1 - SoC Compatible 1T1C FeRAM Memory Array Based on Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$	Jun Okuno, Sony Semiconductor Solutions, Japan
TF2.3 - Improved State Stability of HfO_2 Ferroelectric Tunnel Junction by Template-Induced Crystallization and Remote Scavenging for Efficient In-Memory Reinforcement Learning	Shosuke Fujii, Kioxia, Japan
TF2.5 - Fast Thermal Quenching on the Ferroelectric Al: HfO_2 Thin Film with Record Polarization Density and Flash Memory Application	Changhwan Choi, Hanyang University, Republic of Korea
TF2.6 - Multi-Probe Characterization of Ferroelectric/Dielectric Interface by C-V, P-V and Conductance Methods	Junkang Li, Purdue University, USA
TF2.8 - Atomic-Scale Imaging of Polarization Switching in an (Anti-)Ferroelectric Memory Material: Zirconia (ZrO_2)	Sarah Lombardo, MSE, Georgia Institute of Technology, USA
EF2 Executive Session - Advances in Clocking and Data Converters	
June-17 19:00 PDT / June-18 04:00 CET / June-18 11:00 JST (1 hour)	
Session Chairs: Stacy Ho (MediaTek), Kenichi Okada (Tokyo Institute of Technology)	
CD1.3 - An 8b 1GS/s 2.55mW SAR-Flash ADC with Complementary Dynamic Amplifiers	Dong-Ryeol Oh, Korea Advanced Institute of Science and Technology, Republic of Korea
CD1.4 - A 177mW 10GS/s NRZ DAC with Switching-Glitch Compensation Achieving > 64dBc SFDR and < -77dBc IM3	Hung-Yi Huang, National Cheng Kung University, Taiwan
CD2.2 - A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved Second-Order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS	Dongyang Jiang, University of Macau, Macao
CD2.3 - A 10.4mW 50MHz-BW 80dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp	Kai Xing, University of Macau, China
CD2.5 - A SAR ADC with Reduced kT/C Noise by Decoupling Noise PSD and BW	Zhelu Li, Zhejiang University, University of Texas at Austin, China
CF1.1 - Embedded PLL Phase Noise Measurement Based on a PFD/CP MASH 1-1-1 ΔΣ Time-to-Digital Converter in 7nm CMOS	Mao-Hsuan Chou, TSMC, Taiwan
CF1.3 - A 4GHz 0.73ps_{rms}-Integrated-Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring PLL with a Jitter-Tracking DLL-Assisted DTC	Jaehong Jung, Samsung Electronics, Republic of Korea
CF1.5 - A 3.2-to-3.8GHz Calibration-Free Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving −66dBc Worst-Case In-Band Fractional Spur	Masaru Osada, University of Tokyo, Japan
CW1.3 - A 4-to-18GHz Active Poly Phase Filter Quadrature Clock Generator with Phase Error Correction in 5nm CMOS	Wei-Chih Chen, TSMC, Taiwan
Thursday, June 18	
EG1 Executive Session - Heterogeneous Integration (2)	
June-18 08:00 PDT / June-18 17:00 CET / June-19 00:00 JST (1 hour)	
Session Chairs: Bill En (AMD)	
JFS1.5 - O-Band GeSi Quantum-Confined Stark Effect Electro-Absorption Modulator Integrated in a 220nm Silicon Photonics Platform	Clement Porret, imec, Belgium
TH1.2 - 3D Heterogeneous Package Integration of Air/Magnetic Core Inductor: 89%-Efficiency Buck Converter with Backside Power Delivery Network	Xiao Sun, imec, Belgium
TH1.4 - ExaNoDe: Combined Integration of Chiplets on Active Interposer with Bare Dice in a Multi-Chip-Module for Heterogeneous and Scalable High Performance Compute Nodes	Pierre-Yves Martinez, Université Grenoble Alpes, CEA-LIST, France
TH2.1 - BEOL Compatible Dual-Gate Ultra Thin-Body W-Doped Indium-Oxide Transistor with I_{on}=370μA/μm, SS=73mV/dec and I_{on}/I_{off} ratio > $4x10^9$	Wriddhi Chakraborty, University of Notre Dame, USA
TH3.1 - First Monolithic Integration of 3D Complementary FET (CFET) on 300mm Wafers	Sujith Subramanian, imec, Belgium
TH3.2 - 3D Sequential Low Temperature Top Tier Devices Using Dopant Activation with Excimer Laser Anneal and Strained Silicon as Performance Boosters	Anne Vandooren, imec, Belgium
TH3.3 - 28nm FDSOI CMOS Technology (FEOL and BEOL) Thermal Stability for 3D Sequential Integration: Yield and Reliability Analysis	Camila Cavalcante, CEA-Leti, France
EG2 Executive Session - Robust Computing	
June-18 08:00 PDT / June-18 17:00 CET / June-19 00:00 JST (1 hour)	
Session Chairs: Carlos Tokunaga (Intel)	
CC1.1 - A Performance-Flexible Energy-Optimized Automotive-Grade Cortex-R4F SoC Through Combined AVS/ABB/Bias-in-Memory-Array Closed-Loop Regulation in 28nm FD-SOI	Ricardo Gomez Gomez, STMicroelectronics, France
CC1.2 - A SCA-Resistant AES Engine in 14nm CMOS with Time/Frequency-Domain Leakage Suppression Using Non-linear Digital LDO Cascaded with Arithmetic Countermeasures	Raghavan Kumar, Intel, USA
CC1.3 - A 0.26% BER, 10^{28} Challenge-Response Machine-Learning Resistant Strong-PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection	Vikram Suresh, Intel, USA
CC1.4 - A 435MHz, 2.5Mbps/W Side-Channel-Attack Resistant Crypto-Processor for Secure RSA-4K Public-Key Encryption in 14nm CMOS	Raghavan Kumar, Intel, USA
CC2.1 - A Proactive Voltage-Droop-Mitigation System in a 7nm Hexagon™ Processor	Vijay Kiran Kalyanam, Qualcomm Technologies, USA
CC2.4 - UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in Designs with Large Clock Distribution Delays in 65nm CMOS	Xun Sun, University of Washington, USA
CC2.5 - Low-Clock-Power Digital Standard Cell IPs for High-Performance Graphics/AI Processors in 10nm CMOS	Steven Hsu, Intel, USA
Luncheon - Do You Really Know What Is In Your Computer? Perspectives on Verifiable Supply Chains	Andrew "bunnie" Huang, Singapore

EG3 Executive Session - AI/ML	
June-18 09:00 PDT / June-18 18:00 CET / June-19 01:00 JST (1 hour)	
Session Chairs: Paul Whatmough (Arm)	
CA1.1 - A 3.0 TFLOPS 0.62V Scalable Processor Core for High Compute Utilization AI Training	Sae Kyu Lee, IBM T. J. Watson Research Center, USA
CA1.2 - A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS	Phil Knag, Intel, USA
CA1.5 - A 3mm^2 Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception Using Parallel Gibbs Sampling in 16nm	Glenn G. Ko, Harvard University, USA
CA3.3 - A Probabilistic Self-Annealing Compute Fabric based on 560 Hexagonally Coupled Ring Oscillators for Solving Combinatorial Optimization Problems	Ibrahim Ahmed, University of Minnesota, USA
JFS4.1 - SOT-MRAM Based Analog in-Memory Computing for DNN Inference	Jonas Doevenspeck, imec, ESAT-Katholieke Universiteit Leuven, Belgium
JFS4.3 - An All-Weights-on-Chip DNN Accelerator in 22nm ULL Featuring 24×1 Mb eRRAM	Zhehong Wang, University of Michigan, USA
JFS4.5 - A Mixed-Signal Time-Domain Generative Adversarial Network Accelerator with Efficient Subthreshold Time Multiplier and Mixed-signal On-chip Training for Low Power Edge	Zhengyu Chen, Northwestern University, USA
EG4 Executive Session - Sensing Interfaces and Building Blocks	
June-18 09:00 PDT / June-18 18:00 CET / June-19 01:00 JST (1 hour)	
Session Chairs: Carolina Mora Lopez (imec)	
CB1.1 - A 785nW Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring	Peng Wang, University of Virginia, USA
CB3.3 - A 200μW Eddy Current Displacement Sensor with 6.7nm$_{rms}$ Resolution	Matheus Pimenta, Cypress Semiconductor, Ireland
CB3.4 - A 0.72nW, 1Sample/s Fully Integrated pH Sensor with 65.8LSB/pH Sensitivity	Yihan Zhang, Columbia University, USA
CB3.5 - An 8-Element Frequency-Selective Acoustic Beamformer and Bitstream Feature Extractor with 60 Mel-Frequency Energy Features Enabling 95% Speech Recognition Accuracy	Seungjong Lee, University of Michigan, USA
CB4.1 - A −105dB THD 88dB-SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation	Jiannan Huang, University of California San Diego, USA
CB4.2 - A 4.3fJ/conversion-step 6440μm^2 All-Dynamic Capacitance-to-Digital Converter with Energy-Efficient Charge Reuse	Haoming Xin, Eindhoven University of Technology, Netherlands
CP1.3 - Sample and Average Common-Mode Feedback in a 101nW Acoustic Amplifier	Rohit Rothe, University of Michigan, USA
JFS5.3 - A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-g Measurement Capability and Low Bias Instability	Xiaoliang Li, Carnegie Mellon University, USA
EG5 Executive Session - Devices and Circuits for Advanced Communications	
June-18 10:00 PDT / June-18 19:00 CET / June-19 02:00 JST (1 hour)	
Session Chairs: Kamel Benaissa (Texas Instruments)	
CF2.5 - 315GHz Self-Synchronizing Minimum Shift Keying Receiver in 65nm CMOS	Ibukun Momson, University of Texas at Dallas, USA
CW1.1 - A 4x112 Gb/s ADC-DSP Based Multistandard Receiver in 7nm FinFET	Masum Hossain, University of Alberta, Canada
CW1.2 - A 25-50Gb/s 2.22pJ/b NRZ RX with Dual-Bank and 3-tap Speculative DFE for Microprocessor Application in 7nm FinFET CMOS	Yang You, IBM, USA
CW2.3 - Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20GS/s 5b ENOB Analog-to-Digital Converter and 5GHz Phase Interpolator	Sung-Jin Kim, Stanford University, USA
CW2.4 - A 28mW 32Gb/s/pin 16-QAM Single-Ended Transceiver for High-Speed Memory Interface	Jieqiong Du, University of California, Los Angeles, USA
JFS2.1 (Invited) - Hardware-Software Co-integration for Configurable 5G mmWave Systems	Alberto Valdes-Garcia, IBM, USA
JFS2.2 (Invited) - Beyond 5G & Technologies: A Cross-Domain Vision	Eric Mercier, Université Grenoble Alps, CEA-Leti, France
JFS2.5 - FinFET with Contact Over Active-Gate for 5G Ultra-Wideband Applications	Ali Razavieh, GlobalFoundries, USA

EDS/SSCS Young Professionals and Students Micro-Mentoring and Career Coaching Session (WebEx)
June-18 10:00 PDT / June-18 19:00 CET / June-19 02:00 JST (1 hour)
Session Chair: Organizers: Zeynep Lulec (Analog Devices), Camilo Vélez Cuervo (Real NanoMicro), Xinfei Guo (Nvidia), Ka-Meng Lei (University of Macau), Nilesh Pandey (Indian Institute of Technology Kanpur), Pragya Kushwaha (Indian Space Research Organization)
Link to Event Registration

EH1 Executive Session - MRAM	
June-18 17:00 PDT / June-19 02:00 CET / June-19 09:00 JST (1 hour)	
Session Chairs: Shimeng Yu (Georgia Institute of Technology), Hang-Ting Lue (Macronix International)	
CM2.2 - Dual-Port Field-Free SOT-MRAM Achieving 90MHz Read and 60MHz Write Operations Under 55nm CMOS Technology and 1.2V Supply Voltage	Masanori Natsui, Tohoku University, Japan
JFS4.2 - Compact Probabilistic Poisson Neuron Based on Back-Hopping Oscillation in STT-MRAM for All-Spin Deep Spiking Neural Network	Ming-Hung Wu, National Chiao Tung University, Taiwan
TM3.1 - Scalability of Quad Interface p-MTJ for 1X nm STT-MRAM with 10ns Low Power Write Operation, 10 years Retention and Endurance > 10^{11}	Sadahiko Miura, Tohoku University, Japan
TM3.2 - Reliability Demonstration of Reflow Qualified 22nm STT-MRAM for Embedded Memory Applications	Chia-Yu Wang, TSMC, Taiwan
TM3.3 - Fast Switching of STT-MRAM to Realize High Speed Applications	Tae Young Lee, GlobalFoundries, Singapore
TM3.4 - A Reliable TDDB Lifetime Projection Model Verified Using 40Mb STT-MRAM Macro at Sub-ppm Failure Rate to Realize Unlimited Endurance for Cache Applications	Vinayak Bharat Naik, GlobalFoundries, Singapore
TMFS.1 (Invited) - Recent Progresses in STT-MRAM and SOT-MRAM for Next Generation MRAM	Tetsuo Endoh, Tohoku University, Japan
TMFS.3 - CMOS Compatible Process Integration of SOT-MRAM with Heavy-Metal Bi-Layer Bottom Electrode and 10ns Field-Free SOT Switching with STT Assist	Noriyuki Sato, Intel, USA
TMFS.4 - Deterministic and Field-Free Voltage-Controlled MRAM for High Performance and Low Power Applications	Yueh Chang Wu, imec, Belgium

EH2 Executive Session - High Speed Circuits, Systems, and Devices June-18 17:00 PDT / June-19 02:00 CET / June-19 09:00 JST (1 hour)	
Session Chairs: Parag Upadhyaya (Xilinx), Ho-Jin Song (POSTECH)	
CF2.1 - A 29% PAE 1.5bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked PLL	Yuncheng Zhang, Tokyo Institute of Technology, Japan
CF2.2 - A 28GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation	Jian Pang, Tokyo Institute of Technology, Japan
CF2.3 - A 293/440 GHz Push-Push Double Feedback Oscillators with 5.0/-3.9dBm Output Power and 2.9/0.6% DC-to-RF Efficiency in 65nm CMOS	Dzuhri Radityo Utomo, Korea Advanced Institute of Science and Technology, Republic of Korea
CF2.4 - A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-Gmax Gain Boosting Technique	Dae-Woong Park, imec, Republic of Korea
CW2.1 - A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ Calibration for Memory Interfaces	Yong-Un Jeong, Seoul National University, Republic of Korea
CW2.2 - A 0.1pJ/b/dB 28Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler	Moon-Chul Choi, Seoul National University, Republic of Korea
JFS2.3 - A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring 7nm EUV Process Technology	Minjung Jin, Samsung Electronics, Republic of Korea
JFS2.4 - Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture	Chen Sun, National University of Singapore, Singapore
JFS2.6 - An RF Transceiver with Full Digital Interface Supporting 5G New Radio FR1 with 3.84Gbps DL/1.92Gbps UL and Dual-Band GNSS in 14nm FinFET CMOS	Sangwook Han, Samsung Electronics, Republic of Korea
JFS2.7 - A 1.96Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems	Chen-Chien Kao, National Taiwan University, Taiwan
EH3 Executive Session - New Devices and Applications **June-18 18:00 PDT / June-19 03:00 CET / June-19 10:00 JST (1 hour)**	
Session Chairs: Peide Ye (Purdue University), Masaharu Kobayashi (University of Tokyo)	
TN1.1 - Hair-Like Nanostructure Based Ion Detector by 16nm FinFET Technology	Chien-Ping Wang, National Tsing Hua University, Taiwan
TN1.2 - Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry	Chia-Che Chung, National Taiwan University, Taiwan
TN1.3 - Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFET for Advanced Hardware Security	Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China
TN1.4 - A Bias and Correlation-Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking	Kai Ni, Rochester Institute of Technology, USA
TN1.5 - 1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy	Xu Bai, NEC, Japan
TN1.6 - Proposal and Experimental Demonstration of Reservoir Computing Using $Hf_{0.5}Zr_{0.5}O_2$/Si FeFETs for Neuromorphic Applications	Eishin Nako, University of Tokyo, Japan
TN1.7 - High On-Current 2D nFET of 390μA/μm at V_{DS} = 1V using Monolayer CVD MoS_2 Without Intentional Doping	Ang-Sheng Chou, TSMC, Taiwan
TN1.8 - Ultrahigh Responsivity and Tunable Photogain BEOL Compatible MoS_2 Phototransistor Array for Monolithic 3D Image Sensor with Block-Level Ssensing Circuits	Chih-Chao Yang, Taiwan Semiconductor Research Institute, Taiwan
EH4 Executive Session - Memory (3) **June-18 18:00 PDT / June-19 03:00 CET / June-19 10:00 JST (1 hour)**	
Session Chairs: Seung Kang (Qualcomm Technologies), Tsung-Yung Jonathan Chang (TSMC)	
CM1.1 - A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 175mV VMIN Reduction with Negligible Power Overhead	Zheng Guo, Intel, USA
CM1.2 - A 29.2Mb/mm² Ultra High Density SRAM Macro Using 7nm FinFET Technology with Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit	Yoshisato Yokoyama, Renesas Electronics, Japan
CM1.3 - Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1R1W 8T-bitcell SRAM in 10nm FinFET CMOS	Jaydeep Kulkarni, Intel, USA
CM1.5 - A 7nm Fin-FET 4.04-Mb/mm² TCAM with Improved Electromigration Reliability Using Far-Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier	Makoto Yabuuchi, Renesas Electronics, Japan
CM2.3 - A 28nm 1.5Mb Embedded 1T2R RRAM with 14.8 Mb/mm^2 Using Sneaking Current Suppression and Compensation Techniques	Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China
CM2.4 - A 22nm 96Kx144 RRAM Macro with a Self-Tracking Reference and a Low Ripple Charge Pump to Achieve a Configurable Read Window and a Wide Operating Voltage Range	Chung-Cheng Chou, TSMC, Taiwan
CM3.1 - A 28nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation	Hoyoung Shin, Samsung Electronics, Republic of Korea
JFS5.2 - A 1.8Gb/s/pin 16Tb NAND Flash Memory Multi-Chip Package with F-Chip of Toggle 4.0 Specification for High Performance and High Capacity Storage Systems	Daehoon Na, Samsung Electronics, Republic of Korea

EH5 Executive Session - Advanced CMOS (2)	
June-18 19:00 PDT / June-19 04:00 CET / June-19 11:00 JST (1 hour)	
Session Chairs: Benjamin Colombeau (Applied Materials), Munehiro Tada (NEC)	
JFS3.4 - Local Variation-Aware Transistor Design through Comprehensive Analysis of Various Vdd/Temperatures Using Sub-7nm Advanced FinFET Technology	Soyoun Kim, Samsung Electronics, Republic of Korea
TC1.1 - Enabling Multiple-Vt Device Scaling for CMOS Technology Beyond 7nm Node	Vincent Chang, TSMC, Taiwan
TC1.3 - Cold CMOS as a Power-Performance-Reliability Booster for Advanced FinFETs	H. L. Chiang, TSMC, Taiwan
TC2.1 - Surface Ga-boosted Boron-doped $Si_{0.5}Ge_{0.5}$ using In-situ CVD Epitaxy: Achieving 1.1 × $10^{21}cm^{-3}$ Active Doping Concentration and 5.7× 10^{-10} Ω-cm^2 Contact Resistivity	Haiwen Xu, National University of Singapore, Singapore
TC2.3 - First Demonstration of 4-Stacked $Ge_{0.915}Sn_{0.085}$ Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels	Yu-Shiang Huang, National Taiwan University, Taiwan
TC3.4 - Record Low Contact Resistivity to Ge:B ($8.1x10^{-10}$Ω-cm^2) and GeSn:B ($4.1x10^{-10}$Ω-cm^2) with Optimized [B] and [Sn] by In-situ CVD Doping	Fang-Liang Lu, National Taiwan University, Taiwan
TC3.5 - High Quality N+/P Junction of Ge Substrate Prepared by Initiated CVD Doping Process	Jaehwan Kim, KAIST, Republic of Korea
TC3.6 - Ultra-low ρ_c Extraction for Recessed and Non-Recessed Contacts: Generalized Transmission Line Model	Jishen Zhang, National University of Singapore, Singapore
THL.1 - 5G and AI Integrated High Performance Mobile SoC Process-Design Co-Development and Production with 7nm EUV FinFET Technology	Jie Deng, Qualcomm Technologies, USA
EH6 Executive Session - Si Photonics and DTCO	
June-18 19:00 PDT / June-19 04:00 CET / June-19 11:00 JST (1 hour)	
Session Chairs: Ted Letavic (Global Foundries), Mitsura Takenaka (University of Tokyo)	
JFS1.1 (Invited) - TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s	Chen Sun, Ayar Labs, USA
JFS1.2 (Invited) - High-Temperature Operation of Chip-Scale Silicon-Photonic Transceiver	Daisuke Okamoto, PETRA, Japan
JFS1.3 - A Monolithically Integrated Silicon Photonics 8×8 Switch in 90nm SOI CMOS	Jonathan Proesel, IBM T. J. Watson Research Center, USA
JFS1.4 - III/V-on-Bulk-Si Technology for Commercially Viable Photonics-Integrated VLSI	Dongjae Shin, Samsung Advanced Institute of Technology, Republic of Korea
JFS3.1 (Invited) - Heterogeneous System-Level Package Integration – Trends and Challenges	Frank Lee, TSMC, Taiwan
THL.3 - An Optically Sampled ADC in 3D Integrated Silicon-Photonics/65nm CMOS	Nandish Mehta, University of California, Berkeley, USA
End of Program	