Welcome to the 2020 Symposia on VLSI Technology and Circuits

The Next 40 Years of VLSI for Ubiquitous Intelligence

40th Anniversary

The 2020 Symposia on VLSI Technology & Circuits celebrates its 40th year with a virtual conference and the central theme of "The Next 40 Years of VLSI for Ubiquitous Intelligence". This week-long virtual conference features a fully overlapped program pushing the state-of-the-art in Technology and Circuits, packed with over 200 contributed technical presentations, technology and circuit demonstrations, 3 short courses, our “Friday” Forum and a “Luncheon Talk” that will be offered on-demand from the conference websites. These materials will be available for viewing at your convenience between June 14 to June 27 with the short courses and forum offering early access starting on June 8.

In addition to the on-demand sessions, the VLSI Symposia on Technology and Circuits will also feature an exciting program of live streaming events. This includes 2 plenary sessions, 4 panel discussions, 3 workshops, and 25 Executive Sessions. The goal of Executive Sessions in the VLSI Symposia is to foster a discussion about the current state and future of the field. They will include 2-minute summaries of relevant papers that have been presented at VLSI Symposia 2020 on the topic, along with 35 minutes of discussion among the authors and session chairs on key challenges and opportunities. All conference participants are encouraged to join these meetings and contribute with insight and questions.

Thank you for your support of the Symposia, especially during this unprecedented pandemic time. We hope you enjoy the Symposia and wish you and your family continued good health.

The Organizing Committee
### Live Streaming

**Watch at scheduled times**

<table>
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<th>PDT</th>
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<td>June 8 (Mon)</td>
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<td>June 29 (Mon)</td>
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### On-Demand

**Watch pre-recorded videos at your convenience**

- Early Access for
  - All 3 Short Courses
  - Forum

- All 3 Short Courses
- Forum
- Joint Focus Sessions
- Technology Sessions
- Circuits Sessions
- Joint Panel
- Demo Session
- Luncheon Talk
- All Workshops
- Full Recordings of All Live Events (available day after Live Event) except Young Professionals Mentoring

### Papers & Slides Download

**See email sent to paid attendees**

- Papers & slides of Joint Focus, Technology & Circuits Session papers
- Slides of all 3 Short Courses
- Slides of Forum

### VLSI Symposia in a Nutshell

- Early Access for
  - All 3 Short Courses
  - Forum

- All 3 Short Courses
- Forum
- Joint Focus Sessions
- Technology Sessions
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- Papers & slides of Joint Focus, Technology & Circuits Session papers
- Slides of all 3 Short Courses
- Slides of Forum
On-Demand Content

On-Demand Technology, Circuits, and Joint Sessions are similar to typical paper sessions at previous Symposia on VLSI Technology and Circuits. The 2-page paper abstracts, presentation slides, and 20-minute video presentations are provided for your convenience “on-demand” anytime between June 14 (starting at 9:00am PDT) and June 27 (ending at 11:59pm PDT). Early on-demand access for short courses and the forum begins on June 8 at 9:00am PDT.

While viewing a recorded presentation, you can ask questions by typing them in the "Q&A box", stating first the paper number and then your question. Your question will be directed to the session chairs and authors to respond.

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<thead>
<tr>
<th>Short Courses &amp; Forum</th>
<th>Technology Sessions</th>
<th>Joint Focus Sessions</th>
<th>Circuits Sessions</th>
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<tr>
<td><strong>SC1</strong> Future of Scaling for Logic/Memory</td>
<td>THL Highlight Session</td>
<td>JFS1 Silicon Photonics</td>
<td>CA1 Machine Learning</td>
</tr>
<tr>
<td><strong>SC2</strong> Heterogeneous Integration</td>
<td>TC1 Advanced Si CMOS Devices</td>
<td>TM1 NAND/NOR/PCM</td>
<td>CA2 Visual Processing &amp; AI</td>
</tr>
<tr>
<td><strong>SC3</strong> Trends/Advances in Circuit Design</td>
<td>TC2 Ge and SiGe Devices</td>
<td>TM2 RRAM</td>
<td>CD1 High-Speed Data Converters</td>
</tr>
<tr>
<td><strong>TC</strong> Tech/Circuits for Edge Intelligence</td>
<td>TC3 Advanced Processing</td>
<td>TM3 STT MRAM</td>
<td>CD2 Data Converter Techniques</td>
</tr>
<tr>
<td><strong>WS</strong> Workshops</td>
<td>TF1 FeFETs</td>
<td>TMFS MRAM Future - Beyond STT</td>
<td>CB1 Biomedical Sensors</td>
</tr>
<tr>
<td><strong>WS2</strong> Semiconductor Metrology</td>
<td>TF2 Ferroelectric Memory &amp; Caps</td>
<td>TN1 New Devices &amp; Applications</td>
<td>CB2 Image Sensor &amp; Techniques</td>
</tr>
<tr>
<td><strong>WS3</strong> Quantum Computing</td>
<td>TH1 3D Packaging</td>
<td>TN2 Quantum Computing</td>
<td>CF2 RF &amp; mm-Wave Circuits</td>
</tr>
<tr>
<td><strong>JFS</strong> Joint Focus Sessions</td>
<td>JFS3 STCO/DTCO</td>
<td>JFS4 Devices &amp; Circuits for AI/ML</td>
<td>CP1 Amplifiers</td>
</tr>
<tr>
<td><strong>CC</strong> Circuits Sessions</td>
<td>JFS5 Heterogeneous Integration</td>
<td>CB3 Physical Sensors</td>
<td>CP2 Volt References &amp; Wireless Power</td>
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<tr>
<td><strong>CM</strong> Emerging Memory Design</td>
<td>Other Events</td>
<td>CB4 Front-Ends for Sensor Interfaces</td>
<td>CP3 Power Converters</td>
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<tr>
<td><strong>P2</strong> Joint Panel</td>
<td>DEMOS</td>
<td>CF3 IoT and Wireless Receivers</td>
<td>CW1 Ultra-High-Speed Wireline</td>
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<tr>
<td><strong>Luncheon Talk</strong></td>
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<td>CW2 Wireline Techniques</td>
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<td><strong>CC1</strong> Circuits for Security &amp; Safety</td>
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<td><strong>CM1</strong> Advanced SRAM Design</td>
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### Session Availability

<table>
<thead>
<tr>
<th>Session</th>
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<tbody>
<tr>
<td>Short Courses &amp; Forum</td>
<td>June-08 to June-27</td>
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<tr>
<td>Technology, Joint Focus &amp; Circuits Sessions</td>
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<tr>
<td>P2 Joint Panel</td>
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<td>Demo Session</td>
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<td>Luncheon Talk</td>
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<td>Workshops</td>
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<tr>
<td>PL1 Plenary</td>
<td>June-16 to June-27</td>
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<tr>
<td>Executive Sessions EA &amp; EB</td>
<td>June-17 to June-27</td>
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<tr>
<td>PSC1-3 Short Courses Summaries and Q&amp;A</td>
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<tr>
<td>Executive Sessions EC &amp; ED</td>
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<tr>
<td>P1, P3, P4 Panels</td>
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<tr>
<td>PWS1-2 Workshop Summaries and Q&amp;A</td>
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<tr>
<td>PL2 Plenary</td>
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<tr>
<td>PFF Forum Summary and Q&amp;A</td>
<td>June-18 to June-27</td>
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<tr>
<td>Executive Sessions EE &amp; EF</td>
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<tr>
<td>PWS3 Workshop Summaries and Q&amp;A</td>
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</table>
### Live Streaming Content

All live events (except Young Professionals event) will be available for on-demand access the day after event until June-27

**PDT** Pacific Daylight Time (e.g., Los Angeles)

**CET** Central European Time (e.g., Netherlands)

**JST** Japan Standard Time (e.g., Japan, South Korea)

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#### Traditional Sessions
- **PSC1** Tech SC Summary & Q/A
- **PSC2** Joint SC Summary & Q/A
- **PSC3** Circuit SC Summary & Q/A

#### Executive Sessions
- **PFF** Forum E-Pitch & Q/A

#### Moderated Panels
- **P4** SSCS/EDS Diversity Panel: Cultivating Engineering Confidence in COVID-19 Times

#### Workshop Panel
- **PWS1** Technology & Circuits for ML Workshop
- **PWS2** Metrology Workshop
- **PWS3** Quantum Computing Workshop

#### Webex
- **PWS2** Metrology Workshop
- **PWS3** Quantum Computing Workshop

### Monday June-15

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
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<tbody>
<tr>
<td>08:00 to 09:00</td>
<td>Joint Plenary 1</td>
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<td>09:00 to 10:00</td>
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### Tuesday June-16

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<th>Time</th>
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<tr>
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<td>10:00 to 10:50</td>
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### Wednesday June-17

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<td>10:00 to 10:50</td>
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### Thursday June-18

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<td>Joint Plenary 2</td>
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<td>10:00 to 10:50</td>
<td>Joint Plenary 2</td>
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NEW!!! What is an Executive Session?

This year’s Virtual Symposia introduces new live Executive Sessions to foster live discussions and complement the On-Demand Sessions. The Executive Sessions feature 2-minute summaries of papers assigned to each executive session, along with 35 minutes of discussion among the authors and session chairs on key challenges and opportunities. All conference participants are encouraged to join these meetings and contribute with insights and questions.

There are a total of 25 live 50-minute executive sessions. Every On-Demand Technology, Circuits, and Joint Session paper as well as the Luncheon Talk is assigned to one Executive Session. Papers from each on-demand session may be mapped to several executive sessions.

Example mapping:
VLSI Symposia 2020 - Virtual Program

On Demand Presentations

Short Courses & Forum

SC1 Technology Short Course - Future of Scaling for Logic and Memory

Session Chairs: Nirmal Ramaswamy (Micron), Vijay Narayanan (IBM), Kazuhiko Endo (AIST), Makoto Nagata (Kobe University)

SC1.1 - Nanosheet Transistor as a Replacement of FinFET for Future Nodes: Device Advantages & Specific Process Elements
Nicolas Loubet, IBM, USA

SC1.2 - On-Die Interconnect Challenges and Opportunities for Future Technology Nodes
Mauro Kobrinsky, Intel, USA

SC1.3 - Challenges and Prospects of Memory Scaling
Gwan-Hyeob Koh, Samsung Electronics, Republic of Korea

SC1.4 - Ferroelectric Hafnium Oxide: From Memory to Emerging Applications
Uwe Schroeder, NaMLab gGmbH, Germany

SC1.5 - EUV Lithography and Its Application to Logic and Memory Devices
Anthony Yen, ASML, USA

SC1.6 - Emerging Technologies for TSV-free Monolithic 3DIC
Chang-Hong Shen, Taiwan Semiconductor Research Institute, Taiwan

SC1.7 - In situ BEOL Transistors and Oxide Electronics
Suman Datta, University of Notre Dame, USA

SC1.8 - Layer Transfer Technology for Heterogeneous Material Integration
Tatsuro Maeda, National Institute of Advanced Industrial Science and Technology, Japan

SC2 Joint Short Course - Heterogeneous Integration – To Boldly Go Where No Moore Has Gone Before

Session Chairs: Alvin Loke (TSMC), Vijay Narayanan (IBM), Kazuhiko Endo (AIST), Makoto Nagata (Kobe University)

SC2.1 - Chiplet Meets the Real World: Benefits and Limits of Chiplet Designs
Samuel Naftziger, AMD, USA

SC2.2 - Heterogeneous System Partitioning and the 3D Interconnect Technology Landscape
Eric Beyne, imec, Belgium

SC2.3 - Back-End Based Chiplet Integration Solutions & Roadmap
Key Chung, SPIL R&D, Taiwan

SC2.4 - Heterogeneous Integration for AI Architectures
Arvind Kumar & Mukta Farooq, IBM Research, USA

SC2.5 - Heterogeneous Integration of Chiplets for Sensors
Marco Del Sarto, STMicroelectronics, Italy

SC2.6 - Chiplet-to-Chiplet Communication Circuits for 2.5D/3D Integration Technologies
Kenny C.H. Hsieh, TSMC, Taiwan

SC2.7 - Performance-Driven Design Methodology and Tools for 2.5D Multi-Die Integration
Rajesh Gupta, Synopsys, USA

SC2.8 - Generic Design Strategies and Considerations for 2.5D and 3D Stacked IC Designs
Ki Chul Chun, Samsung Electronics, Republic of Korea

SC3 Circuits Short Course - Trends and Advancements in Circuit Design

Session Chairs: Xin Zhang (IBM), Minkyu Je (KAIST)

SC3.1 - Topologies and Design Techniques of Switched-Capacitor Converters
Wing-Hung Ki, Hong Kong University of Science and Technology, China

SC3.2 - The Noise-Shaping SAR ADC Technique: The Best of Both Worlds
Michael Flynn, University of Michigan, USA

SC3.3 - Next-Generation Readout of Resistor-Based Sensors
Kolf Makinwa, Delft University of Technology, Netherlands

SC3.4 - Time Reference and Frequency Generation
Jae-Yoon Sim, POSTECH, Republic of Korea

SC3.5 - Low-Power and Digitally-Intensive RF Transceiver Design for IoT Applications
Yao-Hong Liu, imec, Netherlands

SC3.6 - Advances and Trends in High-Speed Serial Links for High-Density I/O Applications
Mounir Meghelli, IBM, USA

SC3.7 - Adaptive Circuit & System Design Techniques
Thomas Burd, AMD, USA

SC3.8 - Trends and Design Considerations for Emerging Memories and Memory Computing
Yih Wang, TSMC, Taiwan

FF - “Friday” Forum

Session Chairs: Kamel Benaissa (Texas Instruments), Ron Kapusta (Analog Devices), Kazuyuki Tomida (Sony Semiconductor Solutions), Kouichi Kanda (Fujitsu Laboratories)

FF.1 - Edge Intelligence – Technologies, Circuits, Architectures
Ali Keshavarzi, Stanford University, USA

FF.2 - Intelligent Edge – It’s Not Just Technology, it’s About Responsible Society
Gowri Chindalore, NXP Semiconductors, USA

FF.3 - Heterogeneous Integration Technology Trends at the Edge
Chih Hang Tung, TSMC, Taiwan

FF.4 - Self Powered SOCs for the Intelligent Edge
Benton Calhoun, University of Virginia, USA

FF.5 - CMOS and Beyond CMOS Technologies for Edge Intelligence
Myung Hee Na, imec, Belgium

FF.6 - Low Power Wireless Networking for the Edge
Thomas Watteyne, Analog Devices, USA

FF.7 - Smart Vision Sensor
Hayato Wakabayashi, Sony Semiconductor Solutions, Japan

FF.8 - Efficient Machine Learning at the Edge
David Blaauw, University of Michigan, USA

FF.9 - Security in Edge Devices
Hannes Tschöfenig, Arm, USA

Luncheon Talk

Session Chair: Brian Ginsburg (Texas Instruments)

Do You Really Know What Is In Your Computer? Perspectives on Verifiable Supply Chains
Andrew “bunnie” Huang, Singapore

Panel

P2 Joint Panel - 40 Years of VLSI to Enable the Future of Computing

Organizers: Igor Arsovski (Marvell), Greg Yeric (Arm), Ted Letavic (GlobalFoundries), Munehiro Tada (NEC)

Moderator: Stephen Kosonocky, AMD, USA

Asad Abidi, University of California, Los Angeles, USA

Tae-Jae King Liu, University of California, Berkeley, USA

Akira Matsuzawa, Tokyo Institute of Technology, Japan

Charlie Sodini, Massachusetts Institute of Technology, USA

Naveen Verma, Princeton University, USA

Plenary Sessions

PL1 - Plenary 1

Session Chairs: Brian Ginsburg (Texas Instruments), Katsura Miyashita (Toshiba)

PL1.1 (Plenary) - Silicon is Greener: Why Innovation in Circuits is Needed for Sustainability
Jennifer Lloyd, Analog Devices, USA

PL1.2 (Plenary) - 5G Evolution and 6G
Takehiro Nakamura, NTT Docomo, Japan

PL2 - Plenary 2

Session Chairs: Tomas Palacios (MIT), Yusuke Oike (Sony Semiconductor Solutions)

PL2.1 (Plenary) - The Future of Compute: How the Data Transformation is Reshaping VLSI
Michael Mayberry, Intel, USA

PL2.2 (Plenary) - Empowering Next-Generation Applications through FLASH Innovation
Shigeo (Jeff) Ohshima, Kioxia, Japan
Joint Focus Sessions

**JFS1 - Silicon Photonics**

**Session Chairs:** Ted Letavic (GlobalFoundries), Bryan Casper (Intel), Mitsuuro Takenaka (University of Tokyo), Hisakatsu Yamaguchi (Fujitsu Laboratories)

**JFS1.1** (invited) - TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s Optical I/O

Daisuke Okamoto, PETRA, Japan

JFS1.2 (invited) - High-Temperature Operation of Chip-Scale Silicon-Photonic Transceiver

Jonathan Proesel, IBM T. J. Watson Research Center, USA

JFS1.3 - A Monolithically Integrated Silicon Photonics xK Switch in 90nm SOI CMOS

JFS1.4 - IVV-on-Bulk Si Technology for Commercially Viable Photonics-Integrated VLSI

JFS1.5 - O-Band GeSi Quantum-Confined Stark Effect Electro-Absorption Modulator Integrated in a 220nm Silicon Photonics Platform

Clement Porret, imec, Belgium

**JFS2 - 5G/mm-Wave**

**Session Chairs:** Kamel Benaisna (Texas Instruments), Amin Arabian (Stanford University), Aaron Thean (National University of Singapore), Wei Deng (Tsinghua University)

**JFS2.1** (invited) - Hardware-Software Co-integration for Configurable 5G mmWave Systems

Alberto Valdes-Garcia, IBM, USA

**JFS2.2** (invited) - Beyond 5G & Technologies: A Cross-Domain Vision

Eric Mercier, Université Grenoble Alpes, CEA-Leti, France

**JFS2.3** - A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring Tmm EUV Process Technology

Minjung Jin, Samsung Electronics, Republic of Korea

**JFS2.4** - Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture

Chen Sun, National University of Singapore, Singapore

**JFS2.5** - FinFET with Contact Over Active-Gate for 5G Ultra-Wideband Applications

Ali Razavieh, GlobalFoundries, USA

**JFS2.6** - An RF Transceiver with Full Digital Interface Supporting 5G New Radio FRT with 3.84Gbps DL/1.92Gbps UL and Dual-Band GNSS in 14nm FinFET CMOS

Sangwook Han, Samsung Electronics, Republic of Korea

**JFS2.7** - A 1.96Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems

Chen-Chien Kao, National Taiwan University, Taiwan

**JFS3 - STCO/DTCO**

**Session Chairs:** Seung-Chul Song (Qualcomm Technologies), Keilichi Meekawa (Renesas Electronics)

**JFS3.1** (invited) - Heterogeneous System-Level Package Integration – Trends and Challenges

Frank Lee, TSMC, Taiwan

**JFS3.2** (invited) - Can We Ever Get to a 100nm Tall Library? Power Rail Design for Tnm Technology Node

Victor Moroz, Synopsys, USA

**JFS3.3** - Burred Powered SRAM DTCO and System-Level Benchmarking in N3

Sharife Salahuddin, imec, Belgium

**JFS3.4** - Local Variation-Aware Transistor Design through Comprehensive Analysis of Various Vdd/Temperatures Using Sub-Tnm Advanced FinFET Technology

Soyoun Kim, Samsung Electronics, Republic of Korea

**JFS4 - Devices and Circuits for AI/ML**

**Session Chairs:** Edith Beigne (Facebook), Vijay Narayan (IBM), Nicky Lu (Elron Technology), Huaqiang Wu (Tsinghua University)

**JFS4.1** - SOT-MRAM Based Analog in-Memory Computing for DNN Inference

Jonas Doevenspeck, imec, ESAT-Katholieke Universiteit Leuven, Belgium

**JFS4.2** - Compact Probabilistic Poisson Neuron Based on Back-Hopping Oscillation in STT-MRAM for All-Synaptic Deep Spiking Neural Network

Ming-Hung Wu, National Chiao Tung University, Taiwan

**JFS4.3** - An All-Weights-on-chip UNN Accelerator in 22nm ULL Featuring 24×1 Mb eMRAM

Zhehong Wang, University of Michigan, USA

**JFS4.4** - PNP: A 146.52TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping

Sangyeob Kim, Korea Advanced Institute of Science and Technology, Republic of Korea

**JFS4.5** - A Mixed-Signal Time-Domain Generative Adversarial Network Accelerator with Efficient Subthreshold Time Multiplier and Mixed-signal On-chip Training for Low Power Edge

Zhengyu Chen, Northwestern University, USA

**JFS5 - Heterogeneous Integration**

**Session Chairs:** Carlos Tokunaga (Intel), Greg Yeric (Arm), Masanao Yamaoka (Hitachi), Tetsu Tanaka (Tohoku University)

**JFS5.1** - Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry. Multi-Tier Complementary Carbon Nanotube Logic and Resistive RAM at a 130 nm Node

Tathagata Srinant, Massachusetts Institute of Technology, USA

**JFS5.2** - A 1.8Gb/s/16T NAND Flash Memory Multi-Chip Package with F-Chip of Toggle 4.0 Specification for High Performance and High Capacity Storage Systems

Daehoon Na, Samsung Electronics, Republic of Korea

**JFS5.3** - A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-g Measurement Capability and Low Bias Instability

Xiaoliang Li, Carnegie Mellon University, USA

**JFS5.4** - A 3D-Stacked Cortex-M0 SoC with 20.3Gbps/mm2 7.1mW/mm2 Simultaneous Wireless Inter-Tier Data and Power Transfer

Benjamin Fletcher, University of Southampton, United Kingdom

**JFS5.5** - Heterogeneous Power Delivery for Tnm High-Performance Chiplet-Based Processors Using Integrated Passive Device and In-Packgage Voltage Regulator

Alan Roth, TSMC, USA

**DEMO SESSION**

**Session Chairs:** Rob Aitken (Arm), Vijay Narayan (IBM), Tomohiro Takahashi (Sony Semiconductor Solutions), Koji Hamada (Micron)

5-minute videos by participating authors

**CB1.4** - 1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-chip with Dynamic Incremental-SAR Acquisition

Jun Wang, University of California San Diego, USA

**CB1.5** (invited) - High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at 11.72μm Pitch for Neuronal Network Analysis

Yuri Kato, Sony Semiconductor Solutions, Japan

**CB2.1** (invited) - A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR

Tuan Thanh Ta, Toshiba, Japan

**CB3.4** - A 0.72μW, 1Sample/s Fully Integrated pH Sensor with 65.8LSB/pH Sensitivity

Yifan Zhang, Columbia University, USA

**CG2.3** - Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting

Massimo Aiolio, National University of Singapore, Singapore

**CP3.6** - A Domino Bootstraping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 98% High Efficiency

Hsuan-Yu Chen, National Chiao Tung University, Taiwan

**JFS1.4** - IVV-on-Bulk Si Technology for Commercially Viable Photonics-Integrated VLSI

Dongjia Shin, Samsung Advanced Institute of Technology, Republic of Korea

**JFS2.1** (invited) - Hardware-Software Co-integration for Configurable 5G mmWave Systems

Alberto Valdes-Garcia, IBM, USA

**JFS5.3** - A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-g Measurement Capability and Low Bias Instability

Xiaoliang Li, Carnegie Mellon University, USA

**TM2.2** - A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing

Weier Wan, Stanford University, USA

**TNT1.3** - Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFET for Advanced Hardware Security

Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China
## Technology Sessions

### THL - Highlight Session

| Session Chairs: Gosia Jurczak (Lam Research), Munehiro Tada (NEC) |
|------------------------|---------------------------------------------------------------------|
| THL.1 - 5G and AI Integrated High Performance Mobile SoC Process-Design Co-Development and Production with 7nm EUV FinFET Technology | Jie Deng, Qualcomm Technologies, USA |
| THL.2 - GaN and Si Transistors on 300mm Si(111) enabled by 3D Monolithic Heterogeneous Integration | Han Wui, TSMC, Taiwan |
| THL.3 - An Optically Sampled ADC in 3D Integrated Silicon-Photonic/65nm CMOS | Nandish Mehta, University of California, Berkeley, USA |
| THL.4 - A Monolithic 3D Integration of RRAM Array with Oxide Semiconductor FET for In-Memory Computing in Quantized Neural Network AI Applications | Joxian Wu, University of Tokyo, Japan |
| THL.5 - Improved Air Spacers Co-Integrated with Self-Aligned Contact (SAC) and Contact Over Active Gate (COAG) for Highly Scaled CMOS Technology | Kangguo Cheng, IBM, USA |
| THL.6 - Buried Power Rail Integration with Si FinFETs for CMOS Scaling Beyond the 5nm Node | Anshul Gupta, imec, Belgium |

### TC1 - Advanced Si CMOS Devices

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<td>TC1.2 - 7-Levels Stacked Nanosheet GAA Transistors for High Performance Computing</td>
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<td>TC1.3 - Cold CMOS as a Power-Performance-Reliability Booster for Advanced FinFETs</td>
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<td>TC1.4 - All-Operation-Regime Characterization and Modeling of Drain Current Variability in Junctionless and Inversion-Mode FDSOI Transistors</td>
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### TC2 - Ge and SiGe Devices

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<td>TC2.2 - Addressing Key Challenges for SiGe-pFin Technologies: Fin Integrity, Low-D$_i$ Si-cap-free Gate Stack and Optimizing the Channel Strain</td>
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<td>TC2.3 - First Demonstration of 4-Stacked Ge$<em>x$Si$</em>{1-x}$ nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels</td>
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<td>TC2.4 - Vertical Heterojunction Ge$<em>{0.5}$Si$</em>{0.5}$GaN/Ge GAAN Nanowire MOSFETs: Low SS of 87mV/dec, Small DIBL of 24mV/V and Highest G$_{max}$ of 870μS/μm</td>
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<td>TC2.5 - Structural and Electrical Demonstration of SiGe Cladded Channel for PMOS Stacked Nanosheet Gate-All-Around Devices</td>
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### TC3 - Advanced Processing

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<td>TC3.1 - Materials Technology Co-Optimization of Self-Aligned Gate Contact for Advanced CMOS Technology Nodes</td>
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<td>TC3.2 - Selective Enablement of Dual Dipoles for Near Bandedge Multi-V, Solution in High Performance FinFET and Nanosheet Technologies</td>
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<td>TC3.3 - Composite Interconnects for High-Performance Computing Beyond the 7nm Node</td>
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<td>TC3.4 - Record Low Contact Resistivity to Ge:B (8.1x10$^{-10}$ Ω-cm) and GeSn:B (4.1x10$^{-10}$ Ω-cm) with Optimized [B] and [Sn] by In-situ CVD Doping</td>
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<td>TC3.5 - High Quality N+P Junction of Ge Substrate Prepared by Initiated CVD Doping Process</td>
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<td>TC3.6 - Ultra-low $p_t$ Extraction for Recessed and Non-Recessed Contacts: Generalized Transmission Line Model</td>
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### TF1 - FeFETs

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<td>TF1.2 - Re-Examination of $V_{th}$ Window and Reliability in HfO$_2$ FeFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation</td>
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<td>TF1.3 - Hot Electrons as the Dominant Source of Degradation for Sub-5nm HZO FeFETs</td>
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<td>TF1.4 - A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation</td>
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<td>TF1.5 - Asymmetric Polarization Response of Electrons and Holes in Si FeFETs: Demonstration of Absolute Polarization Hysteresis Loop and Inversion Hole Density Over $2\times10^{13}$ cm$^{-2}$</td>
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### TF2 - Ferroelectric Memory and Capacitors

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<td>TF2.2 - A Novel Dual Ferroelectric Layer Based MFMFIS FeFET with Optimal Stack Tuning Toward Low Power and High-Speed NVM for Neurocomputing Applications</td>
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<td>TF2.3 - Improved State Stability of HfO, Ferroelectric Tunnel Junction by Template-Induced Crystalization and Remote Scavenging for Efficient In-Memory Reinforcement Learning</td>
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<td>TF2.4 - Nanosecond Laser Anneal (NLA) for Si-Implanted HfO$_2$ Ferroelectric Memories Integrated in Back-End Of Line (BEOL)</td>
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<td>TF2.5 - Fast Thermal Quenching on the Ferroelectric Al: HfO$_2$ Thin Film with Record Polarization Density and Flash Memory Application</td>
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<td>TF2.6 - Multi-Probe Characterization of Ferroelectric/Dielectric Interface by C-V, P-V and Conductance Methods</td>
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<td>TF2.7 - Probing the Evolution of Electrically Active Defects in Doped Ferroelectric HfO$_2$ During Wake-Up and Fatigue</td>
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<td>TF2.8 - Atomic-Scale Imaging of Polarization Switching in an (Anti-)Ferroelectric Memory Material: Zirconia (ZrO$_2$)</td>
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TH1 - 3D Packaging

TH1.1 - Low Temperature SiOC Bonding and Stacking Technology for 12/16Hi High Bandwidth Memory (HBM)
C.H. Tsai, TSMC, Taiwan

TH1.2 - 3D Heterogeneous Package Integration of Air/Magnetic Core Inductor: 85%-Efficiency Buck Converter with Backside Power Delivery Network
Xiao Sun, imec, Belgium

TH1.3 - Bumpless Build Cube (BBCube): High-Parallelism, High-Dissipation and Low-Power Stacked Memory Using Water-Level 3D Integration Process
Nori Chuo, Tokyo Institute of Technology, IIR, WOW Alliance / Hitachi, Japan

TH1.4 - ExaNoDe: Combined Integration of Chips-on Active Interposer with Bare Dice in a Multi-Chip-Module for Heterogeneous and Scalable High Performance Compute Nodes
Pierre-Yves Martinez, Université Grenoble Alpes, CEA-LIST, France

TH1.5 - Immersion in Memory Compute (IMc) Technology
C.T. Wang, TSMC, Taiwan

TH1.6 - Low Temperature Cu/3SiO2 Hybrid Bonding with Metal Passivation
Demin Liu, National Chiao Tung University, Taiwan

TH2 - Semiconducting Oxides for 3D Integration

TH2.1 - BEOL Compatible Dual-Gate Ultra Thin-Body W-Doped Indium-Oxide Transistor with Ion=370µA/µm, SS=73mV/dec and Ion/Ioff ratio 4x10^9
Wridddi Chakraborty, University of Notre Dame, USA

TH2.2 - Surrounding Gate Vertical-Channel FET with Gate Length of 40nm Using BEOL Compatible High-Thermal-Tolerance In-Al-Zn Oxide Channel
Hirokazu Fujiwara, Kioxia, Japan

TH2.3 - Amorphous SiO2 TFTs featuring Extremely-Scaled Channel Thickness and 38nm Channel Length: Achieving Record High G_{on,38nm} of 125 µS/µm at V_{DS} of 1V and I_{ON} of 350µA/µm
Subhranu Samanta, National University of Singapore, Singapore

TH3 - Si Technologies for 3D Integration

TH3.1 - First Monolithic Integration of 3D Complementary FET (CFET) on 300mm Wafers
Sujith Subramanian, imec, Belgium

TH3.2 - 3D Sequential Low Temperature Top Tier Devices Using Dopant Activation with Excimer Laser Anneal and Strained Silicon as Performance Boosters
Anne Vandooren, imec, Belgium

TH3.3 - 28nm FDSOI CMOS Technology (FEOL and BEOL) Thermal Stability for 3D Sequential Integration: Yield and Reliability Analysis
Camila Cavalcante, CEA-Leti, France

TH3.4 - First Demonstration of Low Temperature (<500°C) CMOS Devices Featuring Functional RO and SRAM Bitcells toward 3D VLSI Integration
Claire Fenouillet-Beranger, CEA-Leti-MINATEC, France

TH3.5 - Flexible and Transparent BEOL Monolithic 3DIC Technology for Human Skin Adaptable Internet of Things Chips
Ming-Hsuan Kao, Taiwan Semiconductor Research Institute, Taiwan

TM1 - Memory - NAND/NOR/PCM

TM1.1 - An Extremely Scaled Hemi-Cylindrical (HC) 3D NAND Device with Large Vt Memory Window (>10V) and Excellent 100k Endurance
Pei-Ying Du, Macronix International, Taiwan

TM1.2 - An Approach to Embedding Traditional Non-Volatile Memories into a Deep Sub-Micron CMOS
Chia-Sheng Lin, TSMC, Taiwan

TM1.3 - A Vertical 2T NOR (V2T) Architecture to Enable Scaling and Low-Power Solutions for NOR Flash Technology
Hang-Ting Lue, Macronix International, Taiwan

TM1.4 - Understanding of Tunable Selector Performance in Si-Ge-As-Se OTS Devices by Extended Percolation Cluster Model Considering Operation Scheme and Material Design
Shoichi Kabuyanagi, Kioxia, imec, Japan

TM1.5 - A No-Verification Multi-Level-Cell (MLC) Operation in Cross-Point OTS-PCM
Nanbo Gong, IBM T. J. Watson Research Center, USA

TM1.6 - Si Incorporation Into AsSeGe Chalcogenides for High Thermal Stability, High Endurance and Extremely Low Vth Drift 3D Stackable Cross-Point Memory
Hual-Yu Cheng, Macronix International, Taiwan

TM2 - Memory - RRAM

TM2.1 - A SiO2 RRAM-Based Hardware with Spike Frequency Adaptation for Power-Saving Continual Learning in Convolutional Neural Networks
Irene Munoz-Martin, Politecnico di Milano, Italy

TM2.2 - A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing
Weiier Wan, Stanford University, USA

TM2.3 - Industrially Applicable Read Disturb Model and Performance on Mega-Bit 28nm Embedded RRAM
Chang-Feng Yang, TSMC, Taiwan

TM3 - Memory - STT MRAM

TM3.1 - Scalability of Quad Interface p-MTJ for 1X nm STT-MRAM with 10ns Low Power Write Operation, 10 years Retention and Endurance > 10^11
Sadaok Miura, Tohoku University, Japan

TM3.2 - Reliability Demonstration of Rfeff Qualified 22nm STT-MRAM for Embedded Memory Applications
Chia-Yu Wang, TSMC, Taiwan

TM3.3 - Fast Switching of STT-MRAM to Realize High Speed Applications
Tae Young Lee, GlobalFoundries, Singapore

TM3.4 - A Reliable TDB Lifetime Projection Model Verified Using 40Mb STT-MRAM Macro at Sub-mm Failure Rate to Realize Unlimited Endurance for Cache Applications
Vinayak Bharat Naik, GlobalFoundries, Singapore

TMFS - MRAM Future - Opportunities Beyond STT

TMFS.1 (Invited) - Recent Progresses in STT-MRAM and SOFT-MRAM for Next Generation MRAM
Tetsuo Endoh, Tohoku University, Japan

TMFS.2 (Invited) - Magnetic Random Access Memories (MRAM) Beyond Information Storage
Ricardo Sousa, Université Grenoble Alpes / CEA / CNRS, Spintec, France

TMFS.3 - CMOS Compatible Process Integration of STT-MRAM with Heavy-Metal Bi-Layer Bottom Electrode and 10ns Field-Free SOT Switching with STT Assist
Noryuki Sato, Intel, USA

TMFS.4 - Deterministic and Field-Free Voltage-Controlled MRAM for High Performance and Low Power Applications
Yueh Chang Wu, imec, Belgium
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<td>TN1.1 - Hair-Like Nanostructure Based Ion Detector by 16nm FinFET Technology</td>
<td>Chien-Ping Wang, National Tsing Hua University, Taiwan</td>
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<td>TN1.2 - Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry</td>
<td>Chia-Che Chung, National Taiwan University, Taiwan</td>
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<td>TN1.3 - Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFET for Advanced Hardware Security</td>
<td>Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China</td>
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<td>TN1.4 - A Bias and Correlation-Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking</td>
<td>Kai Ni, Rochester Institute of Technology, USA</td>
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<td>TN1.5 - 1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy</td>
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<td>TN1.6 - Proposal and Experimental Demonstration of Reservoir Computing Using Hf$<em>{0.5}$Zr$</em>{0.5}$O$_2$/SiFeFETs for Neuromorphic Applications</td>
<td>Eishin Nako, University of Tokyo, Japan</td>
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<td>TN1.7 - High On-Current 2D nFET of 390μA/μm at V$_{DS}$ = 1V using Monolayer CVD MoS$_2$ Without Intentional Doping</td>
<td>Ang-Sheng Chou, TSMC, Taiwan</td>
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<td>TN1.8 - Ultrahigh Responsivity and Tunable Photogain BEOL Compatible MoS$_2$ Phototransistor Array for Monolithic 3D Image Sensor with Block-Level Sensing Circuits</td>
<td>Chih-Chao Yang, Taiwan Semiconductor Research Institute, Taiwan</td>
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<td>TN1.9 - GaN PMIC Opportunities: Characterization of Analog and Digital Building Blocks in a 650V GaN-on-Si Platform</td>
<td>Wan Lin Jiang, University of Toronto, Canada</td>
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<td>TN2.1 - Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures Down to 100mk for Quantum Computing</td>
<td>Bruna Paz, CEA-Leti-MINATEC, France</td>
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<td>TN2.2 - Toward Long-Coherence-Time Si Spin Qubit: The Origin of Low-Frequency Noise in Cryo-CMOS</td>
<td>Hiroshi Oka, National Institute of Advanced Industrial Science and Technology, Japan</td>
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## Circuits Sessions

### CA1 - Machine Learning

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<td>A 3.0 TFLOPS 0.62V Scalable Processor Core for High Compute Utilization AI Training and Inference</td>
<td>Sae Kyu Lee, IBM T. J. Watson Research Center, USA</td>
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<td>A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS</td>
<td>Phil Knag, Intel, USA</td>
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<td>An Ultra-Low Latency 7.8-13.6 pJ/6 Reconfigurable Neural Network-Assisted Polar Decoder with Multi-Code Length Support</td>
<td>Chieh-Fang Teng, National Taiwan University, Taiwan</td>
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<td>A 4.45ms Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices</td>
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### CA2 - Visual Processing & AI

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<td>A 170µW Image Signal Processor Enabling Hierarchical Image Recognition for Intelligence at the Edge</td>
<td>Hyochan An, University of Michigan, USA</td>
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<td>A 0.055/J/Pixel 70fps FHD 1Meps Event-Driven Visual Data Processing Unit</td>
<td>Somnath Paul, Intel, USA</td>
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<tr>
<td>65nm Image Processing SoC Supporting Multiple DNN Models and Real-Time Communication-Communication Trade-Off via Actor-Critical Neuro-Controller</td>
<td>Ningyuan Cao, Georgia Institute of Technology, USA</td>
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<td>Ray-Casting Accelerator in 10nm CMOS for Efficient 3D Scene Reconstruction in Edge Robotics and Augmented Reality Applications</td>
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<td>A 1200x1200 8-Edges/Vertex FPGA-Based Motion-Planning Accelerator for Dual-Arm-Robot Manipulation Systems</td>
<td>Takashi Oshima, Hitachi, Japan</td>
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<td>Peng Wang, University of Virginia, USA</td>
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<td>Artificial Iris ASIC with High Voltage Liquid Crystal Driver, 10mA Light Range Detector and 40nA Blink Detector for LCD Flicker Removal</td>
<td>Bogdan Raducanu, imec, Belgium</td>
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<td>A Probabilistic Self-Annealing Compute Fabric based on 560 Hexagonally Coupled Ring Oscillators for Solving Combinatorial Optimization Problems</td>
<td>Ibrahim Ahmed, University of Minnesota, USA</td>
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<td>A Monolithic Adiabatic Integration Architecture Microprocessor Using 1.4J/op Superconductor Josephson Junction Devices</td>
<td>Christopher Ayala, Yokohama National University, Japan</td>
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<td>32GHz 6.5mW Gate-Level-Pipelined 4-bit Processor using Superconductor Single-Flux-Quantum Logic</td>
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### CB1 - Biomedical Sensors

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### CB2 - Image Sensor & Imaging Techniques

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### CB3 - Physical Sensors

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<td>A 785nm Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring</td>
<td>Peng Wang, University of Virginia, USA</td>
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<td>A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS</td>
<td>Phil Knag, Intel, USA</td>
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<td>An Ultra-Low Latency 7.8-13.6 pJ/6 Reconfigurable Neural Network-Assisted Polar Decoder with Multi-Code Length Support</td>
<td>Chieh-Fang Teng, National Taiwan University, Taiwan</td>
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<td>A 4.45ms Low-Latency 3D Point-Cloud-Based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices</td>
<td>Dongsuk Im, Korea Advanced Institute of Science and Technology, Republic of Korea</td>
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<td>A 3m² Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception Using Parallel Gibbs Sampling in 16nm</td>
<td>Glenn G. Ko, Harvard University, USA</td>
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### CC1 - Circuits for Security and Safety

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<td>Rob Atken (Arm), Mototsugu Hamada (University of Tokyo)</td>
<td>CC1.1 - A Performance-Flexible Energy-Optimized Automotive-Grade Cortex-R4F SoC through combined AVS/ABB/Bias-in-Memory-Array Closed-Loop Regulation in 28nm FD-SOI</td>
<td>Ricardo Gomez Gomez, STMicroelectronics, France</td>
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<td>CC1.2 - A Stability-Aware AES Engine in 14nm CMOS with Time/Frequency-Domain Leakage Suppression Using Non-linear Digital LDO Cascade and Arithmetic Countermeasures</td>
<td>Raghavan Kumar, Intel, USA</td>
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<td>CC1.3 - A 0.26% BER, 10&lt;sup&gt;th&lt;/sup&gt; Challenge-Response Machine-Learning Resistant Strong-PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection</td>
<td>Vikram Suresh, Intel, USA</td>
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<td>CC1.4 - A 435MHz, 2.5Mbps Side-Channel-Attack Resistant Crypto-Processor for Secure RSA-4K Public-Key Encryption in 14nm CMOS</td>
<td>Raghavan Kumar, Intel, USA</td>
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### CC2 - Adaptive Clocking and Power Delivery

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<td>Vijay Kiran Kalyanam, Qualcomm Technologies, USA</td>
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<td>CC2.2 - An Autonomous Reconfigurable Power Delivery Network (RPDN) for Many-Core SoCs Featuring Dynamic Current Steering</td>
<td>Khondker Ahmed, Intel, USA</td>
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<td>CC2.3 - Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1mW and Sustained Operation under Moonlight Harvesting</td>
<td>Massimo Alito, National University of Singapore, Singapore</td>
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<td>CC2.4 - UniCap-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in Designs with Large Clock Distribution Delays in 65nm CMOS</td>
<td>Xun Sun, University of Washington, USA</td>
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### CD1 - High-Speed Data Converters

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<td>Stacy Ho (MediaTek), Tomohiro Nezuka (MRRI Technologies)</td>
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<td>Benjamin Hershberg, imec, Belgium</td>
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<td>CD1.2 - A 10-bit 100Ms/s SAR ADC with Always-on Reference Ripple Cancellation</td>
<td>Xiyuan Tang, University of Texas at Austin, USA</td>
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<td>CD1.3 - An 8b 1Gs/s 2.55MHz SAR-Flash ADC with Complementary Dynamic Amplifiers</td>
<td>Dong-Ryeol Oh, Korea Advanced Institute of Science and Technology, Korea</td>
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<td>CD1.4 - A 177M/s 10GS/s NRZ DAC with Switching-Glitch Compensation Achieving &gt;64dBc SFDR and &lt;-77dBc IM3</td>
<td>Hung-Yi Huang, National Cheng Kung University, Taiwan</td>
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<td>CD1.5 - A Compact 14GS/s 8-bit Switched-Capacitor DAC in 16nm FinFET CMOS</td>
<td>Pietro Caragiuolo, Stanford University, USA</td>
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<td>Efrain Elord, Deft University of Technology, Netherlands</td>
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<td>CD2.2 - A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved Second-Order ΔΣ Modulator with Digital Feedback Extrapolation in 28nm CMOS</td>
<td>Dongyang Jiang, University of Macau, Macao</td>
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<td>CD2.3 - A 10.4mW 50MHz-BW 80dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp</td>
<td>Kai Xing, University of Macau, China</td>
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<td>CD2.4 - A 1GS/s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9dB FoMs</td>
<td>Yifan Lyu, MICS-Katholieke Universiteit Leuven, Belgium</td>
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<td>CD2.5 - A SAR ADC with Reduced 1.19% Noise by Decoupling Noise PSD and BW</td>
<td>Zhefu Li, Zhejiang University, University of Texas at Austin, China</td>
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<td>Christoph Sandner (Infineon), Kenichi Okada (Tokyo Institute of Technology)</td>
<td>CF1.1 - Embedded PLL Phase Noise Measurement Based on a PDF/DCP MASH 1+1-1 ΔΣ Time-to-Digital Converter in 7nm CMOS</td>
<td>Mao-Hsuwan Chou, TSMC, Taiwan</td>
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<td>CF1.2 - A Fast Locking 5.8-7.2 GHz Fractional-N Synthesizer with Sub-2ps Settling Time in 22nm FD-SOI</td>
<td>Jeffrey Prinzie, Katholieke Universiteit Leuven, Belgium</td>
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<td>CF1.3 - A 4GHz 0.73ps&lt;sub&gt;max&lt;/sub&gt;, Integrated-Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring PLL with a Jitter-Tracking DLL-Assisted DTC</td>
<td>Jaeheong Jung, Samsung Electronics, Republic of Korea</td>
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<td>CF1.4 - A 3.3GHz 101fs&lt;sub&gt;max&lt;/sub&gt;, Integrated-Jitter &lt; -250 dBc FOM Fractional-N DPLL with Phase Error Detection Accomplished in Fully Differential Voltage Domain</td>
<td>Lianbo Wu, ETH Zurich, Switzerland</td>
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<td>Masaru Osada, University of Tokyo, Japan</td>
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<td>CF2.1 - A 29% PAE 1.5-bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked PLLs</td>
<td>Yuncheng Zhang, Tokyo Institute of Technology, Japan</td>
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<td>CF2.2 - A 28GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation</td>
<td>Jian Pang, Tokyo Institute of Technology, Japan</td>
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<td>CF2.3 - A 293/440GHz Push-Push Double Feedback Oscillators with 90/-3.6dBm Output Power and 2.9%/0.6% DC-to-RF Efficiency in 28nm CMOS</td>
<td>Dae-Woong Park, imec, Belgium</td>
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<td>CF2.4 - A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-Quasi-Cascode Technique</td>
<td>Jaehong Jung, Samsung Electronics, Republic of Korea</td>
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<td>CF2.5 - 315GHz Self-Synchronizing Minimum Shift Keying Receiver in 65nm CMOS</td>
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<td>CF3.1 - A 1.7MOPS-36GOPS Adaptive Versatile to IoT Node with 15,000x Peak-to-Idle Power Reduction, 207s Wake-Up Time and 1.3TPS/WS ML Efficiency</td>
<td>Iwan Miro-Parades, Université Grenoble Alpes, CEA, LIST, France</td>
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<td>CF3.2 - (Invited) - Industrial IoT with Crystal-Free Mote-on-Chip</td>
<td>Thomas Watteyne, Inria, France</td>
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<td>CF3.3 - A Multichannel, MEMS-Less, −99dBm 260MHz Bit-level Duty Cycled Wakeup Receiver</td>
<td>Anjana Dissanyake, University of Virginia, USA</td>
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<td>CF3.4 - A 4.4GHz -92/-90.3dBm Sensitivity Dual-mode BLE/Wi-Fi Wake-Up Receiver</td>
<td>Po-Han Peter Wang, University of California San Diego, USA</td>
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<td>CF3.5 - A 920MHz 16-FSK Receiver Achieving a Sensitivity of −103dBm at 0.6mW via an Integrated N-Path Filter Bank</td>
<td>Ali Nikoofard, University of California San Diego, USA</td>
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<td>CF4.1 - A 8.7ppm/°C, 694nW, One-Point Calibrated RC Oscillator Using a Nonlinearity-Aware Dual Phase-Locked Loop and DSM-Controlled Frequency-Locked Loops</td>
<td>Giorgio Cristiano, ETH Zürich, Switzerland</td>
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<td>CF4.2 - A 0.5V 560kHz 18.8fJ/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop</td>
<td>Daniel Truesdell, University of Virginia, USA</td>
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<td>CF4.3 - A 0.9ppm/cycle 8ppm/°C DLL-based Wakeup Timer Enabled by a Time-Domain Trimming and an Embedded Temperature Sensing</td>
<td>Ming Ding, imec, Belgium</td>
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**Session Chairs:** Igor Arsovski (Marvell), Tsung-Yung Jonathan Chang (TSMC)

- **CM1.1** - A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 173mV VMIN Reduction with Negligible Power Overhead
  - Zheng Guo, Intel, USA

- **CM1.2** - A 29nm /mm² Ultra High Density SRAM Macro Using 7nm FinFET Technology with Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit
  - Yoshihito Yokoyama, Renesas Electronics, Japan

- **CM1.3** - Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1R1W 8t-bitcell SRAM in 10nm FinFET CMOS
  - Jaydeep Kulkarni, Intel, USA

- **CM1.4** - 2X-Bandwidth Burst 6t-SRAM for Memory Bandwidth Limited Workloads
  - Charles Augustine, Intel, USA

- **CM1.5** - A 7nm FinFET 4.04-Mb/mm² TCM with Improved Electromigration Reliability Using Far-Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier
  - Makoto Yabuchi, Renesas Electronics, Japan

**CM2 - Emerging Memory Design**

**Session Chairs:** Seung Kang (Qualcomm Technologies), Makoto Miyamura (NEC)

- **CM2.1** - A 14.7/mm² 28nm FDSOI STT-MRAM with Current Starved Read Path, 52Ω/σ Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference
  - El Mehdi Boujamaa, Arm, France

- **CM2.2** - Dual-Port Field-Free SST-MRAM Achieving 90dB Read and 60MHz Write Operations Under 55nm CMOS Technology and 1.2V Supply Voltage
  - Masanori Natsui, Tohoku University, Japan

- **CM2.3** - A 28nm 1.5Mb Embedded 1T2R RAM with 14.8Mb Using Slewing Current Suppression and Compensation Techniques
  - Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China

- **CM2.4** - A 22nm 98×144 8t-DRAM Macro with a Self-Tracking Reference and a Low Ripple Charge Pump to Achieve a Configurable Read Window and a Wide Operating Voltage Range
  - Chung-Cheng Chou, TSMC, Taiwan

**CM3 - Energy Efficient Memory Design**

**Session Chairs:** John Wu (AMD), Kyomin Sohn (Samsung Electronics)

- **CM3.1** - A 28nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation
  - Hoyoung Shin, Samsung Electronics, Republic of Korea

- **CM3.2** - A 65nm 16kB SRAM with 13T,5pW Leakage at 0.9V for Wireless IoT Sensor Nodes
  - Shourya Gupta, University of Virginia, USA

- **CM3.3** - A 0.3pJ/Word Ultra-Low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors
  - Jingcheng Wang, University of Michigan, USA

- **CM3.4** - Z-PIM: An Energy-Efficient Sparsity-Aware Processing-In-Memory Architecture with Fully-Variable Weight Precision
  - Ji-Hoon Kim, Korea Advanced Institute of Science and Technology, Republic of Korea

**CP1 - Amplifiers**

**Session Chairs:** Hylas Lam (Analog Devices), Kuan-Dar Chen (MediaTek)

- **CP1.1** - A ~108Ω 8T 8Ω-Multi-Level Class-D Audio Amplifier
  - Hujun Zhang, Delft University of Technology, Netherlands

- **CP1.2** - An 8Ω, 1.4W, 0.0024% THD+N Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Modes Achieving Low Standby Quiescent Current of 650µA
  - Ji-Hun Lee, Korea Advanced Institute of Science and Technology, Republic of Korea

- **CP1.3** - Sample and Average Common-Mode Feedback in a 101mV Acoustic Amplifier
  - Rolf Roth, University of Michigan, USA

- **CP1.4** - A 0.0046mm² 6.7µW Three-Stage Amplifier Capable of Driving 0.5-to-1.9nF Capacitive Load with >0.68MHz GBW without Compensation Zero
  - Hongsik Shin, Korea Advanced Institute of Science and Technology, Republic of Korea

**CP2 - Voltages References and Wireless Power**

**Session Chairs:** Patrick Mercier (California San Diego), Sung-Wan Hong (Soookyung Women’s University)

- **CP2.1** - A Single-Term Switched Capacitor CMOS Bandgap Reference with a 3σ Inaccuracy of ±0.02%, ±0.12% for Battery Monitoring Applications
  - Jun-Ho Boo, Sogang University, Republic of Korea

- **CP2.2** - A 0.25-V, 5.3-pW Voltage Reference with 25µV/°C Temperature Coefficient, 140µV/°C Line Sensitivity and 2.200µm² Area in 180nm CMOS
  - Longyan Lin, National University of Singapore, Singapore

- **CP2.3** - A 6.7mW Wireless Power Transfer System Enabling Perpendicular Wireless Powering with Efficiency Increase from 0.02% to 48.2% by Adaptive Magnetic Field Adder IC Integrating Shared Coupling Coefficient Sensor
  - Hau Guo, University of Tokyo, Japan

- **CP2.4** - A 120-330V, Sub-µA, 4-Channel Driver for Microrobotic Actuators with Wireless-Optical Power Delivery and Over 99% Current Efficiency
  - Jan Rentmeester, Dartmouth College, USA

**CP3 - Power Converters**

**Session Chairs:** Xirong Zhang (IBM), Po-Hung Chen (National Chiao Tung University)

- **CP3.1** - An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching
  - Dong Yan, University of Texas at Dallas, USA

- **CP3.2** - Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 65nm CMOS
  - Xun Sun, University of Washington, USA

- **CP3.3** - An N-Path Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting Achieving 13.9x Power Extraction Improvement
  - Loai Salem, University of California Santa Barbara, USA

- **CP3.4** - A 4V-0.55V Input Fully Integrated Switched-Capacitor Converter Enabling Dynamic Voltage Domain Stacking and Achieving 80.1% Average Efficiency
  - Tim Thielemans, MICS-Katholieke Universiteit Leuven, Belgium

- **CP3.5** - A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency
  - Xiaosen Liu, Intel, USA

- **CP3.6** - A Domino Bootstrapping 12V GaN Driver for Driving an On-Chip 650V eGaN Power Switch for 96% High Efficiency
  - Hsuan-Yu Chen, National Chiao Tung University, Taiwan

**CW1 - Ultra-High-Speed Wireline**

**Session Chairs:** Jon Proesel (IBM), Ji Lee (National Taiwan University)

- **CW1.1** - A 4×112 Gb/s ADC-DSP Based Multistandard Receiver in 7nm FinFET
  - Haidong Lin, Intel, USA

- **CW1.2** - A 25-50Gb/s 2.222pJ/byte NRZ RX with Dual-Bank and 3-tap Speculative DFE for Microprocessor Application in 7nm FinFET CMOS
  - Yang You, IBM, USA

- **CW1.3** - A 4-to-16GHz Active Poly Phase Filter Quadrature Clock Generator with Phase Error Correction in 5nm CMOS
  - Wei-Chih Chen, TSMC, Taiwan

**CW2 - Wireline Techniques**

**Session Chairs:** Parag Upadhyaya (Xilinx), Patrick Yue (Hong Kong University of Science and Technology)

- **CW2.1** - A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ Calibration for Memory Interfaces
  - Yong-Jn Jeong, Seoul National University, Republic of Korea

- **CW2.2** - A 0.1pJ/µbit 28Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler
  - Moon-Chul Choi, Seoul National University, Republic of Korea

- **CW2.3** - Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20Gb/s 5b ENOB Analog-to-Digital Converter and 5GHz Phase Interpolator
  - Sung-Jin Kim, Stanford University, USA

- **CW2.4** - A 28mW 32Gb/s/pin 15-QAM Single-Ended Transceiver for High-Speed Memory Interface
  - Jieqiong Du, University of California Los Angeles, USA
### Workshops

#### WS1 Workshop - Analog Computing Technologies and Circuits for Efficient Machine Learning Hardware
**Organizers:** Arindam Mallik (imec), Nadine Collaert (imec)

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<td>Boris Murmann, Stanford University, USA</td>
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<td>Designing Material Systems and Algorithms for Analog Computing</td>
<td>Robert L. Bruce, IBM Research, USA</td>
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<td>Monolithically Integrated RRAM-based Analog/ Mixed-Signal In-Memory Computing for Energy-Efficient Deep Learning</td>
<td>Jae-Sun Seo, Arizona State University, USA</td>
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<td>Jaydeep Kulkarni, University of Texas at Austin, USA</td>
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<td>Arindam Mallik, imec, Belgium</td>
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<td>System and Architecture Level Considerations in Leveraging Mixed-Signal Techniques for ML at the Edge</td>
<td>Mahesh Mehendale, Texas Instruments, USA</td>
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#### WS2 Workshop - Know Where You Are Going; Metrology In the New Age of Semiconductor Manufacturing
**Organizers:** Tom Larson (Nova Measuring Instruments), Gosia Jurczak (Lam Research)

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<td>Manufacturing Process Challenges and Requirements for Metrology in Semiconductor Memory Devices</td>
<td>Keiji Suzuki, Kioxia, Japan</td>
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<td>Yi Hung Lin, TSMC, Taiwan</td>
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<td>Dimensional Metrology Overview, Trends and Upcoming Challenges</td>
<td>Philippe Leray, imec, Belgium</td>
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<td>Mark Shirey, KLA, USA</td>
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<td>Enabling Modern Semiconductor Manufacturing With Materials Metrology</td>
<td>Kavita Shah, Nova Measuring Instruments, USA</td>
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<td>Opportunities and Challenges for Lab-based Characterization for Emerging Technologies</td>
<td>Markus Kuhn, Intel, USA</td>
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#### WS3 Workshop - Quantum Computers for Electrical Engineers
**Organizers:** Maud Vinet (CEA-Leti), Iuliana Radu (imec)

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<td>William Oliver, Massachusetts Institute of Technology, USA</td>
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<td>Doug McClure, IBM, USA</td>
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<td>Iuliana Radu, imec, Belgium</td>
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<td>WS3.4</td>
<td>Architectures Challenges for Si Spin Qubits</td>
<td>Maud Vinet, CEA-Leti, France</td>
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<td>WS3.5</td>
<td>Cryogenic CMOS for Control of Transmon Qubits</td>
<td>Joseph Bardin, Google AI Quantum &amp; University of Massachusetts Amherst, USA</td>
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SELECT June-15 08:00 PDT / June-15 17:00 CET / June-16 00:00 JST OR June-15 17:00 PDT / June-16 02:00 CET / June-16 09:00 JST (2 hours)

**Session Chairs:** Brian Ginsburg (Texas Instruments), Katsura Miyashita (Toshiba)

### PL1 - Plenary 1

**PL1.1 (Plenary) - Silicon is Greener: Why Innovation in Circuits is Needed for Sustainability**
Jennifer Lloyd, Analog Devices, USA

**PL1.2 (Plenary) - 5G Evolution and 6G**
Takehiro Nakamura, NTT Docomo, Japan

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### EA1 Executive Session - Advanced CMOS (1)

**June-15 10:00 PDT / June-15 19:00 CET / June-16 02:00 JST (1 hour)**

**Session Chairs:** Paul Grudowski (NXP Semiconductors)

- **TC1.2 - 7-Level-Stacked Nanosheet GAA Transistors for High Performance Computing**
  Sylvain Barraud, CEA-Leti-MINATEC, France

- **TC1.4 - All-Operation-Regime Characterization and Modeling of Drain Current Variability in Junctionless and Inversion-Mode FDSOI Transistors**
  Daphnie Bosch, CEA-Leti-MINATEC, France

- **TC2.2 - Addressing Key Challenges for SiGe-pFin Technologies: Fin Integrity, Low-β, Si-cap-free Gate Stack and Optimizing the Channel Strain**
  Hiroaki Amurita, imec, Belgium

- **TC2.4 - Vertical heterojunction Gex0.85Sn0.15/Ge GAA Nanowire pMOSFETs: Low SS of 67mV/dec, Small DIBL of 244mV/V and Highest G_m,ext of 870μS/μm**
  Mingshan Liu, Forschungszentrum JuEilich, Germany

- **TC2.5 - Structural and Electrical Demonstration of SiGe Cladded Channel for PMOS Stacked Nanosheet Gate-All-Around Devices**
  Shogo Mochizuki, IBM Research, USA

- **TC3.1 - Materials Technology Co-Optimization of Self-Aligned Gate Contact for Advanced CMOS Technology Nodes**
  Ashish Pal, Applied Materials, USA

- **TC3.2 - Selective Enablement of Dual Dipoles for Near Bandedge Multi-V, Solution in High Performance FinFET and Nanosheet Technologies**
  Ruqiang Bao, IBM Research, USA

- **TC3.3 - Composite Interconnects for High-Performance Computing Beyond the 7nm Node**
  Suketu Parikh, Applied Materials, USA

- **THL.5 - Improved Air spacer Co-Integrated with Self-Aligned Contact (SAC) and Contact Over Active Gate (COAG) for Highly Scaled CMOS Technology**
  Kangguo Cheng, IBM, USA

- **THL.6 - Buried Power Rail Integration with Si FinFETs for CMOS Scaling Beyond the 5nm Node**
  Anshul Gupta, imec, Belgium

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### EA2 Executive Session - Sensor Systems

**June-15 10:00 PDT / June-15 19:00 CET / June-16 02:00 JST (1 hour)**

**Session Chairs:** Neale Dutton (STMicroelectronics)

- **CA2.1 - A 170μW Image Signal Processor Enabling Hierarchical Image Recognition for Intelligence at the Edge**
  Hyochan An, University of Michigan, USA

- **CA2.2 - A 0.055μJ/Pixel 70fps FHD 1Meps Event-Driven Visual Data Processing Unit**
  Somnath Paul, Intel, USA

- **CA2.3 - A 65nm Image Processing SoC Supporting Multiple DNN Models and Real-Time Computation-Communication trade-off via Actor-Critical Neuro-Controller**
  Ningyuan Cao, Georgia Institute of Technology, USA

- **CA2.4 - A Ray-Casting Accelerator in 10nm CMOS for Efficient 3D Scene Recreation in Edge Robotics and Augmented Reality Applications**
  Steven Hsu, Intel, USA

- **CA3.2 - 17.3GCUPS Pruning-Based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing**
  Xiaowu Wu, University of Michigan, SequaL, USA

- **CB1.2 - An Artificial Iris ASIC with High Voltage Liquid Crystal Driver, 10μA Light Range Detector and 40μA Blink Detector for LCD Flicker Removal**
  Bogdan Rudacanu, imec, Belgium

- **CB1.3 - A Packaged Ingestible Bio-Pill with 15-Pixel Multiplexed Fluorescence Nucleic-Acid Sensor and Bi-Drectional Wireless Interface for In-vivo Bio-Molecular Sensing**
  Chengjie Zhu, Princeton University, USA

- **CB2.3 - A 3.5μW@5fps QQVGA Self-Controlled Wake-Up Imager with On-Chip Motion Detection, Auto-Exposure and Object Recognition**
  Amaud Verdant, CEA-Leti-MINATEC, France

- **CB3.2 - A Pressure Sensing System with ±0.75mmHg (3σ) Inaccuracy for Battery-Powered Low Power IoT Applications**
  Seok Hyeon Jeong, University of Michigan, USA

- **CB4.4 - A Portable NMR System with 50kHz IF, 10μs Dead Time, and Frequency Tracking**
  Sungjin Hong, University of Texas at Austin, USA

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### EB1 Executive Session - Memory (1)

**June-15 19:00 PDT / June-16 04:00 CET / June-16 11:00 JST (1 hour)**

**Session Chairs:** Brian Ginsburg (Texas Instruments), Katsura Miyashita (Toshiba)

- **EB1.4 - A Vertical 2T NOR (V2T) Architecture to Enable Scaling and Low-Power Solutions for NOR Flash Technology**
  Chia-Sheng Lin, TSMC, Taiwan

- **EB1.5 - A No-Verification Multi-Level-Cell (MLC) Operation in Cross-PointOTS-PCM**
  Manbo Gong, IBM T. J. Watson Research Center, USA

- **EB1.6 - Si Incorporation Into AsSeGe Chalcogenides for High Thermal Stability, High Endurance and Extremely Low Vth Drift 3D Stackable Cross-Point Memory**
  Huai-Yu Cheng, Macronix International Co., Ltd., Taiwan

- **TM2.2 - A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing**
  Weier Wan, Stanford University, USA

- **TM2.3 - Industrially Applicable Read Disturb Model and Performance on Mega-Bit 28nm Embedded RRAM**
  Chang-Feng Yang, TSMC, Taiwan
**Tuesday June-16**

**PSC1 Technology Short Course E-Pitch & Q/A Panel**

**Future of Scaling for Logic and Memory**

June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)

Session Chairs: Nirmal Ramaswamy (Micron), Kazuhiko Endo (AIST)

Nicolas Loubet, IBM, USA
Mauro Kobrinsky, Intel, USA
Gwan-Hyeob Koh, Samsung Electronics, Republic of Korea
Uwe Schroeder, NaMLab gGmbH, Germany
Anthony Yen, ASML, USA
Chang-Hong Shen, Taiwan Semiconductor Research Institute, Taiwan
Suman Datta, University of Notre Dame, USA
Tatsuo Maeda, National Institute of Advanced Industrial Science and Technology, Japan

**PSC2 Joint Short Course E-Pitch & Q/A Panel**

**Heterogeneous Integration – To Boldly Go Where No Moore Has Gone Before**

June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)

Session Chairs: Vijay Narayanan (IBM), Alvin Loke (TSMC)

Samuel Naftziger, AMD, USA
Eric Beyne, imec, Belgium
Key Chung, SPIL R&D, Taiwan
Arvind Kumar & Muxia Faroøq, IBM Research, USA
Marco Del Sarto, STMicroelectronics, Italy
Kenny C.H. Hsieh, TSMC, Taiwan
Rajesh Gupta, Synopsys, USA
Ki Chul Chun, Samsung Electronics, Republic of Korea

**PSC3 Circuits Short Course E-Pitch & Q/A Panel**

**Trends and Advancements in Circuit Design**

June-16 06:00 PDT / 15:00 CET / 22:00 JST (1 hour)

Session Chairs: Xin Zhang (IBM), Minkyu Je (KAIST)

Wing-Hung Ki, Hong Kong University of Science and Technology, China
Michael Flynn, University of Michigan, USA
Kolf Makinwa, Delft University of Technology, Netherlands
Jae-Yoon Sim, POSTECH, Republic of Korea
Yao-Hong Liu, imec, Netherlands
Mounir Meghelli, IBM, USA
Thomas Burd, AMD, USA
Yih Wang, TSMC, Taiwan

**P4 SSCS/EDS-Sponsored Diversity Panel - Cultivating Engineering Confidence**

June-16 08:00 PDT / June-16 17:00 CET / June-17 00:00 JST (1 hour)

Session Chairs: Nadine Collaert (imec), Carolina Mora Lopez (imec)

Susan Feindt, Analog Devices, USA
Danielle Griffith, Texas Instruments, USA
Makoto Ikeda, University of Tokyo, Japan
Myung-Hee Na, imec, Belgium
### PWS2 Workshop 2 Panel and Q&A - Know Where You Are Going; Metrology In the New Age of Semiconductor Manufacturing

**June-16 19:00 PDT / June-17 04:00 CET / June-17 11:00 JST (1 hour)**

**Session Chairs:** Gosia Jurczak (Lam Research), Takaaki Tsunomura (Tokyo Electron)

**Moderator:** Tom Larson, Nova Measuring Instruments

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<th>Tom Larson, Nova Measuring Instruments</th>
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<td>Keiji Suzuki, Kioxia</td>
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<td>Metrology with Angstrom Accuracy Required by Logic IC Manufacturing – Challenges From R&amp;D to High Volume Manufacturing and Solutions in the AI Era</td>
<td>Yi Hung Lin, TSMC</td>
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<td>Philippe Leray, imec</td>
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<td>Mark Shirley, KLA</td>
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<td>Kavita Shah, Nova Measuring Instruments</td>
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<td>Opportunities and Challenges for Lab-based Characterization for Emerging Technologies</td>
<td>Markus Kuhn, Intel</td>
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### Wednesday, June 17

**PWS3 Workshop 3 Panel and Q&A - Quantum Computers for Electrical Engineers**

**June-17 10:00 PDT / June-17 19:00 CET / June-18 02:00 JST (1 hour)**

**Session Chairs:** Maud Vinet (CEA-Leti)

**Moderator:** Iuliana Radu, imec, Belgium

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<td>Hiroshi Oka, National Institute of Advanced Industrial Science and Technology, Japan</td>
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<td>William Oliver, Massachusetts Institute of Technology</td>
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<td>Doug McClure, IBM, USA</td>
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<td>Si Based Qubits: Technology and Material Impact on Performance</td>
<td>Iuliana Radu, imec, Belgium</td>
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<td>WS3.4</td>
<td>Architectures Challenges for Si Spin Qubits</td>
<td>Maud Vinet, CEA-Leti, France</td>
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<td>WS3.5</td>
<td>Cryo-CMOS Components for Quantum Tech</td>
<td>Joseph Bardin, Google AI Quantum &amp; University of Massachusetts Amherst, USA</td>
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TF1.1 - FFET Memory Featuring Large Memory Window and Robust Endurance of Long-Pulse Cycling by Interface Engineering Using High-k AON

TF1.2 - Re-Examination of Yc Window and Reliability in HfO2 FFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation

TF1.3 - Hot Electrons as the Dominant Source of Degradation for Sub-5nm HfO2 FeFETs

TF1.4 - A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation

TF1.5 - Asymmetric Polarization Response of Electrons and Holes in Si FeFETs: Demonstration of Absolute Polarization Hysteresis Loop and Inversion Hole Density Over $2 \times 10^{13}$ cm$^{-2}$

TF2.1 - SoC Compatible 1T1C FeRAM Memory Array Based on Ferroelectric Hf$_3$O$_7$Ta$_3$O$_{12}$

TF2.3 - Improved State Stability of HfO2 Ferroelectric Tunnel Junction by Template-Induced Crystallization and Remote Scavenging for Efficient In-Memory Reinforcement Learning

TF2.5 - Fast Thermal Quenching on the Ferroelectric AI: HfO2 Thin Film with Record Polarization Density and Flash Memory Application

TF2.6 - Multi-Probe Characterization of Ferroelectric/Dielectric Interface by C-V, P-V and Conductance Methods

TF2.8 - Atomic-Scale Imaging of Polarization Switching in an (Anti)-Ferroelectric Memory Material: Zirconia (ZrO$_2$)

CD1.3 - An 8b 1GSPs 2.55mW SAR-Flash ADC with Complementary Dynamic Amplifiers

CD1.4 - A 177mW 10GS/s NRZ DAC with Switching-Glitch Compensation Achieving $>$ 64dBc SFDR and $<$ 77dBc IM3

CD2.2 - A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved Second-Order DDS Modulator with Digital Feedforward Extrapolation in 28nm CMOS

CD2.3 - A 10.4mW 50MHz-BW 80dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp

CD2.5 - A SAR ADC with Reduced kTC Noise by Decoupling Noise PSD and BW

CF1.1 - Embedded PLL Phase Noise Measurement Based on a PFD/CP MASH 1-1-1 ΔΣ Time-Delay-Integrated-Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring

CF1.3 - A 4GHz 0.7ps-Integrated-Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring with a Jitter-Tracking DLL-Assisted DTC

CF1.5 - A 3.2-to-3.8GHz Calibration-Free Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving $>$66dBc Worst-Case In-Band Fractional Spur

CW1.3 - A 4-to-18GHz Active Poly Phase Filter Quadrature Clock Generator with Phase Error Correction in 5nm CMOS

Thursday, June 18

EG1 Executive Session - Heterogeneous Integration (2)

EG2 Executive Session - Robust Computing

EG3 Executive Session - AI/ML
**EH2 Executive Session - High Speed Circuits, Systems, and Devices**

Session Chairs: Seung Kang (Qualcomm Technologies), Taung-Yung Jonathan Chang (TSMC)

- **June 18 17:00 PDT / June 19 02:00 CET / June 19 09:00 JST (1 hour)**

**CF2.1** - A 29% PAE 1.5bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked PLL
Yuncheong Zhang, Tokyo Institute of Technology, Japan

**CF2.2** - A 2.8GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation
Jian Pang, Tokyo Institute of Technology, Japan

**CF2.3** - A 293/440 GHz Push-Push Double Feedback Oscillators with 5.0/-3.9dBm Output Power and 2.90/6.6% DC-to-RF Efficiency in 65nm CMOS
Dzuhy Radyiyo Utomo, Korea Advanced Institute of Science and Technology, Republic of Korea

**CF2.4** - A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-GmGn Gain Boosting Technique
Dae-Woong Park, imec, Republic of Korea

**CW2.1** - A 28Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ Calibration for Memory Interfaces
Yong-Un Jeong, Seoul National University, Republic of Korea

**CW2.2** - A 0.1pJ/b 68GHz Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler
Moon-Chul Choi, Seoul National University, Republic of Korea

**JFS2.1** - A Comprehensive Reliability Characterization of 5G SoC Mobile Platform Featuring 7nm EUV Process Technology
Minjung Jin, Samsung Electronics, Republic of Korea

**JFS2.4** - Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture
Chen Sun, National University of Singapore, Singapore

**JFS2.5** - An RF Transceiver with Full Digital Interface Supporting 5G New Radio FRT with 3.84Gbps DL/1.92Gbps UL and Dual-Band GNSS in 14nm FinFET CMOS
Sangwook Han, Samsung Electronics, Republic of Korea

**JFS2.7** - A 1.96Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems
Chen-Chien Kao, National Taiwan University, Taiwan

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**EH3 Executive Session - New Devices and Applications**

Session Chairs: Peide Ye (Purdue University), Masaharu Kobayashi (University of Tokyo)

- **June 18 18:00 PDT / June 19 03:00 CET / June 19 10:00 JST (1 hour)**

**TN1.1** - Hair-Like Nanostructure Based Ion Detector by 16nm FinFET Technology
Chen-Ping Wang, National Tsing Hua University, Taiwan

**TN1.2** - Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry
Chia-Che Chung, National Taiwan University, Taiwan

**TN1.3** - Robust True Random Number Generator Using Stochastic Short-Term Recovery of Charge Trapping FinFETs for Advanced Hardware Security
Jianguo Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China

**TN1.4** - A Bias and Correlation-Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking
Kai Ni, Rochester Institute of Technology, USA

**TN1.5** - 1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy
Xu Bai, NEC, Japan

**TN1.6** - Proposal and Experimental Demonstration of Reservoir Computing Using HfO2/ZrO2/O/Si FeFETs for Neuromorphic Applications
Eishin Nako, University of Tokyo, Japan

**TN1.7** - High On-Current 2D nFET of 390μA/μm at Vgs = 1V using Monolayer CVD MoS2
Ang-Sheng Chou, TSMC, Taiwan

**TN1.8** - Ultrahigh Responsivity and Tunable Photogain BEOL Compatible MoS2 Phototransistor Array for Monolithic 3D Image Sensor with Block-Level Sensing Circuits
Chih-Chao Yang, Taiwan Semiconductor Research Institute, Taiwan

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**EH4 Executive Session - Memory (3)**

Session Chairs: Chih-Chao Yang (National Taiwan University), Ho-Jin Song (POSTECH)

- **June 18 18:00 PDT / June 19 03:00 CET / June 19 10:00 JST (1 hour)**

**CM1.1** - A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 175mV VMIN Reduction with Negligible Power Overhead
Zheng Guo, Intel, USA

**CM1.2** - A 29.2Mb/mm² Ultra High Density SRAM Macro Using 7nm FinFET Technology with Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit
Yoshisato Yokoyama, Renesas Electronics, Japan

**CM1.3** - Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, Dual-Edge Driven Wordline/Bitline and Write/Read-Assist Circuit
Jaydeep Kulkarni, Intel, USA

**CM1.4** - A 7nm FinFET 4.04-Mb/mm² TCAM with Improved Electromigration Reliability Using Far-Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier
Kai Ni, Rochester Institute of Technology, USA

**CM1.5** - A 1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Oscillator Phase under Sub-Harmonic Injection Locking
Chen Sun, National University of Singapore, Singapore

**CM1.6** - A Bias and Correlation-Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking
Kai Ni, Rochester Institute of Technology, USA

**CM1.7** - High On-Current 2D nFET of 390μA/μm at Vgs = 1V using Monolayer CVD MoS2
Ang-Sheng Chou, TSMC, Taiwan

**CM1.8** - Ultrahigh Responsivity and Tunable Photogain BEOL Compatible MoS2 Phototransistor Array for Monolithic 3D Image Sensor with Block-Level Sensing Circuits
Chih-Chao Yang, Taiwan Semiconductor Research Institute, Taiwan

**CM2.1** - A 10nm SRAM Design Using Gate-Modulated Self-Collapse Write Assist Enabling 175mV VMIN Reduction with Negligible Power Overhead
Chen Sun, National University of Singapore, Singapore

**CM2.2** - A 22nm 96Kx144 RRAM Macro with a Self-Tracking Reference and a Low Ripple Charge Pump to Achieve a Configurable Read Window and a Wide Operating Voltage Range
Chung-Cheng Chou, TSMC, Taiwan

**CM2.3** - A 25nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation
Hoyoung Shin, Samsung Electronics, Republic of Korea

**CM2.4** - A 247 and 272GHz Two-Stage Regenerative Amplifiers in 65nm CMOS with 18 and 15dB Gain Based on Double-GmGn Gain Boosting Technique
Dae-Woong Park, imec, Republic of Korea

**CM2.5** - A 293/440 GHz Push-Push Double Feedback Oscillators with 5.0/-3.9dBm Output Power and 2.90/6.6% DC-to-RF Efficiency in 65nm CMOS
Dzuhy Radyiyo Utomo, Korea Advanced Institute of Science and Technology, Republic of Korea

**CM3.1** - A 28nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation
Hoyoung Shin, Samsung Electronics, Republic of Korea

**CM3.2** - A 1.8Gb/spin 16T NAND Flash Memory Multi-Chip Package with F-Chip of Toggle 4.0 Specification for High Performance and High Capacity Storage Systems
Daehoon Na, Samsung Electronics, Republic of Korea

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**EH6 Executive Session - Advanced CMOS (2)**

**June-18 19:00 PDT / June-19 04:00 CET / June-19 11:00 JST (1 hour)**

**Session Chairs:** Benjamin Colombeau (Applied Materials), Munehiro Tada (NEC)

- JFS3.4 - Local Variation-Aware Transistor Design through Comprehensive Analysis of Various Vdd/Temperatures Using Sub-7nm Advanced FinFET Technology
  - Soyoun Kim, Samsung Electronics, Republic of Korea

- TC1.1 - Enabling Multiple-Vt Device Scaling for CMOS Technology Beyond 7nm Node
  - Vincent Chang, TSMC, Taiwan

- TC3.4 - Record Low Contact Resistivity to Ge:B (8.1x10^-10 Ω-cm^2) and GeSn:B (4.1x10^-10 Ω-cm^2) with Optimized [B] and [Sn] by In-situ CVD Doping
  - Fang-Liang Lu, National Taiwan University, Taiwan

- TC3.5 - High Quality N+/P Junction of Ge Substrate Prepared by Initiated CVD Doping Process
  - Jaehwan Kim, KAIST, Republic of Korea

- TC3.6 - Ultra-low ρc Extraction for Recessed and Non-Recessed Contacts: Generalized Transmission Line Model
  - Jishen Zhang, National University of Singapore, Singapore

- THL.1 - 5G and AI Integrated High Performance Mobile SoC Process-Design Co-Development and Production with 7nm EUV FinFET Technology
  - Jie Deng, Qualcomm Technologies, USA

End of Program