VLSI 2020 Virtual Conference Program

On Demand Presentations

Short Courses

SC1 - Future of Scaling for Logic and Memory

SC1.1 - NanoSheet Transistor as a Replacement of FinFET for Future nodes: Device Advantages & Specific Process Elements
Nicolas Loubet, IBM, United States

SC1.2 - On-die Interconnect Challenges and Opportunities for Future Technology Nodes
Mauro Kobrinisky, Intel, United States

SC1.3 - Challenges and Prospects of Memory Scaling
Gwan-Hyeob Koh, Samsung Electronic, United States

SC1.4 - Ferroelectric Hafnium Oxide: From Memory to Emerging Applications
Uwe Schroeder, NaMLab gGmbH, Germany

SC1.5 - EUV Lithography and Its Application to Logic and Memory Devices
Anthony Yen, ASML, United States

SC1.6 - Emerging Technologies for TSV-free Monolithic 3DIC
Chang-Hong Shen, Taiwan Semiconductor Research Institute, Taiwan

SC1.7 - In situ BEOL transistors and oxide electronics
Suman Datta, University of Notre Dame, United States

SC1.8 - Layer transfer technology for heterogeneous material integration
Tatsuro Maeda, National Institute of Advanced Industrial Science and Technology (AIST), Japan

SC2 - System, Technology, and Design Solutions for Heterogeneous Integration

SC2.1 - Chiplet Meets the Real World: Benefits and Limits of Chiplet Designs
Samuel Naffziger, AMD, United States

SC2.2 - Heterogeneous System Partitioning and the 3D Interconnect Technology Landscape
Eric Beyne, imec, Belgium

SC2.3 - Back-End Based Chiplet Integration Solutions & Roadmap
C.Key Chung, SPIL Co. Ltd./Corp. R&D, Taiwan

SC2.4 - Heterogeneous integration for AI Architectures
Arvind Kumar & Mukta Farooq, IBM Research, United States

SC2.5 - Heterogeneous integration of chiplets for sensors
Marco Del Sarto, ST Microelectronics, Italy

SC2.6 - Chiplet-to-Chiplet Communication Circuits for 2.5D/3D Integration Technologies
Kenny Cheng-Hsiang Hsieh, Taiwan Semiconductor manufacturing Company, Taiwan

SC2.7 - Performance-Driven Design Methodology and Tools for 2.5D/3D Multi-Die Integration
Rajesh Gupta, Synopsys, Inc., United States

SC2.8 - Generic Design Strategies and Considerations for 2.5D and 3D Stacked IC Designs
Ki Chul Chun, Samsung Electronics, Republic of Korea

SC3 - Trends and Advancements in Circuit Design

SC3.1 - Topologies and Design Techniques of Switched-Capacitor Converters
Wing-Hung Ki, Hong Kong University of Science and Technology, Hong Kong

SC3.2 - The noise-shaping SAR ADC technique: The best of both worlds
Michael Flynn, University of Michigan, United States

SC3.3 - Next Generation Resistor-Based Sensors
Kofi Makinwa, Delft University of Technology, Netherlands

SC3.4 - Time reference and frequency generation
Jae-Yoon Sim, POSTECH, Republic of Korea

SC3.5 - Low-power and digitally-intensive RF transceiver design for IoT applications
Yao-Hong Liu, IMEC Netherlands, Netherlands

SC3.6 - Advances and trends in high-speed serial links for high-density IO applications
Mounir Meghelli, IBM, United States

SC3.7 - Adaptive Circuit & System Design Techniques
Thomas Burd, Advanced Micro Devices, United States

SC3.8 - Trends and Design Considerations for Emerging Memories and In-Memory Computing
Yih Wang, TSMC, United States

Luncheon Talk

Do You Really Know What Is In Your Computer? Perspectives on Verifiable Supply Chains
Andrew "bunnie" Huang

"Friday" Forum

FF.1 - Opening, Overview & Introduction
Ali Keshavarzi, Stanford University, United States

FF.2 - Intelligent Edge – It’s not just technology, it’s about responsible Society
GOWRI CHINDALORE, NXP Semiconductors, Inc., United States

FF.3 - Heterogeneous Integration Technology Trends at the Edge
Chih Hang Tung, TSMC, Taiwan

FF.4 - Self Powered SOCs for the Intelligent Edge
Benton Calhoun, University of Virginia, United States

FF.5 - CMOS and beyond CMOS Technologies for Edge Intelligence
Myung Hee Na, imec, Belgium

FF.6 - Low Power Wide Area (LPWA) Wireless Networks
Thomas Wattenye, Analog Devices, United States

FF.7 - Smart Vision Sensor
Hayato Wakabayashi, Sony Semiconductor Solutions Corporation, Japan

FF.8 - Efficient Machine Learning at the Edge
David Blaauw, University of Michigan, United States

FF.9 - Security in Edge Devices
Hannes Tschofenig, Arm, United States
### Joint Focus Sessions

**JFS1 - Silicon Photonics**

  - Daisuke Okamoto, PETRA, Japan
  - Chen Sun, Ayar Labs, Inc., United States

- JFS1.2 (Invited) - High-Temperature Operation of Chip-Scale Silicon-Photonic Transceiver
  - Jonathan Proesel, IBM T. J. Watson Research Center, United States

- JFS1.3 - A Monolithically Integrated Silicon Photonics 8×8 Switch in 90nm SOI CMOS
  - Dongjae Shin, Samsung Advanced Institute of Technology, Republic of Korea

- JFS1.4 - III/V-on-built-Si technology for commercially viable photonics-integrated VLSI
  - Minjae Shin, Samsung Advanced Institute of Technology, Republic of Korea

- JFS1.5 - O-band GeSi quantum-confined Stark effect electro-absorption modulator integrated in a 220nm silicon photonics platform
  - Perret Clement, imec, Belgium

**JFS2 - 5G/mm-Wave**

- JFS2.1 (Invited) - Hardware-Software Co-integration for Configurable 5G mmWave Systems
  - Alberto Valdes-Garcia, IBM, United States

- JFS2.2 (Invited) - Beyond 5G & Technologies : A Cross-domain Vision
  - Eric Mercier, University Grenoble Alps, CEA, Leti, France

- JFS2.3 - A Comprehensive Reliability Characterization of 5G SoC Mobile Platform featuring 7nm EUV Process Technology
  - Minjung Jin, Samsung Electronics, Republic of Korea

- JFS2.4 - Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture
  - Chen Sun, National University of Singapore, Singapore

- JFS2.5 - FinFET with Contact over Active-Gate for 5G Ultra-Wideband Applications
  - Ali Razavieh, Globalfoundries, United States

- JFS2.6 - An RF Transceiver with Full Digital Interface Supporting 5G New Radio FR1 with 3.84Gbps DL/1.92Gbps UL and Dual-Band GNSS in 14nm FinFET CMOS
  - Sangwook Han, Samsung Electronics, Republic of Korea

- JFS2.7 - A 1.96 Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems
  - Chen-Chien Kao, National Taiwan University, Taiwan

**JFS3 - STCO/DTCO**

- JFS3.1 (Invited) - Heterogeneous System-Level Package Integration – Trends and Challenges
  - Frank Lee, TSMC, Taiwan

- JFS3.2 (Invited) - Can We Ever Get to a 100 nm Tall Library? Power Rail Design for 1nm Technology Node
  - Victor Moroz, Synopsys, Inc., United States

- JFS3.3 - Buried powered SRAM DTCO and system-level benchmarking in Nodal
  - SHARFE SALAHUDDIN, imec, Belgium

**JFS4 - Devices and Circuits for AI/ML**

- JFS4.1 - SOT-MRAM based Analog in-Memory Computing for DNN Inference
  - Jonas Doeverspeck, KU Leuven, Belgium

- JFS4.2 - Compact Probabilistic Poisson Neuron based on Back-Hopping Oscillation in STT-MRAM for All-Spin Deep Spiking Neural Network
  - Ming-Hung Wu, National Chiao Tung University, Taiwan

- JFS4.3 - An All-Weights-on-chip 22nm ULL Featuring 24×1 Mb eMRAM
  - Zhehong Wang, University of Michigan, United States

- JFS4.4 - PNPU: A 146.52 TOPS/W Deep-Neural-Network Learning Processor with Stochastic Coarse-Fine Pruning and Adaptive Input/Output/Weight Skipping
  - Sangyeob Kim, Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea

- JFS4.5 - A Mixed-signal Time-Domain Generative Adversarial Network Accelerator with Efficient Subthreshold Time Multiplier and Mixed-signal On-chip Training for Low Power Edge Devices
  - Zhengyu Chen, Northwestern University, United States

**JFS5 - Heterogeneous Integration**

- JFS5.1 - Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry: Multi-Tier Complementary Carbon Nanotube Logic and Resistive RAM at a 130 nm node
  - Tathagata Srimani, MIT, United States

- JFS5.2 - A 1.8 Gb/s/16Tb NAND Flash Memory Multi-chip Package with F-chip of Toggle 4.0 Specification for High performance and High capacity Storage Systems
  - Daeho Na, Flash Design Team, Samsung Electronics, Republic of Korea

- JFS5.3 - A Reconfigurable High-Bandwidth CMOS-MEMS Capacitive Accelerometer Array with High-g Measurement Capability and Low Bias Instability
  - Xiaoliang Li, Carnegie Mellon University, United States

- JFS5.4 - 3D-Stacked Cortex-M0 SoC with 20.3Gbps/mm2 7.1mW/mm2 Simultaneous Wireless Inter-Tier Data and Power Transfer
  - Benjamin Fletcher, University of Southampton, United Kingdom

- JFS5.5 - Heterogeneous Power Delivery for 7nm High-Performance Chiplet-Based Processors Using Integrated Passive Device and In-Package Voltage Regulator
  - Alan Roth, Taiwan Semiconductor manufacturing Company, United States

### Circuits

**CA1 - Machine Learning**

- **CA1.1** - A 3.0 TFLOPS 0.62V Scalable Processor Core for High Compute Utilization AI Training and Inference
  - Sae Kyu Lee, IBM T. J. Watson Research Center, United States

- **CA1.2** - A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS
  - Phil Knag, Intel Corporation, United States

  - Chieh-Fang Teng, National Taiwan University, Taiwan

- **CA1.4** - A 4.45 ms Low-latency 3D Point-cloud-based Neural Network Processor for Hand Pose Estimation in Immersive Wearable Devices
  - Dongseok Im, Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea

- **CA1.5** - A 3mm2 Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception using Parallel Gibbs Sampling in 16nm
  - Glenn G. Ko, Harvard University, United States
### CA2 - Visual Processing & AI

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CA2.1 - A 170μW Image Signal Processor Enabling Hierarchical Image Recognition for Intelligence at the Edge</td>
<td>Hyochan An, University of Michigan, USA</td>
</tr>
<tr>
<td>CA2.2 - A 0.05μJ/Pixel 70fps FHD 1Meps Event-Driven Visual Data Processing Unit</td>
<td>Somnath Paul, Intel Corporation, United States</td>
</tr>
<tr>
<td>CA2.3 - A 65nm Image Processing SoC Supporting Multiple DNN Models and Real-Time Computation-Communication Trade-off via Actor-Critical Neuro-Controller</td>
<td>Ningyuan Cao, Georgia Institute of Technology, United States</td>
</tr>
<tr>
<td>CA2.4 - A Ray-Casting Accelerator in 10nm CMOS for Efficient 3D Scene Reconstruction in Edge Robotics and Augmented Reality Applications</td>
<td>Steven Hsu, Intel Corporation, United States</td>
</tr>
<tr>
<td>CA2.5 - A 1200x1200 8-Edges/Vertex FPGA-based Motion-Planning Accelerator for Dual-Arm Robot Manipulation Systems</td>
<td>Takashi Oshima, Hitachi Ltd., Japan</td>
</tr>
</tbody>
</table>

### CA3 - Image Sensor & Imaging Techniques

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CA3.1 (Invited) - Managing Chip Design Complexity in the Post-Moore's Law Era</td>
<td>Yunsup Lee, SiFive, United States</td>
</tr>
<tr>
<td>CA3.2 - 17.3 GCUPS Pruning-based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing</td>
<td>Xiao Wu, University of Michigan, Sequa Inc, United States</td>
</tr>
<tr>
<td>CA3.3 - A Probabilistic Self-annealing Compute Fabric based on 560 Hexagonally Coupled Ring Oscillators for Solving Combinatorial Optimization Problems</td>
<td>Ibrahim Ahmed, University of Minnesota, United States</td>
</tr>
<tr>
<td>CA3.4 - MANA: A Monolithic Adiabatic Integration Architecture Microprocessor Using 1.42J/op Superconductor Josephson Junction Devices</td>
<td>Christopher Ayala, Yokohama National University, Japan</td>
</tr>
<tr>
<td>CA3.5 - 32 GHz 6.5 mW Gate-Level-Pipelined 4-bit Processor using Superconductor Single-Flux Quantum Logic</td>
<td>Koki Ishida, Kyushu University, Japan</td>
</tr>
</tbody>
</table>

### CB1 - Biomedical Sensors

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CB1.1 - A 785mW Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring</td>
<td>Peng Wang, University of Virginia, United States</td>
</tr>
<tr>
<td>CB1.2 - An Artificial Iris ASIC with High Voltage Liquid Crystal Driver, 10 nA Light Range Detector and 40 nA Blink Detector for LCD flicker removal</td>
<td>Bogdan Raducanu, imec, Belgium</td>
</tr>
<tr>
<td>CB1.3 - A Packaged Ingestible Bio-pill with 15-pixel Multiplexed Fluorescence Nucleic-acid Sensor and Bi-directional Wireless Interface for In-vivo Bio-molecular Sensing</td>
<td>Chengjie Zhu, Princeton University, United States</td>
</tr>
<tr>
<td>CB1.4 - 1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-Chip with Dynamic Incremental-SAR Acquisition</td>
<td>Jun Wang, UCSD, United States</td>
</tr>
<tr>
<td>CB1.5 (Invited) - High-Density and Large-Scale MEA System Featuring 236,880 Electrodes at 11.72 μm Pitch for Neuronal Network Analysis</td>
<td>Yuri Kato, Sony Semiconductor Solutions Corporation, Japan</td>
</tr>
</tbody>
</table>

### CB2 - Image Sensor & Imaging Techniques

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CB2.1 (Invited) - A 2D-SPAD Array and Read-Out AFE for Next-Generation Solid-State LiDAR</td>
<td>Tuan Thanh Ta, Toshiba Corp., Japan</td>
</tr>
<tr>
<td>CB2.2 - A 36-channel SPAD-integrated scanning LiDAR sensor with multi-event histogramming TDC and embedded interference filter</td>
<td>Hyeongseok Seo, Sungkyunkwan University, Republic of Korea</td>
</tr>
<tr>
<td>CB2.3 - A 3.0μW/65ps CVGVA self-controlled wake-up imager with on-chip motion detection, auto-exposure and object recognition</td>
<td>Arnaud Verdant, CEA-LETI-MINATEC, France</td>
</tr>
<tr>
<td>CB2.4 - A Low Noise Read-out IC with Gate Driver for Full Front Display Area Optical Fingerprint Sensors</td>
<td>Yongil Kwon, Samsung electronics, Republic of Korea</td>
</tr>
<tr>
<td>CB2.5 - An Always-On 4x Compressive VGA CMOS Image with 51μj/pixel and &gt;32dB PSNR</td>
<td>Wenda Zhao, The University of Texas at Austin, United States</td>
</tr>
</tbody>
</table>

### CB3 - Physical Sensors

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CB3.1 - A 50.7dB-DR Finger-Resistance Extractable Multi-Touch Sensor IC Achieving Finger-Classification Accuracy of 97.7% on 6.7-inch Capacitive Touch Screen Panel</td>
<td>Tae-Gyun Song, KAIST, Republic of Korea</td>
</tr>
<tr>
<td>CB3.2 - A Pressure Sensing System with ±0.75mmHg (3σ) Inaccuracy for Battery-Powered Low Power IoT applications</td>
<td>Seok Hyeon Jeong, University of Michigan, United States</td>
</tr>
<tr>
<td>CB3.3 - A 200μW Eddy Current Displacement Sensor with 6.7nm RMS Resolution</td>
<td>Matheus Pimenta, Cypress Semiconductor, Ireland</td>
</tr>
<tr>
<td>CB3.4 - A 0.72 nW, 1 Sample/s Fully Integrated pH Sensor with 65.8 LSB/pH Sensitivity</td>
<td>Yihan Zhang, Columbia University, United States</td>
</tr>
<tr>
<td>CB3.5 - An 8-Element Frequency-Selective Acoustic Beamformer and Bitstream Feature Extractor with 60 Mel-Frequency Energy Features Enabling 95% Speech Recognition Accuracy</td>
<td>Seungjong Lee, University of Michigan, United States</td>
</tr>
</tbody>
</table>

### CB4 - Front-Ends for Sensor Interfaces

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CB4.1 - A -105dB THD 88dB-SNDR VCO-based Sensor Front-end Enabled by Background-Calibrated Differential Pulse Code Modulation</td>
<td>Jiannan Huang, University of California San Diego, United States</td>
</tr>
<tr>
<td>CB4.2 - A 4.3fJ/conversion-step 6440μm² all-dynamic capacitance-to-digital converter with energy-efficient charge reuse</td>
<td>Haoming Xin, Eindhoven University of Technology, Netherlands</td>
</tr>
<tr>
<td>CB4.3 - A 0.5V, 62μJ, 0.059mm² Sinusoidal Current Generator IC with 0.098% THD for Bio-impedance Sensing</td>
<td>Kwantaee Kim, Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea</td>
</tr>
<tr>
<td>CB4.4 - A Portable NMR System with 50-KHz IF, 10-us Dead Time, and Frequency Tracking</td>
<td>Sungjin Hong, The University of Texas at Austin, United States</td>
</tr>
</tbody>
</table>

### CC1 - Circuits for Security and Safety

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC1.1 - A Performance-Flexible Energy-Optimized Automotive-Grade Cortex-R4F SoC through combined AVS/ABB/Bias-in-Memory-Array Closed-Loop Regulation in 28nm FD-SOI</td>
<td>Ricardo Gomez Gomez, ST Microelectronics, France</td>
</tr>
<tr>
<td>CC1.2 - A SCA-Resistant AES Engine in 14nm CMOS with Time/Frequency-Domain Leakage Suppression using Non-linear Digital LDO Cascaded with Arithmetic Countermeasures</td>
<td>Raghavan Kumar, Intel, United States</td>
</tr>
<tr>
<td>CC1.3 - A 0.26% BER, 10°28 Challenge-Response Machine-Learning Resistant Strong-PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection</td>
<td>Vikram Suresh, Intel Corporation, United States</td>
</tr>
<tr>
<td>CC1.4 - A 435MHz, 2.5Mbps/W Side-Channel-Attack Resilient Crypto-Processor for Secure RSA- Raghavan Kumar, Intel, United States</td>
<td>4K Public-Key Encryption in 14nm CMOS</td>
</tr>
</tbody>
</table>
### CF1 - Advanced PLLs

- **CF1.1** - A 1MS/s to 1GS/s Ring-Based Pipelined ADC with Fully Dynamic Reference Regulation and Stochastic Scope-on-Chip Background Monitoring in 16nm
  - Vijay Kiran Kalyanam, Qualcomm Technologies, Inc., Austin, United States
  - Khoondker Ahmed, Intel Corporation, United States

- **CF1.2** - A 10-bit 100-MS/s SAR ADC with Always-on Reference Ripple Cancellation
  - Longyang Lin, National University of Singapore, Singapore

- **CF1.3** - An 8b 1GS/s 2.55mW SAR-Flash ADC with Complementary Dynamic Amplifiers
  - Dong-Ryeol Oh, KAIST, Republic of Korea

- **CF1.4** - A 177mW 10GS/s NRZ DAC with Switching-Glitch Compensation Achieving > 64dBc SFDR and < -77dBc IM3
  - Hung-Yi Huang, National Cheng Kung University, Taiwan

- **CF1.5** - A Compact 14 GS/s 8-bit Switched-Capacitor DAC in 16 nm FinFET CMOS
  - Pietro Caragiulo, Stanford University, United States

### CF2 - RF & mm-Wave Circuits

- **CF2.1** - A 29% PAE 1.5bit-DSM-Based Polar Transmitter with Spur-Mitigated Injection-Locked
  - Yuncheng Zhang, Tokyo Institute of Technology, Japan

- **CF2.2** - A 5MHz-BW, 86.1dB-SNR 4X Time-Interleaved second-order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS
  - Dongyang Jiang, AMSV and IME/FST-EC, University of Macau, Macao

- **CF2.3** - A 10.4mW 50MHz-BW 800dB-DR Single-Opamp Third-Order CTSDM with SAB-ELD-Merged Integrator and 3-Stage Opamp
  - Kai Xing, State-Key Laboratory of Analog and Mixed Signal VLSI, IME and DECE/FST, University of Macau, China

- **CF2.4** - A 1 GS/s Reconfigurable BW 2nd-Order Noise-Shaping Hybrid Voltage-Time Two-Step ADC Achieving 170.9 dB FoMs
  - Yifan Lyu, MICAS-KU Leuven, Belgium

- **CF2.5** - A SAR ADC with Reduced kT/C Noise by Decoupling Noise PSD and BW
  - Zhe Li, Zhejiang University, University of Texas at Austin, China

### CD1 - High-Speed Data Converters

- **CD1.1** - A 440μW, 109.8dB DR, 105.5dB SNDR Discrete-Time Zoom ADC with a 20kHz BW
  - Efrain Eland, Delft University of Technology, Netherlands

- **CD1.2** - A 5MHz-BW, 86.1dB-SNR 4X Time-Interleaved second-order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS
  - Dongyang Jiang, AMSV and IME/FST-EC, University of Macau, Macao

- **CD1.3** - A 480MHz 0.73psrms-Integrated Jitter PVT-Insensitive Fractional-N Sub-Sampling Ring PLL with a Jitter-Tracking DLL-Assisted DTC
  - Jaejong Hong, Samsung Electronics, Republic of Korea

- **CD1.4** - A 3.3GHz 101fms Jitter, -250.3dB FOM Fractional-N DPLL with Phase Error Detection Accomplished in Fully Differential Voltage Domain
  - Lianbo Wu, ETH, Switzerland

- **CD1.5** - A 3.2-to-3.8GHz Calibration-Free Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving -66dBc Worst-Case In-Band Fractional Spur
  - Masaru Osada, The University of Tokyo, Japan

### CD2 - Data Converter Techniques

- **CD2.1** - Embedded PLL Phase Noise Measurement Based on a PFD/CP MASH 1-1-1 ΔΣ Time-to-Mao-Hsuan Chou, Taiwan Semiconductor manufacturing Company, Taiwan
  - Digital Converter in 7nm CMOS

- **CD2.2** - A Fast Locking 5.8 - 7.2 GHz Fractional-N Synthesizer with Sub-2 us Settling Time in 22 nm FD-SOI
  - Jeffrey Prinzie, KU Leuven, Belgium

- **CD2.3** - A 280/140 GHz Push-Push Double Feedback Oscillators with 5.0/-3.9 dBm Output Power
  - Dzuhri Radityo Utomo, KAIST, Republic of Korea

- **CD2.4** - A 247 and 272 GHz Two-Stage Regenerative Amplifiers in 65 nm CMOS with 18 and 15 dB Gain Based on Double-Gmax Gain Boosting Technique
  - Dae-Woong Park, imec, Korea

- **CD2.5** - A 315-GHz Self-Synchronizing Minimum Shift Keying Receiver in 65-nm CMOS
  - Hung-Yi Huang, National Cheng Kung University, Taiwan

### CF3 - IoT and Wireless Receivers

- **CF3.1** - A 17MOPS-36GOPS Adaptive Versatile IoT Node with 15,000x Peak-to-Idle Power Reduction, 207ns Wake-up Time and 1.3TOPS/W ML Efficiency
  - Ivan MIRO-PANADES, University Grenoble Alpes, CEA, LIST, France

- **CF3.2** - A 87.7pJ/cycle 89mW 64-QAM OFDM Receiver Using a Nonlinearity-aware Dual Phase-Locked Loop and DSM-controlled Frequency-Locked Loops
  - Giorgio Cristiano, ETH Zurich, Switzerland

- **CF3.3** - A 2.5V 560kHz 18.8dB/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop
  - Daniel Truesdell, University of Virginia, United States

- **CF3.4** - A 0.9pJ/cycle 89mW 64-QAM OFDM Receiver Using a Nonlinearity-aware Dual Phase-Locked Loop and DSM-controlled Frequency-Locked Loops
  - Yifan Lyu, MICAS-KU Leuven, Belgium

### CF4 - Low Power Oscillators

- **CF4.1** - A 8.7pJ/cycle, 694mW, One-Point Calibrated RC Oscillator Using a Nonlinearity-aware Dual Phase-Locked Loop and DSM-controlled Frequency-Locked Loops
  - Meng Ding, IMEC Netherlands, Netherlands

- **CF4.2** - A 570kHz 18.8dB/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop
  - Jeffrey Prinzie, KU Leuven, Belgium

- **CF4.3** - A 0.9pJ/cycle 89mW 64-QAM OFDM Receiver Using a Nonlinearity-aware Dual Phase-Locked Loop and DSM-controlled Frequency-Locked Loops
  - Yifan Lyu, MICAS-KU Leuven, Belgium
CM1 - Advanced SRAM Design
CM1.1 - A 10nm SRAM Design using Gate-Modulated Self-Collapse Write Assist Enabling 175mV VMIN Reduction with Negligible Power Overhead
Zheng Guo, Intel Corporation, United States
CM1.2 - A 29.2 Mb/mm2 ultra high density SRAM macro using 7nm FinFET technology with dual-edge driven wordline/bitline and write/read-assist circuit
Yoshisato Yokoyama, Renesas Electronics, Japan
CM1.3 - Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1R1W 6T-bitcell SRAM in 10nm FinFET CMOS
Jaydeep Kulkarni, Intel Corporation, United States
CM1.4 - 2x-Bandwidth Burst 6T-SRAM for Memory Bandwidth Limited Workloads
Charles Augustine, Intel Corporation, United States
CM1.5 - A 7nm Fin-FET 4.04-Mb/mm2 TCAM with Improved Electromigration Reliability using Far-Masko Yabuuchi, Renesas Electronics, Japan
Side Driving Scheme and Self-Adjust Reference Match-Line Amplifier

CM2 - Emerging Memory Design
CM2.1 - A 14.7Mb/mm2 28nm FDSOI STT-MRAM with Current Starved Read Path, 520/Sigma Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference
El Mehdi Boujamaa, Arm, France
CM2.2 - Dual-Port Field-Free SOT-MRAM Achieving 90-MHz Read and 60-MHz Write Operations under 55-nm CMOS Technology and 1.2-V Supply Voltage
Masanori Natsui, Tohoku University, Japan
CM2.3 - A 28nm 1.5Mb Embedded 1T2R RRAM with 14.8 Mb/mm2 Using Sneaking Current Suppression and Compensation Techniques
Jingang Yang, Institute of Microelectronics of the Chinese Academy of Sciences, China
CM2.4 - A 22nm 96KX144 RRAM macro with a self-tracking reference and a low ripple charge pump to achieve a configurable read window and a wide operating voltage range
Chung-Cheng Chou, Taiwan Semiconductor manufacturing Company, Taiwan

CM3 - Energy Efficient Memory Design
CM3.1 - A 28nm 10Mb Embedded Flash Memory for IoT Product with Ultra-Low Power Near-1V Supply Voltage and High Temperature for Grade 1 Operation
Hoyoung Shin, Samsung Electronics, Korea, Republic of
CM3.2 - A 65nm 16kb SRAM with 131.5pW Leakage at 0.9V for Wireless IoT Sensor Nodes
Shourya Gupta, University of Virginia, United States
CM3.3 - 1.03pW/bit Ultra-low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors
Jingcheng Wang, University of Michigan, United States
CM3.4 - Z-PIM: An Energy-Efficient Sparcity-Aware Processing-In-Memory Architecture with Fully-Connected Dynamic Weight Precision
Korean Advanced Institute of Science and Technology (KAIST), Korea, Republic of

CP1 - Amplifiers
CP1.1 - A ~107.8 dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier
Huajun Zhang, Delft University of Technology, Netherlands
CP1.2 - An 80, 1.4W, 0.0024% THD+N Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Mode Achieving Low Standby Quiescent Current of 660µA
Ji-Hun Lee, KAIST, Korea, Republic of
CP1.3 - Sample and Average Common-Mode Feedback in a 101 nW Acoustic Amplifier
Rohit Rothe, University of Michigan, United States
CP1.4 - A 0.0046mm2 6.7µW Three-Stage Amplifier Capable of Driving 0.5-to-1.9nF Capacitive Load with <0.68MHz GBW without Compensation Zero
Hongseok Shin, Korea Advanced Institute of Science and Technology (KAIST), Korea, Republic of

CP2 - Voltage References and Wireless Power
CP2.1 - A Single-Tim Switched Capacitor CMOS Bandgap Reference with a 20% Inaccuracy of ±0.02%, ±0.12% for Battery Monitoring Applications
Jun-Ho Bo, Sogang University, Korea, Republic of
CP2.2 - A 0.25-V, 5.3-pW Voltage Reference with 25-µV/oC Temperature Coefficient, 140-µµV/V Line Sensitivity and 2,200-µµ2 Area in 180nm
Luigi Fassio, University of Calabria, Italy
CP2.3 - A 6.79 MHz Wireless Power Transfer System Enabling Perpendicular Wireless Powering with Efficiency Increase from 0.02% to 48.2% by Adaptive Magnetic Field Adder IC Integrating
Hao Qiu, The University of Tokyo, Japan
CP2.4 - A 120-330V, sub-µA, 4-Channel Driver for Microrobotic Actuators with Wireless-Optical Power Delivery and over 99% Current Efficiency
Jan Rentmeister, Dartmouth College, United States

CP3 - Power Converters
CP3.1 - An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching
Dong Yan, The University of Texas at Dallas, United States
CP3.2 - Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 65nm CMOS
Xun Sun, University of Washington, United States
CP3.3 - An N-Path Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting Achieving 13.9x Power Extraction Improvement
Loai Salem, University of California Santa Barbara, United States
CP3.4 - A 4V-0.55V Input Fully Integrated Switched-Capacitor Converter Enabling Dynamic Voltage Domain Stacking and Achieving 80.1% Average Efficiency
Tim Thielemans, MICAS-KU Leuven, Belgium
CP3.5 - A Dual-Rail Hybrid Analog/Digital LDO with Dynamic Current Steering for Tunable High PSRR & High Efficiency
Xiaosen Liu, Intel Corporation, United States
CP3.6 - A Domino Bootstrapping 12V GaN Driver for Driving an On-chip 650V eGaN Power Switch for 96% High Efficiency
Hisuan-Yu Chen, ECE, National Chiao Tung University, Taiwan

CW1 - Ultra-High-Speed Wireline
CW1.1 - A 4x112 Gb/s ADC-DSP Based Multistandard Receiver in 7nm FinFET
Masum Hossain, University of Alberta, Canada
CW1.2 - A 25-50Gb/s 2.22pJ/b NRZ RX with Dual-Bank and 3-tap Speculative DFE for Microprocessor Application in 7nm FinFET CMOS
Yang You, IBM, United States
CW1.3 - A 4-to-18GHz Active Poly Phase Filter Quadrature Clock Generator with Phase Error Correction in 5nm CMOS
WEICHH CHEN, Taiwan Semiconductor manufacturing Company, Taiwan

CW2 - Wireline Techniques
CW2.1 - A 28-Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ calibration for Memory Interfaces
Yong-Un Jeong, Seoul National University, Korea, Republic of
CW2.2 - A 0.1-µm/32b 28-Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler
Moon-Chul Choi, Seoul National University, Korea, Republic of
CW2.3 - Open-Source Synthesizable Analog Blocks for High-Speed Link Designs: 20-GS/s 5b ENOB Analog-to-Digital Converter and 5-GHz Phase Interpolator
Sung-Jin Kim, Stanford University, United States
CW2.4 - A 28Wm 32Gb/s pin 16-QAM Single-Ended Transceiver for High-Speed Memory Interface
Jieqiong Du, UCLA ECE Dept., United States
Technology

THL - Highlight Session

THL.1 - Improved Air Spacer Co-Integrated with Self-Aligned Contact (SAC) and Contact Over Active Gate (COAG) for Highly Scaled CMOS Technology
Kangguo Cheng, IBM, United States

THL.2 - Buried Power Rail Integration with Si FinFETs for CMOS Scaling beyond the 5 nm Node
Anshul Gupta, imec, Belgium

TC1 - Advanced Si CMOS Devices

TC1.1 - Enabling Multiple-Vt Device Scaling for CMOS Technology beyond 7nm Node
Vincent S. Chang, TSMC, Taiwan

TC1.2 - 7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing
Sylvain BARRAUD, CEA-LETI-MINATEC, France

TC1.3 - Cold CMOS as a Power-Performance-Reliability Booster for Advanced FinFETs
H. L. Chiang, TSMC, Taiwan

TC1.4 - All-operation-regime characterization and modeling of drain current variability in junctionless and inversion-mode FDSOI transistors
Bosch Daphnée, CEA-LETI-MINATEC, France

TC2 - Ge and SiGe Devices

TC2.1 - Surface Ga-boosted Boron-doped Si0.5Ge0.5 using In-situ CVD Epitaxy: Achieving 1.1 x 10^21 cm^-3 Active Doping Concentration and 5.7x 10^-10 Q-cm2 Contact Resistivity
Haiwen Xu, National University of Singapore, Singapore

TC2.2 - First Demonstration of 4-Stacked Ge0.915Sn0.085 Wide Nanosheets by Highly Selective Isotropic Dry Etching with High S/D Doping and Undoped Channels
Yu-Shiang Huang, National Taiwan University, Taiwan

TC2.3 - Record Low Contact Resistivity to Ge:B (8.1x10^-10Ω-cm2) and GeSn:B (4.1x10^-10Ω-cm2) with Optimized [B] and [Sn] by In-situ CVD Doping
JaeWhan Kim, KAIST, Korea, Republic of

TC2.4 - Vertical heterojunction Ge0.92Sn0.08/Ge GAA Nanowire pMOSFETs: low SS of 67 mV/dec, small DIBL of 24 mV/V and highest gm. of 1200 µS/µm
Fang-Liang Lu, National Taiwan University, Taiwan

TC2.5 - Structural and Electrical Demonstration of SiGe Cladded Channel for PMOS Stacked Nanosheet Gate-All-Around Devices
Shogo Mochizuki, IBM Research, United States

TC3 - Advanced Processing

TC3.1 - Materials Technology Co-optimization of Self-Aligned Gate Contact for Advanced CMOS Technology Nodes
Ashish Pal, Applied Materials, United States

TC3.2 - Selective Enablement of Dual Dipoles for Near Bandedge Multi-Vt Solution in High Performance FinFET and Nanosheet Technologies
Ruqiang Bao, IBM Research, United States

TC3.3 - Composite Interconnects for High-Performance Computing Beyond the 7nm Node
Suketu Parikh, Applied Materials, Inc., United States

TC3.4 - Record Low Contact Resistivity to Ge:B (8.1x10^-10Ω-cm2) and GeSn:B (4.1x10^-10Ω-cm2) with Optimized [B] and [Sn] by In-situ CVD Doping
JaeWhan Kim, KAIST, Korea, Republic of

TC3.5 - High Quality N+/P Junction of Ge Substrate Prepared by  initiated CVD Doping Process
Yu-Shiang Huang, National Taiwan University, Taiwan

TC3.6 - Ultralow pc Extraction for Recessed and Non-Recessed Contacts: Generalized Transmission Line Model
Ying Wu, National University of Singapore, Singapore

TF1 - FeFETs

TF1.1 - FeFET Memory Featuring Large Memory Window and Robust Endurance of Long-Pulse Cycling by Interface Engineering Using High-k AION
Chi-Yu Chan, National Tsing Hua University, Taiwan

TF1.2 - Re-examination of Vth Window and Reliability in HfO2 FeFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation
Reika Ichihara, Kioxia Corporation, Japan

TF1.3 - Hot Electrons as the Dominant Source of Degradation for Sub-5nm HfO2 FeFETs
Fang-Liang Lu, National Taiwan University, Taiwan

TF1.4 - A Comprehensive Model for Ferroelectric FET Capturing the Key Behaviors: Scalability, Variation, Stochasticity, and Accumulation
Kai Ni, Rochester Institute of Technology, United States

TF1.5 - Asymmetric Polarization Response of Electrodes and Holes in Si FeFETs: Demonstration of Absolute Polarization Hysteresis Loop and Inversion Hole Density over 2x1013 cm-2
Kasidit Toprasertpong, The University of Tokyo, Japan

TF2 - Ferroelectric Memory and Capacitors

TF2.1 - 5G and AI Integrated High Performance Mobile SoC Process-Design Co-Development and Production with 7nm EUV FinFET Technology
Jie Deng, Qualcomm Technologies Inc., United States

TF2.2 - A Novel Dual Ferroelectric Layer Based MFMIS FeFET with Optimal Stack Tuning Toward Low Power and High-Speed NVM for Neuromorphic Applications
Tarek Ali, Fraunhofer IPMS Center Nanoelectronic Technologies, Germany

TF2.3 - Improved state stability of HfO2 ferroelectric tunnel junction by template-induced crystallization and remote scavenging for efficient in-memory reinforcement learning
Weng-Sheng Chen, Kioxia Corporation, Japan

TF2.4 - Nanosecond Laser Anneal (NLA) for Si-implanted HfO2 Ferroelectric Memories Integrated in Back-End Of Line (BEOL)
Laurent Grenouillet, CEA-LETI-MINATEC, France

TF2.5 - Advanced Processing of Absolute Polarization Hysteresis Loop and Inversion Hole Density over 2x1013 cm-2
Kasidit Toprasertpong, The University of Tokyo, Japan
TH1 - 3D Packaging

TH1.1 - Low Temperature SiOC Bonding and Stacking Technology for 12/16 Hi High Bandwidth Memory (HBM)
C.H. Tsai, Taiwan Semiconductor manufacturing Company, Taiwan

TH1.2 - 3D Heterogeneous Package Integration of Air/Magnetic Core Inductor: 89%-Efficiency Buck Converter with Backside Power Delivery Network
Xiao Sun, imec, Belgium

TH1.3 - Bumpless Build Cube (BBCube): High-Parallelism, High-Heat-Dissipation and Low-Power Stackable Memory Using Wafer-Level 3D Integration Process
NORIO CHUJO, Tokyo Institute of Technology, IIR, The WOW Alliance / Hitachi Ltd. Research & Development Group, Japan

TH1.4 - ExaNoDex: combined integration of chiplets on active interposer with bare dice in a multi-chip-module for heterogeneous and scalable high performance compute nodes
Pierre-Yves MARTINEZ, Univ. Grenoble Alpes, CEA-LIST, 38054 Grenoble, France, France

TH1.5 - Immersion in Memory Compute (ImMC) Technology
C.T. Wang, TSMC, Taiwan

TH1.6 - Low Temperature Cu/SiO2 Hybrid Bonding with Metal Passivation
Demin Liu, National Chiao Tung University, Taiwan

TH2 - Semiconducting Oxides for 3D Integration

TH2.1 - BEOL Compatible Dual-Gate Ultra Thin-Body W-Doped Indium-Oxide Transistor with Ion = 370uA/um, SS = 73mV/dec and Ion/Ioff ratio > 4x109
Wridddhi Chakraborty, University of Notre Dame, United States

TH2.2 - Surrounding Gate Vertical-Channel FET with Gate Length of 40 nm using BEOL Compatible High-Thermal-Tolerance In-Al-Zn Oxide Channel
Hirokazu Fujiwara, Kioxia Corporation, Japan

TH2.3 - Amorphous IGZO TFTs featuring Extremely-Scaled Channel Thickness and 38 nm Channel Length: Achieving Record High Gm,max of 125 µS/um at VDS of 1 V and ION of 350
SUBHRANU SAMANTA, National University of Singapore, Singapore

TH3 - Si Technologies for 3D Integration

TH3.1 - First Monolithic Integration of 3D Complementary FET (CFET) on 300mm Wafers Sujith Subramaninan, imec, Belgium

TH3.2 - 3D sequential low temperature top tier devices using dopant activation with excimer laser anneal and strained silicon as performance boosters. Anne Vandooren, imec, Belgium

TH3.3 - 28nm FDSOI CMOS technology (FEOL and BEOL) thermal stability for 3D Sequential Integration: yield and reliability analysis Camila Cavalcante, CEA-LETI, France

TH3.4 - First demonstration of low temperature (≤500°C) CMOS devices featuring functional RO and SRAM bitcells toward 3D VLSI integration Claire Fenouillet-Beranger, CEA-LETI-MINATEC, France

TH3.5 - Flexible and Transparent BEOL Monolithic 3DIC Technology for Human Skin Adaptable Internet of Things Chips Ming-Hsuan Kao, Taiwan Semiconductor Research Institute, Taiwan

TM1 - Memory - NAND/NOR/PCM

TM1.1 - An Extremely Scaled Hemicylindrical (HC) 3D NAND Device with Large Vt Memory Window (>10V) and Excellent 100k Endurance Pei-Ying Du, Macronix International Co., Ltd., Taiwan

TM1.2 - An approach to embedding traditional non-volatile memories into a deep sub-micron CMOS Chia-Sheng Lin, Taiwan Semiconductor manufacturing Company, Taiwan

TM1.3 - A Vertical 2T NOR (V2T) Architecture to Enable Scaling and Low-Power Solutions for NOR Flash Technology Hang-Ting Lue, Macronix International Co., Ltd., Taiwan

TM1.4 - Understanding of Tunable Selector Performance in Si-Ge As-Se OTS Devices by Extended Percolation Cluster Model Considering Operation Scheme and Material Design Shoichi Kabuyanagi, Kioxia Corp. assigned at imec, Japan

TM1.5 - A no-verification Multi-Level-Cell (MLC) operation in Cross-Point OTS-PCM Nanbo Gong, IBM T. J. Watson Research Center, United States

TM1.6 - Si Incorporation Into AsSeGe Chalcogenides for High Thermal Stability, High Endurance and Extremely Low Vth Drift 3D Stackable Cross-point Memory HUAI-YU CHENG, Macronix International Co., Ltd., Taiwan

TM2 - RRAM

TM2.1 - A SiOx RRAM-based hardware with spike frequency adaptation for power-saving continual learning in convolutional neural networks Irene Munoz-Martin, Politecnico di Milano, Italy

TM2.2 - A Voltage-Mode Sensing Scheme with Differential-Row Weight Mapping For Energy-Efficient RRAM-Based In-Memory Computing Weier Wan, Stanford University, United States

TM2.3 - Industrially Applicable Read Disturb Model and Performance on Mega-Bit Embedded RRAM CHANG-FENG YANG, Taiwan Semiconductor manufacturing Company, Taiwan

TM3.1 - Scalability of Quad Interface p-MTJ for 1X nm STT-MRAM with 10 ns Low Power Write Operation, 10 years Retention and Endurance > 10^11 Sadahiko Miura, Tohoku University, Japan

TM3.2 - Reliability Demonstration of Rework Qualified 22nm STT-MRAM for Embedded Memory Applications Chia-Yu Wang, Taiwan Semiconductor manufacturing Company, Taiwan

TM3.3 - Fast Switching of STT-MRAM to Realize High Speed Applications Tae Young Lee, Globalfoundries, Singapore

TM3.4 - A Reliable TDDB Lifetime Projection Model Verified Using 40Mb STT-MRAM Macro at Sub-ppm Failure Rate To Realize Unlimited Endurance for Cache Applications VINAYAK BHARAT NAIK, Globalfoundries, Singapore

TM3 - STT MRAM

TMFS.1 (Invited) - Recent Progresses in STT-MRAM and SOT-MRAM for Next Generation NORIO CHUJO, Tokyo Institute of Technology, IIR, The WOW Alliance / Hitachi Ltd. Research & Development Group, Japan

TMFS.2 (Invited) - Magnetic random access memories (MRAM) beyond information storage Ricardo SOUSA, Univ. Grenoble Alpes / CEA / CNRS, Spintec, France

TMFS.3 - CMOS Compatible Process Integration of SOT-MRAM with Heavy-Metal Bi-Layer Bottom Electrode and 10ns Field-Free SOT Switching with STT Assist. Noriyuki Sato, Intel Corporation, United States

TMFS.4 - Deterministic and field-free voltage-controlled MRAM for high performance and low power applications Yueh Chang Wu, imec, Belgium
### TN1 - New Devices and Applications

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Speaker(s)</th>
<th>Institution(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TN1.1</td>
<td>Hair-Like Nanostructure Based Ion Detector by 16nm FinFET Technology</td>
<td>Chien-Ping Wang</td>
<td>National Tsing Hua University, Taiwan</td>
</tr>
<tr>
<td>TN1.2</td>
<td>Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry</td>
<td>Chia-Che Chung</td>
<td>National Taiwan University, Taiwan</td>
</tr>
<tr>
<td>TN1.3</td>
<td>Robust True Random Number Generator Using Stochastic Short-term Recovery of Charge Trapping FinFET for Advanced Hardware Security</td>
<td>Jianguo Yang</td>
<td>Institute of Microelectronics of the Chinese Academy of Sciences, China</td>
</tr>
<tr>
<td>TN1.4</td>
<td>A Bias and Correlation-Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking</td>
<td>Kai Ni</td>
<td>Rochester Institute of Technology, United States</td>
</tr>
<tr>
<td>TN1.5</td>
<td>1.5x Energy-Efficient and 1.4x Operation-Speed Via-Switch FPGA with Rapid and Low-Cost ASIC Migration by Via-Switch Copy</td>
<td>Xu BAI</td>
<td>NEC, Japan</td>
</tr>
<tr>
<td>TN1.6</td>
<td>Proposal and Experimental Demonstration of Reservoir Computing using $\text{Hf}_0.5\text{Zr}_0.5\text{O}_2$/Si FeFETs for Neuromorphic Applications</td>
<td>Eishin Nako</td>
<td>The University of Tokyo, Japan</td>
</tr>
<tr>
<td>TN1.7</td>
<td>High On-Current 2D nFET of 390 $\mu$A/$\mu$m at VDS = 1V using Monolayer CVD MoS2 without Intentional Doping</td>
<td>Ang-Sheng Chou</td>
<td>Taiwan Semiconductor manufacturing Company, Taiwan</td>
</tr>
<tr>
<td>TN1.8</td>
<td>Ultrahigh responsivity and tunable photogain BEOL compatible MoS2 phototransistor array for monolithic 3D image sensor with block-level sensing circuits</td>
<td>Chih-Chao Yang</td>
<td>Taiwan Semiconductor Research Institute, Taiwan</td>
</tr>
<tr>
<td>TN1.9</td>
<td>GaN PMIC Opportunities: Characterization of Analog and Digital Building Blocks in a 650V GaN-on-Si Platform</td>
<td>Wan Lin Jiang</td>
<td>University of Toronto, Canada</td>
</tr>
</tbody>
</table>

### TN2 - Quantum Computing

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Speaker(s)</th>
<th>Institution(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TN2.1</td>
<td>Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures down to 100mK for Quantum Computing</td>
<td>Bruna Paz</td>
<td>CEA-LETI-MINATEC, France</td>
</tr>
<tr>
<td>TN2.2</td>
<td>Toward Long-coherence-time Si Spin Qubit: The Origin of Low-Frequency Noise in Cryo-CMOS</td>
<td>Hiroshi Oka</td>
<td>National Institute of Advanced Industrial Science and Technology (AIST), Japan</td>
</tr>
</tbody>
</table>

In addition to the on-demand sessions described above, the VLSI Symposia on Technology and Circuits will also feature an exciting program of live events, as summarized in the next page. This includes 2 plenary sessions, 4 panel discussions, 3 workshops, and 25 executive sessions. The goal of Executive Sessions in the VLSI Symposia is to foster a discussion about the current state and future of the field. They will start with a 2 min summary of relevant papers that have been presented at VLSI 2020 on the topic. This will be followed by a 35 min discussion among the authors and session chairs on key challenges and opportunities. All conference participants are welcome to join these sessions and contribute with their insight and questions.
### LIVE PROGRAM SCHEDULE

<table>
<thead>
<tr>
<th>JOINT SHIFT</th>
<th>PDT</th>
<th>CET</th>
<th>JST</th>
<th>Track 1</th>
<th>Track 2</th>
<th>Track 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Monday 6/15</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (I)</strong></td>
<td>06:00-07:00</td>
<td>15:00-16:00</td>
<td>22:00-23:00</td>
<td>Tech SC E-Pitch &amp; Q/A</td>
<td>Joint SC E-Pitch &amp; Q/A</td>
<td>Circ SC E-Pitch &amp; Q/A</td>
</tr>
<tr>
<td><strong>Joint Plenary (II)</strong></td>
<td>08:00-08:50</td>
<td>17:00-17:50</td>
<td>00:00-00:50 next day</td>
<td>Joint Plenary (I)</td>
<td>WIE Panel</td>
<td>10 min break / hallway mingle</td>
</tr>
<tr>
<td><strong>Joint Plenary (III)</strong></td>
<td>09:00-09:50</td>
<td>18:00-18:50</td>
<td>01:00-01:50 next day</td>
<td>10 min break / hallway mingle</td>
<td>Memory (2)</td>
<td>Analog Building Blocks</td>
</tr>
<tr>
<td><strong>Joint Plenary (IV)</strong></td>
<td>10:00-10:50</td>
<td>19:00-19:50</td>
<td>02:00-02:50 next day</td>
<td>10 min break / hallway mingle</td>
<td>Technology and Circuits for ML Workshop</td>
<td>Adaptive Systems</td>
</tr>
<tr>
<td><strong>Joint Plenary (V)</strong></td>
<td>17:00-17:50</td>
<td>02:00-02:50 next day</td>
<td>Advanced CMOS (1)</td>
<td>Sensor Systems</td>
<td>10 min break / hallway mingle</td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (VI)</strong></td>
<td>18:00-18:50</td>
<td>03:00-03:50 next day</td>
<td>10 min break / hallway mingle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (VII)</strong></td>
<td>19:00-19:50</td>
<td>04:00-04:50 next day</td>
<td>10 min break / hallway mingle</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th>NAE SHIFT</th>
<th>PDT</th>
<th>CET</th>
<th>JST</th>
<th>Track 1</th>
<th>Track 2</th>
<th>Track 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tuesday 6/16</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (I)</strong></td>
<td>06:00-07:00</td>
<td>15:00-16:00</td>
<td>22:00-23:00</td>
<td>Tech SC E-Pitch &amp; Q/A</td>
<td>Joint SC E-Pitch &amp; Q/A</td>
<td>Circ SC E-Pitch &amp; Q/A</td>
</tr>
<tr>
<td><strong>Joint Plenary (II)</strong></td>
<td>08:00-08:50</td>
<td>17:00-17:50</td>
<td>00:00-00:50 next day</td>
<td>Joint Plenary (I)</td>
<td>WIE Panel</td>
<td>10 min break / hallway mingle</td>
</tr>
<tr>
<td><strong>Joint Plenary (III)</strong></td>
<td>09:00-09:50</td>
<td>18:00-18:50</td>
<td>01:00-01:50 next day</td>
<td>10 min break / hallway mingle</td>
<td>Memory (2)</td>
<td>Analog Building Blocks</td>
</tr>
<tr>
<td><strong>Joint Plenary (IV)</strong></td>
<td>10:00-10:50</td>
<td>19:00-19:50</td>
<td>02:00-02:50 next day</td>
<td>10 min break / hallway mingle</td>
<td>Technology and Circuits for ML Workshop</td>
<td>Adaptive Systems</td>
</tr>
<tr>
<td><strong>Joint Plenary (V)</strong></td>
<td>17:00-17:50</td>
<td>02:00-02:50 next day</td>
<td>Advanced CMOS (1)</td>
<td>Sensor Systems</td>
<td>10 min break / hallway mingle</td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (VI)</strong></td>
<td>18:00-18:50</td>
<td>03:00-03:50 next day</td>
<td>10 min break / hallway mingle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (VII)</strong></td>
<td>19:00-19:50</td>
<td>04:00-04:50 next day</td>
<td>10 min break / hallway mingle</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th>JFE SHIFT</th>
<th>PDT</th>
<th>CET</th>
<th>JST</th>
<th>Track 1</th>
<th>Track 2</th>
<th>Track 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Wednesday 6/17</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (I)</strong></td>
<td>06:00-07:00</td>
<td>15:00-16:00</td>
<td>22:00-23:00</td>
<td>Tech SC E-Pitch &amp; Q/A</td>
<td>Joint SC E-Pitch &amp; Q/A</td>
<td>Circ SC E-Pitch &amp; Q/A</td>
</tr>
<tr>
<td><strong>Joint Plenary (II)</strong></td>
<td>08:00-08:50</td>
<td>17:00-17:50</td>
<td>00:00-00:50 next day</td>
<td>Joint Plenary (I)</td>
<td>WIE Panel</td>
<td>10 min break / hallway mingle</td>
</tr>
<tr>
<td><strong>Joint Plenary (III)</strong></td>
<td>09:00-09:50</td>
<td>18:00-18:50</td>
<td>01:00-01:50 next day</td>
<td>10 min break / hallway mingle</td>
<td>Memory (2)</td>
<td>Analog Building Blocks</td>
</tr>
<tr>
<td><strong>Joint Plenary (IV)</strong></td>
<td>10:00-10:50</td>
<td>19:00-19:50</td>
<td>02:00-02:50 next day</td>
<td>10 min break / hallway mingle</td>
<td>Technology and Circuits for ML Workshop</td>
<td>Adaptive Systems</td>
</tr>
<tr>
<td><strong>Joint Plenary (V)</strong></td>
<td>17:00-17:50</td>
<td>02:00-02:50 next day</td>
<td>Advanced CMOS (1)</td>
<td>Sensor Systems</td>
<td>10 min break / hallway mingle</td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (VI)</strong></td>
<td>18:00-18:50</td>
<td>03:00-03:50 next day</td>
<td>10 min break / hallway mingle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (VII)</strong></td>
<td>19:00-19:50</td>
<td>04:00-04:50 next day</td>
<td>10 min break / hallway mingle</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th><strong>Thursday 6/18</strong></th>
<th>Track 1</th>
<th>Track 2</th>
<th>Track 1</th>
<th>Track 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Joint Plenary (I)</strong></td>
<td>06:00-07:00</td>
<td>15:00-16:00</td>
<td>22:00-23:00</td>
<td>Tech SC E-Pitch &amp; Q/A</td>
</tr>
<tr>
<td><strong>Joint Plenary (II)</strong></td>
<td>08:00-08:50</td>
<td>17:00-17:50</td>
<td>00:00-00:50 next day</td>
<td>Joint SC E-Pitch &amp; Q/A</td>
</tr>
<tr>
<td><strong>Joint Plenary (III)</strong></td>
<td>09:00-09:50</td>
<td>18:00-18:50</td>
<td>01:00-01:50 next day</td>
<td>Circ SC E-Pitch &amp; Q/A</td>
</tr>
<tr>
<td><strong>Joint Plenary (IV)</strong></td>
<td>10:00-10:50</td>
<td>19:00-19:50</td>
<td>02:00-02:50 next day</td>
<td>10 min break / hallway mingle</td>
</tr>
<tr>
<td><strong>Joint Plenary (V)</strong></td>
<td>17:00-17:50</td>
<td>02:00-02:50 next day</td>
<td>Advanced CMOS (1)</td>
<td>Sensor Systems</td>
</tr>
<tr>
<td><strong>Joint Plenary (VI)</strong></td>
<td>18:00-18:50</td>
<td>03:00-03:50 next day</td>
<td>10 min break / hallway mingle</td>
<td></td>
</tr>
<tr>
<td><strong>Joint Plenary (VII)</strong></td>
<td>19:00-19:50</td>
<td>04:00-04:50 next day</td>
<td>10 min break / hallway mingle</td>
<td></td>
</tr>
</tbody>
</table>

---

**PDT** Pacific Daylight Time (e.g., Los Angeles)  
**CET** Central European Time (e.g., Netherlands)  
**JST** Japan Standard Time (e.g., Japan, South Korea)