The 2023 Symposium on VLSI Technology & Circuits, Evolving VLSI for a Better World with the Theme: "Rebooting Technology and Circuits for a Sustainable Future"

Tokyo, Japan (APRIL 25, 2023) – For the 43rd consecutive year delivering a unique convergence of microelectronics technology and circuits in one venue, Symposium on VLSI Technology & Circuits will resume as an in-person event in Kyoto, Japan on June 11–16, 2023. The six-day event will take place at the Rihga Royal Hotel Kyoto to showcase the theme of "Rebooting Technology and Circuits for a Sustainable Future". The Symposium will feature advanced VLSI technology developments, innovative circuit designs, and the applications they enable, such as artificial intelligence, machine learning, IoT, wearable/implantable biomedical devices, big data, cloud/edge computing, and augmented/virtual reality (AR/VR).

The weeklong Symposium is the premier global venue that promotes synergies between technologists and designers on today's applications and future breakthroughs. In addition to the technical presentations, the Symposium program will feature a demonstration session, joint focus sessions, evening panels, short courses, workshops, and a special forum.

Plenary Sessions:

• "Multi-Chiplet Heterogeneous Integration Packaging for Semiconductor System Scaling" by Suraya Bhattacharya, Director, System-in-Package, A*STAR, IME

Over the past decade, diverse system requirements from a broad range of markets have driven the industry to embrace advanced packaging to heterogeneously integrate multiple chiplets as a key new toolbox for System-in-Package scaling. Dr. Bhattacharya will provide an overview of multi-chiplet heterogeneous integration packaging platforms to address system scaling needs in the coming decades.

• "Searching for Nonlinearity: Scaling Limits in NAND Flash" by Siva Sivaram, President, Western Digital

In this talk, Dr. Sivaram will show that achieving higher bit growth in NAND Flash memory through incessant 3D-stacking of more layers results in sub-linear cost reduction. Wafer bonding technology can disruptively decouple the memory array from complex logic circuits, allowing new integration of high-speed logic with the memory layers, and shortening manufacturing cycle times. This technology frees the industry from one-size-fits-all NAND dies to customized solutions for various applications and system-level savings.

• "Quantum Computing from Hype to Game Changer" by Hiroyuki Mizuno, Distinguished Researcher, Hitachi, Ltd.
Quantum computing is increasingly considered hype as its benefit to the consumer remains unrealized despite widespread investment and investigation. CMOS annealing technology attempts to provide a stop gap solution. This talk introduces the top-down approach that takes full advantage of existing semiconductor technologies and notable developments including the "shuttling qubit" to reach the next milestone to develop silicon quantum computers – qubit operation in a scalable qubit array structure.

• "A Six-Word Story on the Future of VLSI: AI-Driven, Software-Defined, and Uncomfortably Exciting" by Partha Ranganathan, Vice President, Technical Fellow, Google
The AI revolution, cloud, and smart edge are all accelerating the demand for computing, yet Moore's Law is slowing down. This is constantly challenging traditional assumptions around cheaper and more energy-efficient systems and resulting in a significant and growing supply-demand gap for future computing systems. In this talk, Dr. Ranganathan discusses how to rethink and design future hardware and presents two broad themes – efficient hardware design through custom silicon accelerators and efficient hardware utilization through software-defined systems design.

Focus Sessions:

Two technology focus sessions will be held: "BEOL/backside power distribution network (BSPDN)" and "future memory directions". In addition, there will be four joint focus sessions covering both circuits and technology novelty and interest: "new computing", "AR/VR/MR Metaverse", "automotive and aerospace," and "3D system integration".

Short Courses on Key VLSI Topics:

Two full-day short courses will be featured:

- Short Course 1: "*Advanced CMOS Technologies for 1 nm & Beyond*" focuses on novel logic technologies with coverage of FEOL/BEOL processes including EUV lithography, device evolution from Si to novel 2D materials, 3D integration from backside PDN and heterogeneous integration, and future metrology for production.

- Short Course 2: "*Future Directions in High-Speed Wireline and Optical IO*" delves into the latest advancements in SerDes circuit system design, coherent ASICs, and silicon photonics. State-of-the-art chiplet technology, innovative packaging, high-speed receivers and transmitters, and memory interfaces are also covered.

Forum Session:

The Symposium program also features a full-day Forum Session on "Compute Paradigms for Secured Microelectronics and Combinatorial Optimization".

- This Forum is devoted to topics that extend the scope of the Symposia by suggesting the future direction of the VLSI Symposium and emerging cutting-edge VLSI applications. This year, expert speakers from all over the world will focus on secure microelectronics and combinatorial optimization, covering hardware security, cryptographic circuit technology, cyber security as well as combinatorial optimization accelerators based on processor, FPGA, and superconducting quantum annealer.

Evening Panel Discussions:

- *"What is Scalable and Sustainable in the Next 25 Years?"*
  Technology node scaling has been successful for many decades with the evolution in lithography, materials, and device structure. What about the next 25 years? How can we overcome the limits of scaling imposed by physics, manufacturability, economics, energy consumed during chip manufacturing and operation, greenhouse gas emissions in manufacturing, and engineering resources? Can our industry remain attractive

and grow further? Dr. Tomonari Yamamoto from TEL will moderate a panel of distinguished guests from across industry and R&D organizations to offer valuable insights.

- *"Can Universities Help to Revitalize the IC Design Industry? If So, How?"*
  Chips are becoming commodities, forcing the semiconductor industry to reinvent itself. In this climate, can universities contribute to revitalizing chip companies? Are mutually beneficial relationships possible? Or will university researchers continue to focus only what they want to do while companies continue regard universities only as a source of educated talent? Prof. Asad Abidi from the University of California, Los Angeles will moderate a panel of distinguished industry and academia guests to tackle this important topic.

Demo Session:
For the first time this year, the demonstration session will be a fully in-person experience, providing participants an opportunity for in-depth interaction with authors of selected papers from both Technology and Circuits sessions. These demonstrations will show device characterization, chip operation, and potential applications for circuit-level innovations.

Workshops:
A series of workshop sessions will kick off the Symposium program to provide additional learning opportunities. This year, we are pleased to announce six exciting workshops:

Technology Workshops
• EUV Lithography & Path to High-NA EUV Patterning Solutions
• Towards Functional Backside: What's Next after Backside Power Delivery?
• The Deployment of Materials to System Co-Optimization Methodology (MSCO™) to Enable Rapid PPACt Assessment for Advanced Node Technology Development

Circuit Workshops
• Open Source PDKs and EDAs, Community Experiences toward Democratization of Chip Design
• Uniform and Rigorous Benchmarking of Machine Learning ICs and Systems
• 3D Image Sensor

Special Events at the Symposium include mentoring events sponsored by the Women in Engineering and Young Professionals groups of the IEEE Solid-State Circuits Society.

Best Student Paper Awards will be chosen based on paper and presentation quality. The recipients will receive a monetary award, travel cost support, and a certificate.

Further information about the Symposium is available at: http://www.vlsisymposium.org.

Sponsoring Organizations:
The VLSI Symposium on Technology & Circuits is sponsored by Japan Society of Applied Physics, the IEEE Electron Devices Society, the IEEE Solid State Circuits Society, and in corporation with the Institute of Electronics, Information and Communication Engineers.

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