2014 VLSI SYMPOSIA HIGHLIGHTS

The 2014 VLSI Symposia technical program consists of overlapping sessions from June 9 – 12 (Technology) and June 10 – 13 (Circuits), with more than 200 presentations, short courses and panel discussions by the leading researchers and scientists. Program is designed to highlight recent advances in microelectronics technology and circuits, and promote networking amongst participants.

SYMPOSIUM ON VLSI TECHNOLOGY

PLENARY PRESENTATIONS
Tuesday morning, June 10
- Device & Technology Implications of the Internet of Things – Robert Attkin, ARM
- Customer Value Creation in the Information Explosion Era – Keiichiro Shimada, Sony Corporation

RUMP SESSION (panel discussion)
Tuesday evening, June 10
450mm, EUV, III-V, 3D – All in 7nm? Are You Serious?!
Moderator: Andrzej Strojwas, PDF Solutions
Expert panelists from Applied Materials, ASML, IBM, imec, Lam Research, Soitec

TECHNOLOGY FOCUS SESSIONS
Embedded NV Memory Technologies
Session TS (Tuesday, June 10, 3:25pm)
Interconnect: Local & Global
Session T16 (Wednesday, June 11, 8:05am)

JOINT PROGRAM HIGHLIGHTS

JOINT FOCUS SESSIONS
- 3D Circuits & Applications
- 3D Systems & Packaging
- Design Technology Co-Optimization II
- Non-volatile & Emerging Memory
- SRAM & DRAM

JOINT RUMP SESSION (panel discussion)
Tuesday evening, June 10
Who Gives Up on Scaling First: Device & Process Technology Engineers, Circuit Designers or Company Executives? Which Scaling Ends First – Memory or Logic?!
Moderators: Elad Alon, UC Berkeley / Yee Chia Yeo, NUS
Expert panelists from Intel, NVIDIA, Qualcomm, Renesas, Sandisk, SK Hynix, TSMC, UC Berkeley

LUNCHEON & EXECUTIVE PANEL DISCUSSION
Thursday, June 12
Emerging Semiconductor Industry Trends & Implications
Moderator: Jan Rabaey, UC Berkeley
Expert panelists from Intel, NVIDIA, Qualcomm, Renesas, Sandisk, SK Hynix, TSMC, UC Berkeley

SYMPOSIUM ON VLSI CIRCUITS

PLENARY PRESENTATIONS
Wednesday morning, June 11
- Data Center 2020: Near-memory Acceleration for Data-Oriented Applications – Ed Dolter, Micron Technology
- Technology Development for Printed LSIs Based on Organic Semiconductors – Jun Takeya, University of Tokyo

RUMP SESSIONS (panel discussion)
Thursday evening, June 12
What Should Circuit Designers do in an Era of System Level Design? – Moderator: Jan Rabaey, UC Berkeley
Expert panelists from AMD, MediaTek, Qualcomm, Samsung, UC Berkeley, Waseda University, Xilinx

PROFESSIONAL DEVELOPMENT OPPORTUNITIES (CIRCUITS)

SHORT COURSE
Advanced Data Converter & Mixed-Signal Circuit Design
Tuesday, June 10
- A/D Converter Trends: Power Efficiency & Digitally Assisted Architectures
- System Design for Direct Sampling RF Front Ends
- Advances in SAR ADCs with the Scaling of CMOS
- Ultra-wideband Time-interleaved SAR ADCs for Wireline/Optical Communications
- Digitally Assisted Wireless Transceivers & Synthesizers
- Digital Error Correction of Time-interleaved A/D Converters

JOINT PROGRAM HIGHLIGHTS

JOINT FOCUS SESSIONS
- Overview & Advances in Energy Efficient Digital Design
- Overview & Advances in Energy Efficient Digital Design
- Low Power CPUs for SoC Integration
- Energy-Efficient System Architectures
- Fine-Grained Power Management Using Integrated DC-DC Converters
- Challenges & Techniques for Ultra-Low Voltage Logic with Nearly-Minimal Energy
- Advanced Energy Efficient SRAM Design

SATELLITE WORKSHOPS

IEEE Silicon Nanoelectronics Workshop
- June 8 & 9
Spintronics Workshop
- June 9

For complete conference and registration information, visit: http://www.vlsisymposium.org/