

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I	Time	Suzaku I, II, III
7:30-18:00	Registration (Technology and Circuits)							
8:30-12:20		Short Course 3 Opportunities and Challenges at the Intersection of Security and AI 8:30 Introduction to Artificial Intelligence & Security, R. Aitken, ARM Ltd. 9:20 Mobile Deep Learning Processors: Turning Challenges into Opportunities, H.-J. Yoo, KAIST 10:10 Break 10:40 AI Computing Architectures and Hardware, J. Burns, IBM 11:30 Nonvolatile Circuit for AI Edge Applications, M.-F. Chang, National Tsing-Hua Univ. 12:20 Lunch	Short Course 2 Advanced 5G Circuits, Systems and Applications 8:30 5G Real and Future, T. Nakamura, NTT Docomo 9:20 mmWave RFIC Technologies for 5G Infrastructure Applications, S.-G. Yang, Samsung 10:10 Break 10:40 The Hitchhiker's Guide to Saving Moore's Law in the 5G Era, H.-J. Lee, Intel Corp. 11:30 Design Challenges and Solutions of LO Generation for 5G Mobile Systems, J.-H. Choi, UNIST 12:20 Lunch	Short Course 1 CMOS Technology Enablers for Pushing the Limits of Semiconductors: Materials to Packaging 8:30 Breaking the Limitations of FinFET Scaling, M. Liu, Intel Corp. 9:20 Emerging Interconnect Technologies for Nanoelectronics, K. Saraswat, Stanford Univ. 10:10 Break 10:40 Advanced Process Technologies Required for Future Scaling and Devices, R. Clark, TEL 11:30 DTCO in 2019: The Precious Metal Stack and the Route to Better Designs, B. Cline, ARM Ltd. 12:20 Lunch			8:30-17:40 2019 Silicon Nanoelectronics Workshop (Day 2)	Enabling Technologies for Autonomous Driving (Friday Forum) 9:00 Opening 9:10 Inertial and Depth Sensors for Autonomous Vehicles, R. Kapusta, Analog Devices, Inc. 9:55 Safety and Security: Changing the Outlook of the Autonomous Car, K. Khouri, NXP Semiconductors 10:40 Break 11:00 Electronics Technologies Evolve Automobiles!?, N. Kawahara, DENSO Corp. 11:45 Automotive Image Sensor for Autonomous Vehicle and Adaptive Driver Assistance System, H. Matsumoto, Sony Corp.
	12:20-13:10		13:10 RRAM Fabric for In-memory Computing and Neuromorphic Computing Applications, W. Lu, Univ. of Michigan 14:00 Circuit Design Resistant to Side Channel Attacks, N. Homma, Tohoku Univ., 14:50 Break 15:10 Energy-efficient Circuits for Cryptography and Entropy Generation, S. Mathew, Intel Corp. 16:00 Introduction to Electromagnetic Information Security, Y. Hayashi, Nara Institute of Science and Technology	13:10 Acoustic Filter for 5G Smartphones, H. Nakamura, Skyworks 14:00 Substrate Material and Packaging Technology for 5G Millimeter Wave Communication, K. Sudo, Murata 14:50 Break 15:10 Beamforming Circuits, Systems, and Operations for 5G MIMO Systems, H. Wang, Georgia Institute of Tech. 16:00 Built-In Test and Calibration of Phased Arrays, B. Floyd, NCSU	13:10 3D Integration for More Moore and More than Moore, C.-H. Tung, TSMC 14:00 Recent STT-MRAM Technology: From Lab to Fab, Y. Song, Samsung 14:50 Break 15:10 Emerging Logic Devices for Future Computing, S. Salahuddin, Univ. of California, Berkeley 16:00 Overview in Three-dimensionally Arrayed Flash Memory Technology, R. Katsumata, Toshiba Memory Corp.			
13:10-16:50	Demo Setup							
16:50-17:10	Demo Setup							
17:30-21:30	17:30-19:30 Demo Session & Reception							
				20:00-21:30 Joint Evening Panel Discussion				
			The Semiconductor Industry at a Tipping Point: What's Next?					

Friday Evening Event: 16:15-19:35 [Taizo-in]

2019 Symposia on VLSI Technology and Circuits June 11th (Tuesday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:00-17:00	Registration (Technology and Circuits)					
8:00-10:00				T1/C1: Joint Opening and Plenary Session 1		
				8:00-8:40		
				Joint Welcome and Opening Remarks		
				C1-1 8:40-9:20 (Plenary) The Univ. of Tokyo Virtual Cyborg: Beyond Human Limits		
				T1-1 9:20-10:00 (Plenary) DARPA Managing Moore's Inflection: DARPA's Electronics Resurgence Initiative		
10:30-12:35	C2: Advanced Wireless		C3: High Performance Computing		T2: Highlight	
	C2-1 10:30-10:55 Asahi Kasei Microdevices A 76- to 81-GHz, 0.6° degree rms Phase Error Multi-channel Transmitter with a Novel Phase Detector and Compensation Technique	C3-1 10:30-10:55 TSMC A 7nm 4GHz Arm®-Core-based CoWoS® Chiplet Design for High Performance Computing	T2-1 10:30-10:55 Samsung Electronics Enhanced Reliability of 7nm Process Technology Featuring EUV			
	C2-2 10:55-11:20 The Univ. of Texas at Dallas 426-GHz Imaging Pixel Integrating a Transmitter and a Coherent Receiver with an Area of 380x470 μm ² in 65-nm CMOS	C3-2 10:55-11:20 Univ. of Michigan A 1.4 GHz 695 Giga RISC-V Inst/s 496-core Manycore Processor with Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS	T2-2 10:55-11:20 IBM Research Technology Challenges and Enablers to Extend Cu Metallization to Beyond 7 nm Node			
	C2-3 11:20-11:45 Univ. of Southern California A 1-5GHz Direct-Digital RF Modulator with an Embedded Time-Approximation Filter Achieving -43dB EVM at 1024 QAM	C3-3 11:20-11:45 Intel A 250mV, 0.063J/GHash Bitcoin Mining Engine in 14nm CMOS Featuring Dual-Vcc SHA256 Datapath and 3-Phase Latch Based Clocking	T2-3 11:20-11:45 TSMC 3D Multi-Chip Integration with System on Integrated Chips (SoIC™)			
	C2-4 11:45-12:10 Princeton Univ. A 26-42 GHz Broadband, Back-off efficient and VSWR Tolerant CMOS Power Amplifier Architecture for 5G Applications	C3-4 11:45-12:10 ARM Research Labs A 16nm 25mm ² SoC with a 54.5x Flexibility-Efficiency Range from Dual-Core Arm Cortex-A53, to eFPGA, and Cache-Coherent Accelerators	T2-4 11:45-12:10 Toshiba In-Memory Reinforcement Learning with Moderately-Stochastic Conductance Switching of Ferroelectric Tunnel Junctions			
	C2-5 12:10-12:35 Yonsei Univ. A Time Domain Artificial Intelligence Radar for Hand Gesture Recognition Using 33-GHz Direct Sampling		T2-5 12:10-12:35 MIT Monolithic Three-Dimensional Imaging System: Carbon Nanotube Computing Circuitry Integrated Directly Over Silicon Imager			
12:35-14:00						
14:00-15:40	C4: Advanced Frequency Generators		C5: Energy Efficient Computing		T3: Focus Session - Quantum & Neuromorphic Computing	
	C4-1 14:00-14:25 Tokyo Institute of Technology 0.2mW 70fs _{rms} -Jitter Injection-Locked PLL Using Desensitized SSPD-Based Injecting-Time Self-Alignment Achieving -270dB FoM and -66dBc Reference Spur	C5-1 14:00-14:25 Semiconductor Energy Laboratory A 48 MHz 880-nW Standby Power Normally-Off MCU with 1 Clock Full Backup and 4.69-μs Wakeup Featuring 60-nm Crystalline In-Ga-Zn Oxide BEOL-FETs	C6-1 14:00-14:25 imec A 196μW Reconfigurable Light-to-Digital Converter with 119dB Dynamic Range for Wearable PPG/NIRS Sensors	T3-1 14:00-14:25 (Invited) NEC Superconductive Parametric Devices	T4-1 14:00-14:25 Univ. of Notre Dame Energy-Efficient Edge Inference on Multi-Channel Streaming Data in 28nm HKMG FeFET Technology	
	C4-2 14:25-14:50 The Hong Kong Univ. of Science and Technology A 270-GHz Fully-Integrated Frequency Synthesizer in 65nm CMOS	C5-2 14:25-14:50 Intel A Microwatt-Class Always-On Sensor Fusion Engine Featuring Ultra-Low-Power AOI Clocked Circuits in 14nm CMOS	C6-2 14:25-14:50 Yonsei Univ. A 0.02mm ² 100dB-DR Impedance Monitoring IC with PWM-Dual GRO Architecture	T3-2 14:25-14:50 (Invited) CNRS Towards Scalable Quantum Computing Based on Silicon Spin	T4-2 14:25-14:50 Univ. of Notre Dame Fundamental Understanding and Control of Device-To-Device Variation in Deeply Scaled Ferroelectric FETs	
	C4-3 14:50-15:15 Univ. of California, Berkeley A 138fs _{rms} -Integrated-Jitter and -249dB-FoM Clock Multiplier with -51dBc Spur Using A Digital Spur Calibration Technique in 28-nm CMOS	C5-3 14:50-15:15 KU Leuven 18μW SoC for Near-Microphone Keyword Spotting and Speaker Verification	C6-3 14:50-15:15 Georgia Institute of Technology A 21952-Pixel Multi-Modal CMOS Cellular Sensor Array with 1568-Pixel Parallel Recording and 4-Point Impedance Sensing	T3-3 14:50-15:15 The Pennsylvania State Univ. Monolithic 3D ¹ -IC Based Reconfigurable Compute-in-Memory SRAM Macro	T4-3 14:50-15:15 The Univ. of Tokyo Experimental Demonstration of Ferroelectric HfO ₂ FET with Ultrathin-Body IGZO for High-Density and Low-Power Memory Application	
	C4-4 15:15-15:40 Hong Kong Univ. of Science and Technology A 2.2μW 600kHz Frequency-Locked Relaxation Oscillator with 0.046%/V Voltage and 48.69ppm/°C Temperature Stability for IoT Sensor Node Applications	C5-4 15:15-15:40 Columbia Univ. Catena: A 0.5-V Sub-0.4-mW 16-Core Spatial Array Accelerator for Mobile and Embedded Computing	C6-4 15:15-15:40 Technical Univ. of Munich A CMOS Temperature Stabilized 2-Dimensional Mechanical Stress Sensor with 11-bit Resolution	T3-4 15:15-15:40 National Chiao Tung Univ. Extremely Compact Integrate-and-Fire STT-MRAM Neuron: A Pathway Toward All-Spin Artificial Deep Neural Network	T4-4 15:15-15:40 Purdue Univ. Ferroelectric and Anti-Ferroelectric Hafnium Zirconium Oxide: Scaling Limit, Switching Speed and Record High Polarization Density	
16:00-18:05	C7: Data Converter Techniques		C8: Low-Power Wireless		T5: Focus Session - 3D Integration and Packaging	
	C7-1 16:00-16:25 The Univ. of Texas at Austin A 75.8dB-SNDR Pipeline SAR ADC with 2 nd -order Interstage Gain Error Shaping	C8-1 16:00-16:25 Intel An Ultra-Low Power, Fully Integrated Wake-Up Receiver and Digital Baseband with All-Digital Impairment Correction and -92.4dBm Sensitivity for 802.11ba	C9-1 16:00-16:25 Kandou Bus A 1.02pJ/b 417Gb/s/mm USR Link in 16nm FinFET	T5-1 16:00-16:25 (Invited) Samsung The Future of Advanced Package Solutions	T6-1 16:00-16:25 Macronix International Comprehensive Scaling Study on 3D Cross-Point PCM Toward 1Znm Node for SCM Applications	
	C7-2 16:25-16:50 MediaTek An Amplifier-Less Calibration-Free SAR ADC Achieving >100dB SNDR for Multi-Channel ECG Acquisition with 667mV ^{pp} Linear Input Range	C8-2 16:25-16:50 Auburn Univ. A 3.8 mW Sub-Sampling Direct RF-to-Digital Converter for Polar Receiver Achieving 1.94 Gb/s Data Rate with 1024-APSK Modulation	C9-2 16:25-16:50 Seoul National Univ. A 370-fJ/b, 0.0056 mm ² /DQ, 4.8-Gb/s DQ Receiver for HBM3 with a Baud-Rate Self-Tracking Loop	T5-2 16:25-16:50 (Invited) ASE Heterogeneous Integration Roadmap - Driving Force & Enabling Technology for Systems of the Future	T6-2 16:25-16:50 POSTECH Ultra-Thin (<10nm) Dual-Oxide (Al ₂ O ₃ /TiO ₂) Hybrid Device (Memory/Selector) with Extremely Low I _{off} (<1nA) and I _{reset} (<1nA) for 3D Storage Class Memory	
	C7-3 16:50-17:15 KAIST A 40nm CMOS 12b 200MS/s Single-Amplifier Dual-Residue Pipelined-SAR ADC	C8-3 16:50-17:15 Verily Life Sciences A 1.53 mm ³ Crystal-Less Standards-Compliant Bluetooth Low Energy Module for Volume Constrained Wireless Sensors	C9-3 16:50-17:15 Samsung Semiconductor An 8nm All-Digital 7.3Gb/s/pin LPDDR5 PHY with an Approximate Delay Compensation Scheme	T5-3 16:50-17:15 TSMC High Performance Heterogeneous Integration on Fan-Out RDL Interposer	T6-3 16:50-17:15 Politecnico di Milano Monte Carlo Model of Resistance Evolution in Embedded PCM with Ge-Rich GST	
	C7-4 17:15-17:40 Univ. of Twente A 0.2 - 8 MS/s flexible SAR ADC Achieving 0.35 - 2.5 fJ/Conv-Step and Using Self-Quenched Dynamic Bias Comparator	C8-4 17:15-17:40 Univ. of Virginia A -106dBm 33nW Bit-Level Duty-Cycled Tuned RF Wake-Up Receiver		T5-4 17:15-17:40 MIT 1 Kbit 6T SRAM Arrays in Carbon Nanotube FET CMOS	T6-4 17:15-17:40 IBM T. J. Watson Research Center Confined PCM-Based Analog Synaptic Devices Offering Low Resistance-Drift and 1000 Programmable States for Deep Learning	
	C7-5 17:40-18:05 Univ. of Macau A 29mW 5GS/s Time-Interleaved SAR ADC Achieving 48.5dB SNDR with Fully-Digital Timing-Skew Calibration Based on Digital-Mixing	C8-5 17:40-18:05 Univ. of California, Berkeley A Crystal-Free Single-Chip Micro Mote with Integrated 802.15.4 Compatible Transceiver, Sub-mW BLE Compatible Beacon Transmitter, and Cortex M0		T5-5 17:40-18:05 imec Buried Metal Line Compatible with 3D Sequential Integration for Top Tier Planar Devices Dynamic V _{th} Tuning and RF Shielding Applications.		
18:00-19:30						
20:00-21:30	Circuits Evening Panel Discussion			Technology Evening Panel Discussion		
	Technology We Will See Coming Out of the Tokyo Olympics and Beyond			What Will the Foundries of the Future Do?		

Diversity Luncheon: 12:45-13:55 [Le Bois]

Young Professionals and Students Micro-mentoring and Career Coaching Session: 18:15-19:15 [La Cigogne]

2019 Symposia on VLSI Technology and Circuits June 12th (Wednesday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I					
7:30-17:00	Registration (Technology and Circuits)										
8:00-10:00				T7/C10: Remarks, Awards and Plenary Session 2							
				Remarks and Award Ceremony							
				C10-1 8:40-9:20 (Plenary)							
				Facebook Inc. Computational Directions for Augmented Reality Systems							
				T7-1 9:20-10:00 (Plenary) RIKEN, Tokyo Univ. of Science Si Platform for Developing Spin-Based Quantum Computing							
10:30-12:35	C11: SRAM and DRAM		C12: LDOs for High Performance Digital		C13: High-Speed DACs and Analog Techniques		T8: AI I		T9: Ge & SiGe FET		
	C11-1	10:30-10:55	C12-1	10:30-10:55	C13-1	10:30-10:55	T8-1	10:30-10:55	T9-1	10:30-10:55	
	Arm Inc.	A 4GHz 16nm SRAM Architecture with Low-Power Features for Heterogeneous Computing Platforms	Intel	A Variation-Adaptive Integrated Computational Digital LDO in 22nm CMOS with Fast Transient Response	National Cheng Kung Univ.	A 0.07mm ² 210mW Single-1.1V-Supply 14-bit 10GS/s DAC with Concentric Parallelogram Routing and Output Impedance Compensation	IBM Research	Inference of Long-Short Term Memory Networks at Software-Equivalent Accuracy Using 2.5M Analog Phase Change Memory Devices	imec	A Record G _{MSAT} /SS _{SAT} and PBTI Reliability in Si-Passivated Ge nFinFETs by Improved Gate Stack Surface Preparation	
	Samsung Electronics	A 5Gb/spin 16Gb LPDDR4/4X Reconfigurable SDRAM with Voltage-High Keeper and a Prediction-based Fast-tracking ZQ Calibration	Qualcomm Technologies	A 7nm Leakage-Current-Supply Circuit for LDO Dropout Voltage Reduction	KAIST	A 6b 28GS/s 4-channel Time-interleaved Current-Steering DAC with Background Clock Phase Calibration	imec	Gait Identification Using Stochastic OXRRAM-Based Time Sequence Machine Learning	imec	High Performance Strained Germanium Gate All Around P-Channel Devices with Excellent Electrostatic Control for Sub-30nm L _g	
	Etron Technology	A 4.8GB/s 256Mb(x16) Reduced-Pin-Count DRAM and Controller Architecture (RPCA) to Reduce Form-Factor & Cost for IOT/Wearable/TCON/Video/AI-Edge Systems	Columbia Univ.	A 0.5-1V Input Event-Driven Multiple Digital Low-Dropout Regulator System for Supporting a Large Digital Load	The Univ. of Texas at Austin	An Energy-Efficient Comparator with Dynamic Floating Inverter Pre-Amplifier	Duke Univ.	RRAM-Based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable in Situ Nonlinear Activation	IBM Research	SiGe Channel CMOS: Understanding Dielectric Breakdown and Bias Temperature Instability Tradeoffs	
	POSTECH	Area-Efficient and Variation-Tolerant In-Memory BNN Computing Using 6T SRAM Array	Ulsan National Institute of Science and Technology	A 0.5V-V _{IN} , 0.29ps-Transient-FOM, and Sub-2mV-Accuracy Adaptive-Sampling Digital LDO Using Single-VCO-Based Edge-Racing Time Quantizer	Univ. of Michigan	A 31 pW-to-113 nW Hybrid BJT and CMOS Voltage Reference with 3.6% ±3σ-Inaccuracy from 0 °C to 170 °C for Low-Power High-Temperature Systems	National Univ. of Singapore	First Demonstration of a Fully-Printed MoS ₂ RRAM on Flexible Substrate with Ultra-Low Switching Voltage and Its Application as Electronic Synapse	IBM Research	Channel Strain Dependence of T _{inv} in Strained Si and Si _{1-x} Ge _x FETs: Internal Strain-Induced Modification of Chemical Oxidation	
	Tsinghua Univ.	A 5.1pJ/Neuron 127.3us/Inference RNN-Based Speech Recognition Processor Using 16 Computing-in-Memory SRAM Macros in 65nm CMOS	Dankook Univ.	A 300mA BGR-Recursive Low-Dropout Regulator Achieving 102-to-80dB PSR at Frequencies from 100Hz to 0.1MHz with Current Efficiency of 99.98%	The Univ. of Texas at Austin	A 0.6-V Tail-Less Inverter Stacking Amplifier with 0.96 PEF			The Univ. of Tokyo	Improvement of SiGe MOS Interface Properties with a Wide Range of Ge Contents by Using TiN/Y ₂ O ₃ Gate Stacks with TMA Passivation	
	12:35-14:00	JFS1: New Computing		C14: PLL Techniques		C15: DC-DC Converters		T10: Advanced FinFET & GAA I		T11: Embedded Memory	
	14:00-15:40	JFS1-1	14:00-14:25 (Invited)	C14-1	14:00-14:25	C15-1	14:00-14:25 (Invited)	T10-1	14:00-14:25	T11-1	14:00-14:25
	Hitachi	A Cloud-Ready Scalable Annealing Processor for Solving Large-Scale Combinatorial Optimization Problems	Hong Kong Univ. of Science and Technology	A 0.25-0.4V, Sub-0.11mW/GHz, 0.15-1.6GHz PLL Using an Offset Dual-Path Loop Architecture with Dynamic Charge Pumps	IBM T. J. Watson Research Center	A 48 V Input 0.75 V Output DC-DC Converter Power Block for HPC Systems and Datacenters	Qualcomm Technologies	7nm Mobile SoC and 5G Platform Technology and Design Co-Development for PPA and Manufacturability	Foundry Business, Samsung Electronics	High-Speed and Ultra-Low Power IoT One-Chip (MCU + Connectivity-Chip) on a Robust 28-nm Embedded Flash Process	
Univ. of Michigan	A 7.3 M Output Non-Zeros/J Sparse Matrix-Matrix Multiplication Accelerator Using Memory Reconfiguration in 40 nm	Univ. of Michigan	A Reference Oversampling Digital Phase-Locked Loop with -240 dB FOM and -80 dBc Reference Spur	The Univ. of Texas at Dallas	A Two-Phase 2MHz DSD GaN Power Converter with Master-Slave AO ² T Control for Direct 48V/1V DC-DC Conversion	Samsung Electronics	Accurate High-Sigma Mismatch Model for Low Power Design in Sub-7nm Technology	GLOBALFOUNDRIES	Turning Logic Transistors into Secure, Multi-Time Programmable, Embedded Non-Volatile Memory Elements for 14 nm FINFET Technologies and Beyond		
Univ. of Notre Dame	Spoken Vowel Classification Using Synchronization of Phase Transition Nano-Oscillators	National Univ. of Singapore	A 2.2-GHz 3.2-mW DTC-free Sampling ΔΣ Fractional-N PLL with -110 dBc/Hz In-Band Phase Noise and -246dB FoM and -83dBc Reference Spur	The Univ. of Texas at Dallas	A 10-MHz 14.3W/mm ² DAB Hysteretic Control Power Converter Achieving 2.5W/247ms Full Load Power Flipping and above 80% Efficiency in 99.9% Power Range for 5G IoTs	Samsung Electronics	Sub-10 nm Advanced FinFET Design for Different Applications in Various V _{dd} and Temperature Operation Ranges	National Chiao Tung Univ.	Embedded PUF on 14nm HKMG FinFET Platform: A Novel 2-Bit-Per-Cell OTP-Based Memory Feasible for IoT Security Solution in 5G Era		
National Tsing Hua Univ.	A 250mW 5.4G-Noel-Pixel/s Photorealistic Refocusing Processor for Full-HD Five-Camera Applications	TSMC	A 387.6fs Integrated Jitter and -80dBc Reference Spurs Ring Based PLL with Track-and-Hold Charge Pump and Automatic Loop Gain Control in 7nm FinFET CMOS	National Chiao Tung Univ.	A Right-Half-Plane Zero-Free Buck-Boost DC-DC Converter with 97.46% High Efficiency and Low Output Voltage Ripple	United Microelectronics Corp.	Fin Bending Mitigation and Local Layout Effect Alleviation in Advanced FinFET Technology Through Material Engineering and Metrology Optimization	Tohoku Univ.	Novel Quad Interface MTJ Technology and Its First Demonstration with High Thermal Stability and Switching Efficiency for STT-MRAM Beyond 2Xnm		
16:00-18:05	JFS2: IoT & Sensor		C16: Speciality I/Os		C17: Non-Volatile Memories		T12: AI II		T13: Process		
	National Univ. of Singapore	Integrated Power Management and Microcontroller for Ultra-Wide Power Adaptation Down to nW	Xilinx	A 50Gb/s Hybrid Integrated Si-Photonic Optical Link in 16nm FinFET	Renesas Electronics	A 65nm Silicon-on-Thin-Box (SOTB) Embedded 2T-MONOS Flash Achieving 0.22 pJ/bit Read Energy with 64 MHz Access for IoT Applications	National Central Univ.	Split-Gate FeFET (SG-FeFET) with Dynamic Memory Window Modulation for Non-Volatile Memory and Neuromorphic Applications	IBM Research	Gate-Cut-Last in RMG to Enable Gate Extension Scaling and Parasitic Capacitance Reduction	
	Univ. of Michigan	A 10mm ³ Light-Dose Sensing IoT ² System with 35-to-339nW 10-to-300kx Light-Dose-to-Digital Converter	Univ. of California, Berkeley	A Laser-forwarded Coherent 10Gb/s BPSK Transceiver Using Monolithic Microring Resonators in 45nm SOI CMOS	STMicroelectronics	Embedded PCM Macrocell for Automotive-Grade Microcontroller in 28nm FD-SOI Technology	Peking Univ.	Bio-Inspired Neurons Based on Novel Leaky-FeFET with Ultra-Low Hardware Cost and Advanced Functionality for All-Ferroelectric Neural Network	IBM Research	Direct Partition Measurement of Parasitic Resistance Components in Advanced Transistor Architectures	
	Keio Univ.	Low-Power and ppm-Level Detection of Gas Molecules by Integrated Metal Nanosheets	Seoul National Univ.	A 4-to-20Gb/s 1.87pJ/b Referenceless Digital CDR with Unlimited Frequency Detection Capability in 65nm CMOS	Univ. of Wisconsin-Madison	Liquid Silicon: A Nonvolatile Fully Programmable Processing-In-Memory Processor with Monolithically Integrated ReRAM for Big Data/Machine Learning Applications	National Chiao Tung Univ.	A Novel Architecture to Build Ideal-Linearity Neuromorphic Synapses on a Pure Logic FinFET Platform Featuring 2.5ns PGM-Time and 10 ¹² Endurance	IBM Research	Self-Aligned Gate Contact (SAGC) for CMOS Technology Scaling Beyond 7nm	
	Ulsan National Institute of Science and Technology	Record-High Performance Trantenna Based on Asymmetric Nano-Ring FET for Polarization-Independent Large-Scale/Real-Time THz Imaging	KAIST	A 0.87 V 12.5 Gb/s Clock-Path Feedback Equalization Receiver with Unfixed Tap Weighting Property in 65 nm CMOS	National Chiao Tung Univ.	The Demonstration of Gate Dielectric-Fuse 4kb OTP Memory Feasible for Embedded Applications in High-K Metal-gate CMOS Generations and Beyond	Univ. of Notre Dame	Biologically Plausible Energy-Efficient Ferroelectric Quasi-Leaky Integrate and Fire Neuron	National Univ. of Singapore	A Novel Fast-Turn-Around Ladder TLM Methodology with Parasitic Metal Resistance Elimination, and 2×10 ⁻¹⁰ Ω-cm ² Resolution: Theoretical Design and Experimental Demonstration	
	Microsoft	Custom Silicon and Sensors Developed for a 2nd Generation Augmented Reality User Interface	Seoul National Univ.	A 0.1pJ/b/dB 1.62-to-10.8Gb/s Video Interface Receiver with Fully Adaptive Equalization Using Un-Even Data Level	Renesas Electronics	A 24MB Embedded Flash System Based on 28nm SG-MONOS Featuring 240MHz Read Operations and Robust Over-The-Air Software Update for Automotive					
19:00-21:00	Technology / Circuits Joint Banquet										

2019 Symposia on VLSI Technology and Circuits June 13th (Thursday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
8:00-17:00	Registration (Technology and Circuits)					
8:30-10:10	C18: Sensors for Object Detection and Recognition	C19: Continuous-Time ADCs	C20: Accelerators for Security and Coding	JFS3: Technology and System for AI		T14: GeSn Device
	C18-1 8:30-8:55 Yonsei Univ. A 640x640 Fully Dynamic CMOS Image Sensor for Always-On Object Recognition	C19-1 8:30-8:55 Delft Univ. of Technology A Low Power Continuous-Time Zoom ADC for Audio Applications	C20-1 8:30-8:55 Intel A 4900 μm^2 839Mbps Side-Channel Attack Resistant AES-128 in 14nm CMOS with Heterogeneous Sboxes, Linear Masked MixColumns and Dual-Rail Key Addition	JFS3-1 8:30-8:55 (Invited) National Tsing Hua Univ. Considerations of Integrating Computing-In-Memory and Processing-In-Sensor into Convolutional Neural Network Accelerators for Low-Power Edge Devices	T14-1 8:30-8:55 National Univ. of Singapore High Performance GeSn Photodiode on a 200 mm Ge-On-Insulator Photonics Platform for Advanced Optoelectronic Integration with Ge CMOS Operating at 2 μm Band	
	C18-2 8:55-9:20 iniVation A 132 by 104 10 μm -Pixel 250 μW 1kefps Dynamic Vision Sensor with Pixel-Parallel Noise and Spatial Redundancy Suppression	C19-2 8:55-9:20 Indian Institute of Technology Madras A 24mW Chopped CTDSM Achieving 103.5dB SNDR and 107.5dB DR in a 250kHz Bandwidth	C20-2 8:55-9:20 Southeast Univ. A 923Gbps/W, 113-Cycle, 2-Sbox Energy-Efficient AES Accelerator in 28nm CMOS	JFS3-2 8:55-9:20 (Invited) IBM Research Computational Memory-Based Inference and Training of Deep Neural Networks	T14-2 8:55-9:20 National Taiwan Univ. Record Low Contact Resistivity (4.4x10 ⁻¹⁰ Ω-cm ²) to Ge Using <i>In-Situ</i> B and Sn Incorporation by CVD with Low Thermal Budget ($\leq 400^\circ\text{C}$) and without Ga	
	C18-3 9:20-9:45 Samsung Electronics An Automatic Ear Detection Technique in Capacitive Sensing Readout IC Using Cascaded Classifiers and Hovering function	C19-3 9:20-9:45 MediaTek A 71.4dB SNDR 30MHz BW Continuous-Time Delta-Sigma Modulator Using a Time-Interleaved Noise-Shaping Quantizer in 12-nm CMOS	C20-3 9:20-9:45 Intel A 1.4GHz 20.5Gbps GZIP Decompression Accelerator in 14nm CMOS Featuring Dual-Path Out-of-Order Speculative Huffman Decoder and Multi-Write Enabled Register File Array	JFS3-3 9:20-9:45 Renesas Electronics A Ternary Based Bit Scalable, 8.80 TOPS/W CNN Accelerator with Many-Core Processing-in-Memory Architecture with 896K Synapses/mm ²	T14-3 9:20-9:45 National Taiwan Univ. First Vertically Stacked, Compressively Strained, and Triangular Ge _{0.91} Sn _{0.09} pGAAFs with High I _{ON} of 19.3 μA at V _{DS} =-0.5V, G _m of 50.2 μS at V _{DS} =-0.5V and Low S _{SD} of 84mV/Dec by CVD Epitaxy and Orientation Dependent Etching	
C18-4 9:45-10:10 Univ. of Electronic Science and Technology of China A 1.54mW per Element 150 μm -Pitch-Matched Receiver ASIC with Element-Level SAR-Shared-Single-Slope Hybrid ADCs for Miniature 3D Ultrasound Probes	C19-4 9:45-10:10 Delft Univ. of Technology A 3.2mW SAR-assisted CT $\Delta\Sigma$ ADC with 77.5dB SNDR and 40MHz BW in 28nm CMOS	C20-4 9:45-10:10 Univ. of Michigan A 3.25Gb/s, 13.2pJ/b, 0.64mm ² Configurable Successive-Cancellation List Polar Decoder Using Split-Tree Architecture in 40nm CMOS	JFS3-4 9:45-10:10 Politecnico di Milano Energy-Efficient Continual Learning in Hybrid Supervised-Unsupervised Neural Networks with PCM Synapses	T14-4 9:45-10:10 National Univ. of Singapore First Demonstration of Complementary FinFETs and Tunneling FinFETs Co-Integrated on a 200 mm GeSnOI Substrate: A Pathway Towards Future Hybrid Nano-Electronics Systems		
10:30-12:35	C21: Time of Flight (ToF) 3D and Time-Resolved Sensor	C22: High-Speed PAM4 Transceivers	JFS4: The Future of Memory		T15: Advanced FinFET & GAA II	
	C21-1 10:30-10:55 (Invited) TriLumina Automotive LIDAR Technology	C22-1 10:30-10:55 Intel 112 Gb/s PAM4 ADC Based SERDES Receiver for Long-Reach Channels in 10nm Process	JFS4-1 10:30-10:55 (Invited) Toshiba Circuit and Systems Based on Advanced MRAM for Near Future Computing Applications	T15-1 10:30-10:55 imec 12-EUV Layer Surrounding Gate Transistor (SGT) for Vertical 6-T SRAM: 5-nm-Class Technology for Ultra-Density Logic Devices		
	C21-2 10:55-11:20 Yonsei Univ. A 64x64 APD-Based ToF Image Sensor with Background Light Suppression Up to 200 klx Using In-Pixel Auto-Zeroing and Chopping	C22-2 10:55-11:20 Seoul National Univ. A 64Gb/s 2.29pJ/b PAM-4 VCSEL Transmitter with 3-Tap Asymmetric FFE in 65nm CMOS	JFS4-2 10:55-11:20 Toshiba Memory Ag Ionic Memory Cell Technology for Terabit-Scale High-Density Application	T15-2 10:55-11:20 TSMC Self-Heating Temperature Behavior Analysis for DC - GHz Design Optimization in Advanced FinFETs		
	C21-3 11:20-11:45 Samsung Electronics A 640x480 Indirect Time-of-Flight CMOS Image Sensor with 4-tap 7- μm Global-Shutter Pixel and Fixed-Pattern Phase Noise Self-Compensation Scheme	C22-3 11:20-11:45 TSMC A 56Gb/s Long Reach Fully Adaptive Wireline PAM-4 Transceiver in 7nm FinFET	JFS4-3 11:20-11:45 (Invited) TSMC Recent Progress and Next Directions for Embedded MRAM Technology	T15-3 11:20-11:45 imec Economics of Semiconductor Scaling: A Cost Analysis for Advanced Technology Node		
	C21-4 11:45-12:10 Univ. of Edinburgh A 128x120 5-Wire 1.96mm ² 40nm/90nm 3D Stacked SPAD Time Resolved Image Sensor SoC for Microendoscopy	C22-4 11:45-12:10 TSMC A 56Gb/s PAM-4 Receiver with Voltage Pre-Shift CTLE and 10-Tap DFE of Tap-1 Speculation in 7nm FinFET	JFS4-4 11:45-12:10 (Invited) STMicroelectronics The PCM Way for Embedded Non Volatile Memories Applications	T15-4 11:45-12:10 imec Device-, Circuit- & Block-Level Evaluation of CFET in a 4 Track Library		
	C21-5 12:10-12:35 Univ. of California, Berkeley Fully Integrated Coherent LiDAR in 3D-Integrated Silicon Photonics/65nm CMOS	C22-5 12:10-12:35 Hong Kong Univ. of Science and Technology A 52-Gb/s Sub-1pJ/bit PAM4 Receiver in 40-nm CMOS for Low-Power Interconnects	JFS4-5 12:10-12:35 (Late News) imec Manufacturable 300mm Platform Solution for Field-Free Switching SOT-MRAM	T15-5 12:10-12:35 Qualcomm Technologies 2nm Node: Benchmarking FinFET Vs Nano-Slab Transistor Architectures for Artificial Intelligence and Next Gen Smart Mobile Devices		
12:35-14:00	Luncheon Talk					
Developing Visual Systems for Entertainment and Art						
14:00-15:40	C23: Biomedical Circuits and Systems	C24: AI Accelerators	T16: 3D NAND		T17: Ferroelectric II	
	C23-1 14:00-14:25 KAIST A Multimodal Multichannel Neural Activity Readout IC with 0.7 μW /Channel Ca ²⁺ -Probe-Based Fluorescence Recording and Electrical Recording	C24-1 14:00-14:25 NVIDIA A 0.11 pJ/Op, 0.32-128 TOPS, Scalable, Multi-Chip-Module-Based Deep Neural Network Accelerator with Ground-Reference Signaling in 16nm	T16-1 14:00-14:25 Macronix International Advantage of Extremely-Thin Body (Tsi~3nm) Device to Boost The Memory Window for 3D NAND Flash	T17-1 14:00-14:25 The Univ. of Tokyo Transient Negative Capacitance as Cause of Reverse Drain-Induced Barrier Lowering and Negative Differential Resistance in Ferroelectric FETs		
	C23-2 14:25-14:50 KAIST A 100Mb/s Galvanically-Coupled Body-Channel-Communication Transceiver with 4.75pJ/b TX and 26.8 pJ/b RX for Bionic Arms	C24-2 14:25-14:50 KAIST A Full HD 60 fps CNN Super Resolution Processor with Selective Caching based Layer Fusion for Mobile Devices	T16-2 14:25-14:50 Macronix International A Novel Confined Nitride-Trapping Layer Device for 3D NAND Flash with Robust Retention Performances	T17-2 14:25-14:50 Taiwan Semiconductor Research Institute A Comprehensive Kinetic Modeling of Polymorphic Phase Distribution of Ferroelectric-Dielectrics and Interfacial Energy Effects on Negative Capacitance FETs		
	C23-3 14:50-15:15 POSTECH A 143mW Glucose-Monitoring Smart Contact Lens IC with a Dual-Mode Transmitter for Wireless-Powered Backscattering and RF-Radiated Transmission Using a Single Loop Antenna	C24-3 14:50-15:15 KAIST A 1.32 TOPS/W Energy Efficient Deep Neural Network Learning Processor with Direct Feedback Alignment based Heterogeneous Core Architecture	T16-3 14:50-15:15 Seoul National Univ. Modeling of Charge Loss Mechanisms During The Short Term Retention Operation in 3-D NAND Flash Memories	T17-3 14:50-15:15 National Chiao Tung Univ. Negative Capacitance CMOS Field-Effect Transistors with Non-Hysteretic Steep Sub-60mV/Dec Swing and Defect-Passivated Multidomain Switching		
	C23-4 15:15-15:40 Zhejiang Univ. A 108dB DR Hybrid-CTDT Direct-Digitalization $\Delta\Sigma$ -EM Front-End with 720mV _{pp} Input Range and >300mV Offset Removal for Wearable Bio-Signal Recording	C24-4 15:15-15:40 Univ. of Michigan SNAP: A 1.67 - 21.55TOPS/W Sparse Neural Acceleration Processor for Unstructured Sparse Deep Neural Network Inference in 16nm CMOS	T16-4 15:15-15:40 Chuo Univ. Pre-Shipment Data-Retention/Read-Disturb Lifetime Prediction & Aftermarket Cell Error Detection & Correction by Neural Network for 3D-TLC NAND Flash Memory	T17-4 15:15-15:40 Purdue Univ. Microscopic Crystal Phase Inspired Modeling of Zr Concentration Effects in Hf _{1-x} Zr _x O ₂ Thin Films		
16:00-18:05	C25: Biosensors	C26: Power Management & Energy Harvester	T18: ReRAM & Selector		T19: III-V & 2D	
	C25-1 16:00-16:25 Univ. of Michigan A 1.7x4.1x2 mm ³ Fully Integrated pH Sensor for Implantable Applications using Differential Sensing and Drift-Compensation	C26-1 16:00-16:25 Univ. of Science and Technology of China A 6.78MHz 92.3%-Peak-Efficiency Single-Stage Wireless Charger with CC-CV Charging and On-Chip Bootstrapping Techniques	T18-1 16:00-16:25 Intel Non-Volatile RRAM Embedded into 22FLL FinFET Technology	T19-1 16:00-16:25 SMART GaN HEMTs with Breakdown Voltage of 2200 V Realized on a 200 mm GaN-on-Insulator(GNOI)-on-Si Wafer		
	C25-2 16:25-16:50 Stanford Univ. An Aptamer-based Electrochemical-Sensing Implant for Continuous Therapeutic-Drug Monitoring <i>in vivo</i>	C26-2 16:25-16:50 National Chiao Tung Univ. A High Current efficiency Stacked Digital Low Dropout Array with True-Random-Noise Injection and Ultralow Output Ripple for Power-Side Channel Attack Protection	T18-2 16:25-16:50 National Tsing Hua Univ. A 40nm 2Mb ReRAM Macro with 85% Reduction in FORMING Time and 99% Reduction in Page-Write Time Using Auto-FORMING and Auto-Write Schemes	T19-2 16:25-16:50 TSMC First Demonstration of 40-nm Channel Length Top-Gate WS ₂ pFET Using Channel Area-Selective CVD Growth Directly on SiO ₂ /Si Substrate		
	C25-3 16:50-17:15 Univ. of California, Berkeley A 114GHz Biosensor with Integrated Dielectrophoresis for Single Cell Characterization	C26-3 16:50-17:15 Univ. of Virginia A Piezoelectric Energy-Harvesting System with Parallel-SSHI Rectifier and Integrated MPPT Achieving 417% Energy-Extraction Improvement and 97% Tracking Efficiency	T18-3 16:50-17:15 Chuo Univ. Application-Induced Cell Reliability Variability-Aware Approximate Computing in TaO _x -Based ReRAM Data Center Storage for Machine Learning	T19-3 16:50-17:15 MIT Reassessing Ingaas for Logic: Mobility Extraction in Sub-10nm Fin-Width FinFETs		
	C25-4 17:15-17:40 Univ. of California, San Diego A Sub-pA Current Sensing Front-End for Transient Induced Molecular Spectroscopy	C26-4 17:15-17:40 Korea Univ. A Bidirectional High-Voltage Dual-Input Buck Converter for Triboelectric Energy-Harvesting Interface Achieving 70.72% End-to-End Efficiency	T18-4 17:15-17:40 Institute of Microelectronics of the Chinese Academy of Sciences Nb _{1-x} O ₂ Based Universal Selector with Ultra-High Endurance (>10 ¹²), High Speed (10ns) and Excellent V _{th} Stability	T19-4 17:15-17:40 Seoul National Univ. Monolithic Integration of GaAs/InGaAs Photodetectors for Multicolor Detection		
			T18-5 17:40-18:05 Liverpool John Moores Univ. Evidence of Filamentary Switching and Relaxation Mechanisms in Ge _x Se _{1-x} OTS Selectors			