2019 Symposia on VLSI Technology and Circuits June 10th (Monday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:30-18:00	Registration (Technology and Circuits)					
8:30-12:20		**Short Course 3** **Opportunities and Challenges at the Intersection of Security and AI** **8:30 Introduction to Artificial Intelligence & Security,** R. Aitken, ARM Ltd. **9:20 Mobile Deep Learning Processors: Turning Challenges into Opportunities,** H.-J. Yoo, KAIST **10:10 Break** **10:40 AI Computing Architectures and Hardware,** J. Burns, IBM **11:30 Nonvolatile Circuit for AI Edge Applications,** M.-F. Chang, National Tsing-Hua Univ.	**Short Course 2** **Advanced 5G Circuits, Systems and Applications** **8:30 5G Real and Future,** T. Nakamura, NTT Docomo **9:20 mmWave RFIC Technologies for 5G Infrastructure Applications,** S.-G. Yang, Samsung **10:10 Break** **10:40 The Hitchhiker's Guide to Saving Moore's Law in the 5G Era,** H.-J. Lee, Intel Corp. **11:30 Design Challenges and Solutions of LO Generation for 5G Mobile Systems,** J.-H. Choi , UNIST	**Short Course 1** **CMOS Technology Enablers for Pushing the Limits of Semiconductors: Materials to Packaging** **8:30 Breaking the Limitations of FinFET Scaling,** M. Liu, Intel Corp. **9:20 Emerging Interconnect Technologies for Nanoelectronics,** K. Saraswat, Stanford Univ. **10:10 Break** **10:40 Advanced Process Technologies Required for Future Scaling and Devices,** R. Clark, TEL **11:30 DTCO in 2019: The Precious Metal Stack and the Route to Better Designs,** B. Cline, ARM Ltd.	8:30-17:40 2019 Silicon Nanoelectronics Workshop (Day 2)
12:20-13:10		**12:20 Lunch**	**12:20 Lunch**	**12:20 Lunch**		
13:10-16:50	Demo Setup	**13:10 RRAM Fabric for In-memory Computing and Neuromorphic Computing Applications,** W. Lu, Univ. of Michigan **14:00 Circuit Design Resistant to Side Channel Attacks,** N. Homma, Tohoku Univ., **14:50 Break** **15:10 Energy-efficient Circuits for Cryptography and Entropy Generation,** S. Mathew, Intel Corp. **16:00 Introduction to Electromagnetic Information Security,** Y. Hayashi, Nara Institute of Science and Technology	**13:10 Acoustic Filter for 5G Smartphones,** H. Nakamura, Skyworks **14:00 Substrate Material and Packaging Technology for 5G Millimeter Wave Communication,** K. Sudo, Murata **14:50 Break** **15:10 Beamforming Circuits, Systems, and Operations for 5G MIMO Systems,** H. Wang, Georgia Institute of Tech. **16:00 Built-In Test and Calibration of Phased Arrays,** B. Floyd , NCSU	**13:10 3D Integration for More Moore and More than Moore,** C.-H. Tung, TSMC **14:00 Recent STT-MRAM Technology: From Lab to Fab,** Y. Song, Samsung **14:50 Break** **15:10 Emerging Logic Devices for Future Computing,** S. Salahuddin, Univ. of California, Berkeley **16:00 Overview in Three-dimensionally Arrayed Flash Memory Technology,** R. Katsumata, Toshiba Memory Corp.	
16:50-17:10	Demo Setup					
17:30-21:30	17:30-19:30 Demo Session & Reception			**20:00-21:30 Joint Evening Panel Discussion** **The Semiconductor Industry at a Tipping Point: What's Next?**		

June 9th (Sunday)
Sunday Workshop: 19:00-22:00, 1 [ShunjuIII], 2 [Le Bois], 3 [La Cigogne]
2019 Silicon Nanoelectronics Workshop (Day 1): 8:30-17:40 [Shunju I]
2019 Spintronics Workshop on LSI: 19:00-22:00 [Suzaku III]

2019 Symposia on VLSI Techonlogy and Circuits June 14th (Friday)

Time	Suzaku I, II, III
9:00-12:30	**Enabling Technologies for Autonomous Driving (Friday Forum)** **Envisioning Smart Mobility Society in the Connected Future,** T. Imai, Toyota Info Technology Center **Safety and Security: Changing the Outlook of the Autonomous Car,** K. Khouri, NXP Semiconductors **Electronics Technologies Evolve Automobiles!?,** N. Kawahara, DENSO Corp. **Automotive Image Sensor for Autonomous Vehicle and Adaptive Driver Assistance System,** H. Matsumoto, Sony Corp.
12:30-13:30	**The Advent of the GPU in AI/Supercomputing and its Application to Autonomous Driving,** T. Baji, NVIDIA Corp.
13:30-15:35	

Friday Evening Event: 16:15-19:35 [Taizo-in]

2019 Symposia on VLSI Technology and Circuits June 11th (Tuesday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:00-17:00	**Registration (Technology and Circuits)**					
8:00-10:00				**T1/C1: Joint Opening and Plenary Session 1** 8:00-8:40 ***Joint Welcome and Opening Remarks*** C1-1 8:40-9:20 **(Plenary)** The Univ. of Tokyo — Virtual Cyborg: Beyond Human Limits T1-1 9:20-10:00 **(Plenary)** DARPA — Managing Moore's Inflection: DARPA's Electronics Resurgence Initiative		
10:30-12:35		**C2: Advanced Wireless** C2-1 10:30-10:55 Asahi Kasei Microdevices — A 76- to 81-GHz, 0.6° degree rms Phase Error Multi-channel Transmitter with a Novel Phase Detector and Compensation Technique C2-2 10:55-11:20 The Univ. of Texas at Dallas — 426-GHz Imaging Pixel Integrating a Transmitter and a Coherent Receiver with an Area of 380x470 μm^2 in 65-nm CMOS C2-3 11:20-11:45 Univ. of Southern California — A 1-5GHz Direct-Digital RF Modulator with an Embedded Time-Approximation Filter Achieving -43dB EVM at 1024 QAM C2-4 11:45-12:10 Princeton Univ. — A 26-42 GHz Broadband, Back-off efficient and VSWR Tolerant CMOS Power Amplifier Architecture for 5G Applications C2-5 12:10-12:35 Yonsei Univ. — A Time Domain Artificial Intelligence Radar for Hand Gesture Recognition Using 33-GHz Direct Sampling	**C3: High Performance Computing** C3-1 10:30-10:55 TSMC — A 7nm 4GHz Arm®-Core-based CoWoS® Chiplet Design for High Performance Computing C3-2 10:55-11:20 Univ. of Michigan — A 1.4 GHz 695 Giga RISC-V Inst/s 496-core Manycore Processor with Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS C3-3 11:20-11:45 Intel — A 250mV, 0.063J/GHash Bitcoin Mining Engine in 14nm CMOS Featuring Dual-Vcc SHA256 Datapath and 3-Phase Latch Based Clocking C3-4 11:45-12:10 ARM Research Labs — A 16nm 25mm^2 SoC with a 54.5x Flexibility-Efficiency Range from Dual-Core Arm Cortex-A53, to eFPGA, and Cache-Coherent Accelerators	**T2: Highlight** T2-1 10:30-10:55 Samsung Electronics — Enhanced Reliability of 7nm Process Technology Featuring EUV T2-2 10:55-11:20 IBM Research — Technology Challenges and Enablers to Extend Cu Metallization to Beyond 7 nm Node T2-3 11:20-11:45 TSMC — 3D Multi-Chip Integration with System on Integrated Chips (SoIC™) T2-4 11:45-12:10 Toshiba — In-Memory Reinforcement Learning with Moderately-Stochastic Conductance Switching of Ferroelectric Tunnel Junctions T2-5 12:10-12:35 MIT — Monolithic Three-Dimensional Imaging System: Carbon Nanotube Computing Circuitry Integrated Directly Over Silicon Imager	
12:35-14:00						
14:00-15:40	**C4: Advanced Frequency Generators** C4-1 14:00-14:25 Tokyo Institute of Technology — 0.2mW 70fs_{rms}-Jitter Injection-Locked PLL Using De-Sensitized SSPD-Based Injecting-Time Self-Alignment Achieving -270dB FoM and -66dBc Reference Spur C4-2 14:25-14:50 The Hong Kong Univ. of Science and Technology — A 270-GHz Fully-Integrated Frequency Synthesizer in 65nm CMOS C4-3 14:50-15:15 Univ. of California, Berkeley — A 138fs_{rms}-Integrated-Jitter and -249dB-FoM Clock Multiplier with -51dBc Spur Using A Digital Spur Calibration Technique in 28-nm CMOS C4-4 15:15-15:40 Hong Kong Univ. of Science and Technology — A 2.2µW 600kHz Frequency-Locked Relaxation Oscillator with 0.046%/V Voltage and 48.69ppm/°C Temperature Stability for IoT Sensor Node Applications	**C5: Energy Efficient Computing** C5-1 14:00-14:25 Semiconductor Energy Laboratory — A 48 MHz 880-nW Standby Power Normally-Off MCU with 1 Clock Full Backup and 4.69-µs Wakeup Featuring 60-nm Crystalline In-Ga-Zn Oxide BEOL-FETs C5-2 14:25-14:50 Intel — A Microwatt-Class Always-On Sensor Fusion Engine Featuring Ultra-Low-Power AOI Clocked Circuits in 14nm CMOS C5-3 14:50-15:15 KU Leuven — 18µW SoC for Near-Microphone Keyword Spotting and Speaker Verification C5-4 15:15-15:40 Columbia Univ. — Catena: A 0.5-V Sub-0.4-mW 16-Core Spatial Array Accelerator for Mobile and Embedded Computing	**C6: Physical Sensors** C6-1 14:00-14:25 imec — A 196µW Reconfigurable Light-to-Digital Converter with 119dB Dynamic Range for Wearable PPG/NIRS Sensors C6-2 14:25-14:50 Yonsei Univ. — A 0.02mm^2 100dB-DR Impedance Monitoring IC with PWM-Dual GRO Architecture C6-3 14:50-15:15 Georgia Institute of Technology — A 21952-Pixel Multi-Modal CMOS Cellular Sensor Array with 1568-Pixel Parallel Recording and 4-Point Impedance Sensing C6-4 15:15-15:40 Technical Univ. of Munich — A CMOS Temperature Stabilized 2-Dimensional Mechanical Stress Sensor with 11-bit Resolution	**T3: Focus Session - Quantum & Neuromorphic Computing** T3-1 14:00-14:25 **(Invited)** NEC — Superconductive Parametric Devices T3-2 14:25-14:50 **(Invited)** CNRS — Towards Scalable Quantum Computing Based on Silicon Spin T3-3 14:50-15:15 The Pennsylvania State Univ. — Monolithic 3D$^+$-IC Based Reconfigurable Compute-in-Memory SRAM Macro T3-4 15:15-15:40 National Chiao Tung Univ. — Extremely Compact Integrate-and-Fire STT-MRAM Neuron: A Pathway Toward All-Spin Artificial Deep Neural Network	**T4: Ferroelectric I** T4-1 14:00-14:25 Univ. of Notre Dame — Energy-Efficient Edge Inference on Multi-Channel Streaming Data in 28nm HKMG FeFET Technology T4-2 14:25-14:50 Univ. of Notre Dame — Fundamental Understanding and Control of Device-To-Device Variation in Deeply Scaled Ferroelectric FETs T4-3 14:50-15:15 The Univ. of Tokyo — Experimental Demonstration of Ferroelectric HfO_2 FET with Ultrathin-Body IGZO for High-Density and Low-Power Memory Application T4-4 15:15-15:40 Purdue Univ. — Ferroelectric and Anti-Ferroelectric Hafnium Zirconium Oxide: Scaling Limit, Switching Speed and Record High Polarization Density
16:00-18:05	**C7: Data Converter Techniques** C7-1 16:00-16:25 The Univ. of Texas at Austin — A 75.8dB-SNDR Pipeline SAR ADC with 2nd-order Interstage Gain Error Shaping C7-2 16:25-16:50 MediaTek . — An Amplifier-Less Calibration-Free SAR ADC Achieving >100dB SNDR for Multi-Channel ECG Acquisition with 667mV^{pp} Linear Input Range C7-3 16:50-17:15 KAIST — A 40nm CMOS 12b 200MS/s Single-Amplifier Dual-Residue Pipelined-SAR ADC C7-4 17:15-17:40 Univ. of Twente — A 0.2 - 8 MS/s flexible SAR ADC Achieving 0.35 - 2.5 fJ/Conv-Step and Using Self-Quenched Dynamic Bias Comparator C7-5 17:40-18:05 Univ. of Macau — A 29mW 5GS/s Time-Interleaved SAR ADC Achieving 48.5dB SNDR with Fully-Digital Timing-Skew Calibration Based on Digital-Mixing	**C8: Low-Power Wireless** C8-1 16:00-16:25 Intel — An Ultra-Low Power, Fully Integrated Wake-Up Receiver and Digital Baseband with All-Digital Impairment Correction and -92.4dBm Sensitivity for 802.11ba C8-2 16:25-16:50 Auburn Univ. — A 3.8 mW Sub-Sampling Direct RF-to-Digital Converter for Polar Receiver Achieving 1.94 Gb/s Data Rate with 1024-APSK Modulation C8-3 16:50-17:15 Verily Life Sciences — A 1.53 mm^3 Crystal-Less Standards-Compliant Bluetooth Low Energy Module for Volume Constrained Wireless Sensors C8-4 17:15-17:40 Univ. of Virginia — A -106dBm 33nW Bit-Level Duty-Cycled Tuned RF Wake-Up Receiver C8-5 17:40-18:05 Univ. of California, Berkeley — A Crystal-Free Single-Chip Micro Mote with Integrated 802.15.4 Compatible Transceiver, Sub-mW BLE Compatible Beacon Transmitter, and Cortex M0	**C9: High-Density I/Os** C9-1 16:00-16:25 Kandou Bus — A 1.02pJ/b 417Gb/s/mm USR Link in 16nm FinFET C9-2 16:25-16:50 Seoul National Univ. — A 370-fJ/b, 0.0056 mm^2/DQ, 4.8-Gb/s DQ Receiver for HBM3 with a Baud-Rate Self-Tracking Loop C9-3 16:50-17:15 Samsung Semiconductor — An 8nm All-Digital 7.3Gb/s/pin LPDDR5 PHY with an Approximate Delay Compensation Scheme	**T5: Focus Session - 3D Integration and Packaging** T5-1 16:00-16:25 **(Invited)** Samsung — The Future of Advanced Package Solutions T5-2 16:25-16:50 **(Invited)** ASE — Heterogeneous Integration Roadmap - Driving Force & Enabling Technology for Systems of the Future T5-3 16:50-17:15 TSMC — High Performance Heterogeneous Integration on Fan-Out RDL Interposer T5-4 17:15-17:40 MIT — 1 Kbit 6T SRAM Arrays in Carbon Nanotube FET CMOS T5-5 17:40-18:05 imec — Buried Metal Line Compatible with 3D Sequential Integration for Top Tier Planar Devices Dynamic V_{th} Tuning and RF Shielding Applications.	**T6: PCM & ReRAM** T6-1 16:00-16:25 Macronix International — Comprehensive Scaling Study on 3D Cross-Point PCM Toward 1Znm Node for SCM Applications T6-2 16:25-16:50 POSTECH — Ultra-Thin (<10nm) Dual-Oxide (Al_2O_3/TiO_2) Hybrid Device (Memory/Selector) with Extremely Low I_{off} (<1nA) and I_{reset} (<1nA) for 3D Storage Class Memory T6-3 16:50-17:15 Politecnico di Milano — Monte Carlo Model of Resistance Evolution in Embedded PCM with Ge-Rich GST T6-4 17:15-17:40 IBM T. J. Watson Research Center — Confined PCM-Based Analog Synaptic Devices Offering Low Resistance-Drift and 1000 Programmable States for Deep Learning
18:00-19:30						
20:00-21:30			**Circuits Evening Panel Discussion** **Technology We Will See Coming Out of the Tokyo Olympics and Beyond**			**Technology Evening Panel Discussion** **What Will the Foundries of the Future Do?**

Diversity Luncheon: 12:45-13:55 [Le Bois]

Young Professionals and Students Micro-mentoring and Career Coaching Session: 18:15-19:15 [La Cigogne]

2019 Symposia on VLSI Technology and Circuits June 12th (Wednesday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:30-17:00	**Registration (Technology and Circuits)**					
8:00-10:00				**T7/C10: Remarks, Awards and Plenary Session 2** 8:00-8:40 ***Remarks and Award Ceremony*** C10-1 8:40-9:20 **(Plenary)** Facebook Inc. — Computational and Technology Directions for Augmented Reality Systems T7-1 9:20-10:00 **(Plenary)** The Univ. of Tokyo, RIKEN — Si Platform for Developing Spin-Based Quantum Computing		
10:30-12:35	**C11: SRAM and DRAM** C11-1 10:30-10:55 Arm Inc. — A 4GHz 16nm SRAM Architecture with Low-Power Features for Heterogeneous Computing Platforms C11-2 10:55-11:20 Samsung Electronics — A 5Gb/s/pin 16Gb LPDDR4/4X Reconfigurable SDRAM with Voltage-High Keeper and a Prediction-based Fast-tracking ZQ Calibration C11-3 11:20-11:45 Etron Technology — A 4.8GB/s 256Mb(x16) Reduced-Pin-Count DRAM and Controller Architecture (RPCA) to Reduce Form-Factor & Cost for IOT/Wearable/TCON/Video/AI-Edge Systems C11-4 11:45-12:10 POSTECH — Area-Efficient and Variation-Tolerant In-Memory BNN Computing Using 6T SRAM Array C11-5 12:10-12:35 Tsinghua Univ. — A 5.1pJ/Neuron 127.3us/Inference RNN-Based Speech Recognition Processor Using 16 Computing-in-Memory SRAM Macros in 65nm CMOS	**C12: LDOs for High Performance Digital** C12-1 10:30-10:55 Intel — A Variation-Adaptive Integrated Computational Digital LDO in 22nm CMOS with Fast Transient Response C12-2 10:55-11:20 Qualcomm Technologies — A 7nm Leakage-Current-Supply Circuit for LDO Dropout Voltage Reduction C12-3 11:20-11:45 Columbia Univ. — A 0.5-1V Input Event-Driven Multiple Digital Low-Dropout-Regulator System for Supporting a Large Digital Load C12-4 11:45-12:10 Ulsan National Institute of Science and Technology — A 0.5V-V_{IN}, 0.29ps-Transient-FOM, and Sub-2mV-Accuracy Adaptive-Sampling Digital LDO Using Single-VCO-Based Edge-Racing Time Quantizer C12-5 12:10-12:35 Dankook Univ. — A 300mA BGR-Recursive Low-Dropout Regulator Achieving 102-to-80dB PSR at Frequencies from 100Hz to 0.1MHz with Current Efficiency of 99.98%	**C13: High-Speed DACs and Analog Techniques** C13-1 10:30-10:55 National Cheng Kung Univ. — A 0.07mm^2 210mW Single-1.1V-Supply 14-bit 10GS/s DAC with Concentric Parallelogram Routing and Output Impedance Compensation C13-2 10:55-11:20 KAIST — A 6b 28GS/s 4-channel Time-interleaved Current-Steering DAC with Background Clock Phase Calibration C13-3 11:20-11:45 The Univ. of Texas at Austin — An Energy-Efficient Comparator with Dynamic Floating Inverter Pre-Amplifier C13-4 11:45-12:10 Univ. of Michigan — A 31 pW-to-113 nW Hybrid BJT and CMOS Voltage Reference with 3.6% ±3σ-Inaccuracy from 0 ℃ to 170 ℃ for Low-Power High-Temperature Systems C13-5 12:10-12:35 The Univ. of Texas at Austin — A 0.6-V Tail-Less Inverter Stacking Amplifier with 0.96 PEF	**T8: AI I** T8-1 10:30-10:55 IBM Research — Inference of Long-Short Term Memory Networks at Software-Equivalent Accuracy Using 2.5M Analog Phase Change Memory Devices T8-2 10:55-11:20 imec — Gait Identification Using Stochastic OXRRAM-Based Time Sequence Machine Learning T8-3 11:20-11:45 Duke Univ. — RRAM-Based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable in Situ Nonlinear Activation T8-4 11:45-12:10 National Univ. of Singapore — First Demonstration of A Fully-Printed MoS_2 RRAM on Flexible Substrate with Ultra-Low Switching Voltage and Its Application as Electronic Synapse	**T9: Ge & SiGe FET** T9-1 10:30-10:55 imec — A Record G_{mSAT}/SS_{SAT} and PBTI Reliability in Si-Passivated Ge nFinFETs by Improved Gate Stack Surface Preparation T9-2 10:55-11:20 imec — High Performance Strained Germanium Gate All Around P-Channel Devices with Excellent Electrostatic Control for Sub-30nm L_G T9-3 11:20-11:45 IBM Research — SiGe Channel CMOS: Understanding Dielectric Breakdown and Bias Temperature Instability Tradeoffs T9-4 11:45-12:10 IBM Research — Channel Strain Dependence of Tinv in Strained Si and $Si_{1-x}Ge_x$ FETs: Internal Strain-Induced Modification of Chemical Oxidation T9-5 12:10-12:35 The Univ. of Tokyo — Improvement of SiGe MOS Interface Properties with A Wide Range of Ge Contents by Using TiN/Y_2O_3 Gate Stacks with TMA Passivation
12:35-14:00						
14:00-15:40	**JFS1: New Computing** JFS1-1 14:00-14:25 **(Invited)** Hitachi — A Cloud-Ready Scalable Annealing Processor for Solving Large-Scale Combinatorial Optimization Problems JFS1-2 14:25-14:50 Univ. of Michigan — A 7.3 M Output Non-Zeros/J Sparse Matrix-Matrix Multiplication Accelerator Using Memory Reconfiguration in 40 nm JFS1-3 14:50-15:15 Univ. of Notre Dame — Spoken Vowel Classification Using Synchronization of Phase Transition Nano-Oscillators JFS1-4 15:15-15:40 National Tsing Hua Univ. — A 250mW 5.4G-Novel-Pixel/s Photorealistic Refocusing Processor for Full-HD Five-Camera Applications	**C14: PLL Techniques** C14-1 14:00-14:25 Hong Kong Univ. of Science and Technology — A 0.25-0.4V, Sub-0.11mW/GHz, 0.15-1.6GHz PLL Using an Offset Dual-Path Loop Architecture with Dynamic Charge Pumps C14-2 14:25-14:50 Univ. of Michigan — A Reference Oversampling Digital Phase-Locked Loop with -240 dB FOM and -80 dBc Reference Spur C14-3 14:50-15:15 National Univ. of Singapore — A 2.2-GHz 3.2-mW DTC-free Sampling ΔΣ Fractional-N PLL with -110 dBc/Hz In-Band Phase Noise and -246dB FoM and -83dBc Reference Spur C14-4 15:15-15:40 TSMC — A 387.6fs Integrated Jitter and -80dBc Reference Spurs Ring Based PLL with Track-and-Hold Charge Pump and Automatic Loop Gain Control in 7nm FinFET CMOS	**C15: DC-DC Converters** C15-1 14:00-14:25 **(Invited)** IBM T. J. Watson Research Center — A 48 V Input 0.75 V Output DC-DC Converter Power Block for HPC Systems and Datacenters C15-2 14:25-14:50 The Univ. of Texas at Dallas — A Two-Phase 2MHz DSD GaN Power Converter with Master-Slave AO^{2}T Control for Direct 48V/1V DC-DC Conversion C15-3 14:50-15:15 The Univ. of Texas at Dallas — A 10-MHz 14.3W/mm^2 DAB Hysteretic Control Power Converter Achieving 2.5W/247ns Full Load Power Flipping and above 80% Efficiency in 99.9% Power Range for 5G IoTs C15-4 15:15-15:40 National Chiao Tung Univ. — A Right-Half-Plane Zero-Free Buck-Boost DC-DC Converter with 97.46% High Efficiency and Low Output Voltage Ripple	**T10: Advanced FinFET & GAA I** T10-1 14:00-14:25 Qualcomm Technologies — 7nm Mobile SoC and 5G Platform Technology and Design Co-Development for PPA and Manufacturability T10-2 14:25-14:50 Samsung Electronics — Accurate High-Sigma Mismatch Model for Low Power Design in Sub-7nm Technology T10-3 14:50-15:15 Samsung Electronics — Sub-10 nm Advanced FinFET Design for Different Applications in Various Vdd and Temperature Operation Ranges T10-4 15:15-15:40 United Microelectronics Corp. — Fin Bending Mitigation and Local Layout Effect Alleviation in Advanced FinFET Technology Through Material Engineering and Metrology Optimization	**T11: Embedded Memory** T11-1 14:00-14:25 Foundry Business, Samsung Electronics — High-Speed and Ultra-Low Power IoT One-Chip (MCU + Connectivity-Chip) on a Robust 28-nm Embedded Flash Process T11-2 14:25-14:50 GLOBALFOUNDRIES — Turning Logic Transistors into Secure, Multi-Time Programmable, Embedded Non-Volatile Memory Elements for 14 nm FINFET Technologies and Beyond T11-3 14:50-15:15 National Chiao Tung Univ. — Embedded PUF on 14nm HKMG FinFET Platform: A Novel 2-Bit-Per-Cell OTP-Based Memory Feasible for IoT Secuirty Solution in 5G Era T11-4 15:15-15:40 Tohoku Univ. — Novel Quad Interface MTJ Technology and Its First Demonstration with High Thermal Stability and Switching Efficiency for STT-MRAM Beyond 2Xnm
16:00-18:05	**JFS2: IoT & Sensor** JFS2-1 16:00-16:25 National Univ. of Singapore — Integrated Power Management and Microcontroller for Ultra-Wide Power Adaptation Down to nW JFS2-2 16:25-16:50 Univ. of Michigan — A 10mm^3 Light-Dose Sensing IoT^2 System with 35-to-339nW 10-to-300klx Light-Dose-to-Digital Converter JFS2-3 16:50-17:15 Keio Univ. — Low-Power and ppm-Level Detection of Gas Molecules by Integrated Metal Nanosheets JFS2-4 17:15-17:40 Ulsan National Institute of Science and Technology — Record-High Performance Trantenna Based on Asymmetric Nano-Ring FET for Polarization-Independent Large-Scale/Real-Time THz Imaging JFS2-5 17:40-18:05 **(Invited)** Microsoft — Custom Silicon and Sensors Developed for a 2nd Generation Augmented Reality User Interface	**C16: Speciality I/Os** C16-1 16:00-16:25 Xilinx — A 50Gb/s Hybrid Integrated Si-Photonic Optical Link in 16nm FinFET C16-2 16:25-16:50 Univ. of California, Berkeley — A Laser-forwarded Coherent 10Gb/s BPSK Transceiver Using Monolithic Microring Resonators in 45nm SOI CMOS C16-3 16:50-17:15 Seoul National Univ. — A 4-to-20Gb/s 1.87pJ/b Referenceless Digital CDR with Unlimited Frequency Detection Capability in 65nm CMOS C16-4 17:15-17:40 KAIST — A 0.87 V 12.5 Gb/s Clock-Path Feedback Equalization Receiver with Unfixed Tap Weighting Property in 65 nm CMOS C16-5 17:40-18:05 Seoul National Univ. — A 0.1pJ/b/dB 1.62-to-10.8Gb/s Video Interface Receiver with Fully Adaptive Equalization Using Un-Even Data Level	**C17: Non-Volatile Memories** C17-1 16:00-16:25 Renesas Electronics — A 65nm Silicon-on-Thin-Box (SOTB) Embedded 2T-MONOS Flash Achieving 0.22 pJ/bit Read Energy with 64 MHz Access for IoT Applications C17-2 16:25-16:50 STMicroelectronics — Embedded PCM Macrocell for Automotive-Grade Microcontroller in 28nm FD-SOI Technology C17-3 16:50-17:15 Univ. of Wisconsin-Madison — Liquid Silicon: A Nonvolatile Fully Programmable Processing-In-Memory Processor with Monolithically Integrated ReRAM for Big Data/Machine Learning Applications C17-4 17:15-17:40 National Chiao Tung Univ. — The Demonstration of Gate Dielectric-Fuse 4kb OTP Memory Feasible for Embedded Applications in High-K Metal-gate CMOS Generations and Beyond C17-5 17:40-18:05 Renesas Electronics — A 24MB Embedded Flash System Based on 28nm SG-MONOS Featuring 240MHz Read Operations and Robust Over-The-Air Software Update for Automotive	**T12: AI II** T12-1 16:00-16:25 National Central Univ. — Split-Gate FeFET (SG-FeFET) with Dynamic Memory Window Modulation for Non-Volatile Memory and Neuromorphic Applications T12-2 16:25-16:50 Peking Univ. — Bio-Inspired Neurons Based on Novel Leaky-FeFET with Ultra-Low Hardware Cost and Advanced Functionality for All-Ferroelectric Neural Network T12-3 16:50-17:15 National Chiao Tung Univ. — A Novel Architecture to Build Ideal-Linearity Neuromorphic Synapses on a Pure Logic FinFET Platform Featuring 2.5ns PGM-Time and 10^{12} Endurance T12-4 17:15-17:40 Univ. of Notre Dame — Biologically Plausible Energy-Efficient Ferroelectric Quasi-Leaky Integrate and Fire Neuron	**T13: Process** T13-1 16:00-16:25 IBM Research — Gate-Cut-Last in RMG to Enable Gate Extension Scaling and Parasitic Capacitance Reduction T13-2 16:25-16:50 IBM Research — Direct Partition Measurement of Parasitic Resistance Components in Advanced Transistor Architectures T13-3 16:50-17:15 IBM Research — Self-Aligned Gate Contact (SAGC) for CMOS Technology Scaling Beyond 7nm T13-4 17:15-17:40 National Univ. of Singapore — A Novel Fast-Turn-Around Ladder TLM Methodology with Parasitic Metal Resistance Elimination, and 2×10^{-10} Ω-cm^2 Resolution: Theoretical Design and Experimental Demonstration
19:00-21:00				**Technology / Circuits Joint Banquet**		

2019 Symposia on VLSI Technology and Circuits June 13th (Thursday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
8:00-17:00	**Registration (Technology and Circuits)**					
8:30-10:10	**C18: Sensors for Object Detection and Recognition**	**C19: Continous-Time ADCs**	**C20: Accelerators for Security and Coding**	**JFS3: Technology and System for AI**		**T14: GeSn Device**
	C18-1 8:30-8:55	C19-1 8:30-8:55	C20-1 8:30-8:55	JFS3-1 8:30-8:55 **(Invited)**		T14-1 8:30-8:55
	Yonsei Univ. A 640x640 Fully Dynamic CMOS Image Sensor for Always-On Object Recognition	Delft Univ. of Technology A Low Power Continuous-Time Zoom ADC for Audio Applications	Intel A 4900μm^2 839Mbps Side-Channel Attack Resistant AES-128 in 14nm CMOS with Heterogeneous Sboxes, Linear Masked MixColumns and Dual-Rail Key Addition	National Tsing Hua Univ. Considerations of Integrating Computing-In-Memory and Processing-In-Sensorinto Convolutional Neural Network Accelerators for Low-Power Edge Devices		National Univ. of Singapore High Performance GeSn Photodiode on a 200 mm Ge-On-Insulator Photonics Platform for Advanced Optoelectronic Integration with Ge CMOS Operating at 2 μm Band
	C18-2 8:55-9:20	C19-2 8:55-9:20	C20-2 8:55-9:20	JFS3-2 8:55-9:20 **(Invited)**		T14-2 8:55-9:20
	iniVation A 132 by 104 10μm-Pixel 250μW 1kefps Dynamic Vision Sensor with Pixel-Parallel Noise and Spatial Redundancy Suppression	Indian Institute of Technology Madras A 24mW Chopped CTDSM Achieving 103.5dB SNDR and 107.5dB DR in a 250kHz Bandwidth	Southeast Univ. A 923Gbps/W, 113-Cycle, 2-Sbox Energy-Efficient AES Accelerator in 28nm CMOS	IBM Research Computational Memory-Based Inference and Training of Deep Neural Networks		National Taiwan Univ. Record Low Contact Resistivity ($4.4\times10^{-10}\Omega$-cm^2) to Ge Using *In-Situ* B and Sn Incorporation by CVD with Low Thermal Budget (≤400°C) and without Ga
	C18-3 9:20-9:45	C19-3 9:20-9:45	C20-3 9:20-9:45	JFS3-3 9:20-9:45		T14-3 9:20-9:45
	Samsung Electronics An Automatic Ear Detection Technique in Capacitive Sensing Readout IC Using Cascaded Classifiers and Hovering function	MediaTek . A 71.4dB SNDR 30MHz BW Continuous-Time Delta-Sigma Modulator Using a Time-Interleaved Noise-Shaping Quantizer in 12-nm CMOS	Intel A 1.4GHz 20.5Gbps GZIP Decompression Accelerator in 14nm CMOS Featuring Dual-Path Out-of-Order Speculative Huffman Decoder and Multi-Write Enabled Register File Array	Renesas Electronics A Ternary Based Bit Scalable, 8.80 TOPS/W CNN Accelerator with Many-Core Processing-in-Memory Architecture with 896K Synapses/mm^2		National Taiwan Univ. First Vertically Stacked, Compressively Strained, and Triangular $Ge_{0.91}Sn_{0.09}$ pGAAFETs with High I_{ON} of 19.3μA at V_{OV}=V_{DS}=-0.5V, G_m of 50.2μS at V_{DS}=-0.5V and Low SS_{lin} of 84mV/Dec by CVD Epitaxy and Orientation Dependent Etching
	C18-4 9:45-10:10	C19-4 9:45-10:10	C20-4 9:45-10:10	JFS3-4 9:45-10:10		T14-4 9:45-10:10
	Univ. of Electronic Science and Technology of China A 1.54mW per Element 150μm-Pitch-Matched Receiver ASIC with Element-Level SAR-Shared-Single-Slope Hybrid ADCs for Miniature 3D Ultrasound Probes	Delft Univ. of Technology A 3.2mW SAR-assisted CTΔΣ ADC with 77.5dB SNDR and 40MHz BW in 28nm CMOS	Univ. of Michigan A 3.25Gb/s, 13.2pJ/b, 0.64mm^2 Configurable Successive-Cancellation List Polar Decoder Using Split-Tree Architecture in 40nm CMOS	Politecnico di Milano Energy-Efficient Continual Learning in Hybrid Supervised-Unsupervised Neural Networks with PCM Synapses		National Univ. of Singapore First Demonstration of Complementary FinFETs and Tunneling FinFETs Co-Integrated on a 200 mm GeSnOI Substrate: A Pathway Towards Future Hybrid Nano-Electronics Systems
10:30-12:35	**C21: Time of Flight (Tof) 3D and Time-Resolved Sensor**	**C22: High-Speed PAM4 Transceivers**		**JFS4: The Future of Memory**		**T15: Advanced FinFET & GAA II**
	C21-1 10:30-10:55 **(Invited)**	C22-1 10:30-10:55		JFS4-1 10:30-10:55 **(Invited)**		T15-1 10:30-10:55
	TriLumina Automotive LIDAR Technology	Intel 112 Gb/s PAM4 ADC Based SERDES Receiver for Long-Reach Channels in 10nm Process		Toshiba Circuit and Systems Based on Advanced MRAM for Near Future Computing Applications		imec 12-EUV Layer Surrounding Gate Transistor (SGT) for Vertical 6-T SRAM: 5-nm-Class Technology for Ultra-Density Logic Devices
	C21-2 10:55-11:20	C22-2 10:55-11:20		JFS4-2 10:55-11:20		T15-2 10:55-11:20
	Yonsei Univ. A 64x64 APD-Based ToF Image Sensor with Background Light Suppression Up to 200 klx Using In-Pixel Auto-Zeroing and Chopping	Seoul National Univ. A 64Gb/s 2.29pJ/b PAM-4 VCSEL Transmitter with 3-Tap Asymmetric FFE in 65nm CMOS		Toshiba Memory Ag Ionic Memory Cell Technology for Terabit-Scale High-Density Application		TSMC Self-Heating Temperature Behavior Analysis for DC - GHz Design Optimization in Advanced FinFETs
	C21-3 11:20-11:45	C22-3 11:20-11:45		JFS4-3 11:20-11:45 **(Invited)**		T15-3 11:20-11:45
	Samsung Electronics A 640x480 Indirect Time-of-Flight CMOS Image Sensor with 4-tap 7-μm Global-Shutter Pixel and Fixed-Pattern Phase Noise Self-Compensation Scheme	TSMC A 56Gb/s Long Reach Fully Adaptive Wireline PAM-4 Transceiver in 7nm FinFET		TSMC Recent Progress and Next Directions for Embedded MRAM Technology		imec Economics of Semiconductor Scaling, A Cost Analysis for Advanced Technology Node
	C21-4 11:45-12:10	C22-4 11:45-12:10		JFS4-4 11:45-12:10 **(Invited)**		T15-4 11:45-12:10
	Univ. of Edinburgh A 128x120 5-Wire 1.96mm^2 40nm/90nm 3D Stacked SPAD Time Resolved Image Sensor SoC for Microendoscopy	TSMC A 56Gb/s PAM-4 Receiver with Voltage Pre-Shift CTLE and 10-Tap DFE of Tap-1 Speculation in 7nm FinFET		STMicroelectronics The PCM Way for Embedded Non Volatile Memories Applications		imec Device-, Circuit- & Block-Level Evaluation of CFET in a 4 Track Library
	C21-5 12:10-12:35	C22-5 12:10-12:35		JFS4-5 12:10-12:35 (Late News)		T15-5 12:10-12:35
	Univ. of California, Berkeley Fully Integrated Coherent LiDAR in 3D-Integrated Silicon Photonics/65nm CMOS	Hong Kong Univ. of Science and Technology A 52-Gb/s Sub-1pJ/bit PAM4 Receiver in 40-nm CMOS for Low-Power Interconnects		imec Manufacturable 300mm Platform Solution for Field-Free Switching SOT-MRAM		Qualcomm Technologies 2nm Node: Benchmarking FinFET Vs Nano-Slab Transistor Architectures for Artificial Intelligence and Next Gen Smart Mobile Devices
12:35-14:00			**Luncheon Talk** **Developing Visual Systems for Entertainment and Art**			
14:00-15:40	**C23: Biomedical Circuits and Systems**	**C24: AI Accelerators**		**T16: 3D NAND**		**T17: Ferroelectric II**
	C23-1 14:00-14:25	C24-1 14:00-14:25		T16-1 14:00-14:25		T17-1 14:00-14:25
	KAIST A Multimodal Multichannel Neural Activity Readout IC with 0.7μW/Channel Ca^{2+}-Probe-Based Fluorescence Recording and Electrical Recording	NVIDIA A 0.11 pJ/Op, 0.32-128 TOPS, Scalable, Multi-Chip-Module-Based Deep Neural Network Accelerator with Ground-Reference Signaling in 16nm		Macronix International Advantage of Extremely-Thin Body (Tsi~3nm) Device to Boost The Memory Window for 3D NAND Flash		The Univ. of Tokyo Transient Negative Capacitance as Cause of Reverse Drain-Induced Barrier Lowering and Negative Differential Resistance in Ferroelectric FETs
	C23-2 14:25-14:50	C24-2 14:25-14:50		T16-2 14:25-14:50		T17-2 14:25-14:50
	KAIST A 100Mb/s Galvanically-Coupled Body-Channel-Communication Transceiver with 4.75pJ/b TX and 26.8 pJ/b RX for Bionic Arms	KAIST A Full HD 60 fps CNN Super Resolution Processor with Selective Caching based Layer Fusion for Mobile Devices		Macronix International A Novel Confined Nitride-Trapping Layer Device for 3D NAND Flash with Robust Retention Performances		Taiwan Semiconductor Research Institute A Comprehensive Kinetical Modeling of Polymorphic Phase Distribution of Ferroelectric-Dielectrics and Interfacial Energy Effects on Negative Capacitance FETs
	C23-3 14:50-15:15	C24-3 14:50-15:15		T16-3 14:50-15:15		T17-3 14:50-15:15
	POSTECH A 143nW Glucose-Monitoring Smart Contact Lens IC with a Dual-Mode Transmitter for Wireless-Powered Backscattering and RF-Radiated Transmission Using a Single Loop Antenna	KAIST A 1.32 TOPS/W Energy Efficient Deep Neural Network Learning Processor with Direct Feedback Alignment based Heterogeneous Core Architecture		Seoul National Univ. Modeling of Charge Loss Mechanisms During The Short Term Retention Operation in 3-D NAND Flash Memories		National Chiao Tung Univ. Negative Capacitance CMOS Field-Effect Transistors with Non-Hysteretic Steep Sub-60mV/Dec Swing and Defect-Passivated Multidomain Switching
	C23-4 15:15-15:40	C24-4 15:15-15:40		T16-4 15:15-15:40		T17-4 15:15-15:40
	Zhejiang Univ. A 108dB DR Hybrid-CTDT Direct-Digitalization ΔΣ-ΣM Front-End with 720mV$_{pp}$ Input Range and >300mV Offset Removal for Wearable Bio-Signal Recording	Univ. of Michigan SNAP: A 1.67 – 21.55TOPS/W Sparse Neural Acceleration Processor for Unstructured Sparse Deep Neural Network Inference in 16nm CMOS		Chuo Univ. Pre-Shipment Data-Retention/Read-Disturb Lifetime Prediction & Aftermarket Cell Error Detection & Correction by Neural Network for 3D-TLC NAND Flash Memory		Purdue Univ. Microscopic Crystal Phase Inspired Modeling of Zr Concentration Effects in $Hf_{1-x}Zr_xO_2$ Thin Films
16:00-18:05	**C25: Biosensors**	**C26: Power Management & Energy Harvester**		**T18: ReRAM & Selector**		**T19: III-V & 2D**
	C25-1 16:00-16:25	C26-1 16:00-16:25		T18-1 16:00-16:25		T19-1 16:00-16:25
	Univ. of Michigan A 1.7x4.1x2 mm^3 Fully Integrated pH Sensor for Implantable Applications using Differential Sensing and Drift-Compensation	Univ. of Science and Technology of China A 6.78MHz 92.3%-Peak-Efficiency Single-Stage Wireless Charger with CC-CV Charging and On-Chip Bootstrapping Techniques		Intel Non-Volatile RRAM Embedded into 22FFL FinFET Technology		SMART GaN HEMTs with Breakdown Voltage of 2200 V Realized on a 200 mm GaN-on-Insulator(GNOI)-on-Si Wafer
	C25-2 16:25-16:50	C26-2 16:25-16:50		T18-2 16:25-16:50		T19-2 16:25-16:50
	Stanford Univ. An Aptamer-based Electrochemical-Sensing Implant for Continuous Therapeutic-Drug Monitoring *in vivo*	National Chiao Tung Univ. A High Current efficiency Stacked Digital Low Dropout Array with True-Random-Noise Injection and Ultralow Output Ripple for Power-Side Channel Attack Protection		National Tsing Hua Univ. A 40nm 2Mb ReRAM Macro with 85% Reduction in FORMING Time and 99% Reduction in Page-Write Time Using Auto-FORMING and Auto-Write Schemes		TSMC First Demonstration of 40-nm Channel Length Top-Gate WS_2 pFET Using Channel Area-Selective CVD Growth Directly on SiO_x/Si Substrate
	C25-3 16:50-17:15	C26-3 16:50-17:15		T18-3 16:50-17:15		T19-3 16:50-17:15
	Univ. of California, Berkeley A 114GHz Biosensor with Integrated Dielectrophoresis for Single Cell Characterization	Univ. of Virginia A Piezoelectric Energy-Harvesting System with Parallel-SSHI Rectifier and Integrated MPPT Achieving 417% Energy-Extraction Improvement and 97% Tracking Efficiency		Chuo Univ. Application-Induced Cell Reliability Variability-Aware Approximate Computing in TaO_x-Based ReRAM Data Center Storage for Machine Learning		MIT Reassessing Ingaas for Logic: Mobility Extraction in Sub-10nm Fin-Width FinFETs
	C25-4 17:15-17:40	C26-4 17:15-17:40		T18-4 17:15-17:40		T19-4 17:15-17:40
	Univ. of California, San Diego A Sub-pA Current Sensing Front-End for Transient Induced Molecular Spectroscopy	Korea Univ. A Bidirectional High-Voltage Dual-Input Buck Converter for Triboelectric Energy-Harvesting Interface Achieving 70.72% End-to-End Efficiency		Institute of Microelectronics of the Chinese Academy of Sciences $Nb_{1-x}O_2$ Based Universal Selector with Ultra-High Endurance (>10^{12}), High Speed (10ns) and Excellent V_{th} Stability		Seoul National Univ. Monolithic Integration of GaAs//InGaAs Photodetectors for Multicolor Detection
				T18-5 17:40-18:05		
				Liverpool John Moores Univ. Evidence of Filamentary Switching and Relaxation Mechanisms in Ge_xSe_{1-x} OTS Selectors		