Symposia Demo Session

Monday, June 18, 5:30 p.m. – 7:30 p.m.
Tapa 1

The 2018 Symposia Demo Session will provide an opportunity for in-depth interactions with authors of outstanding papers selected from both Technology and Circuits sessions.

20 outstanding demonstrations will illustrate technological concepts and analyses, table-top real-time presentations of new device characterization, their chip operation highlighting key results, and systems showcasing potential applications for circuit-level innovations.

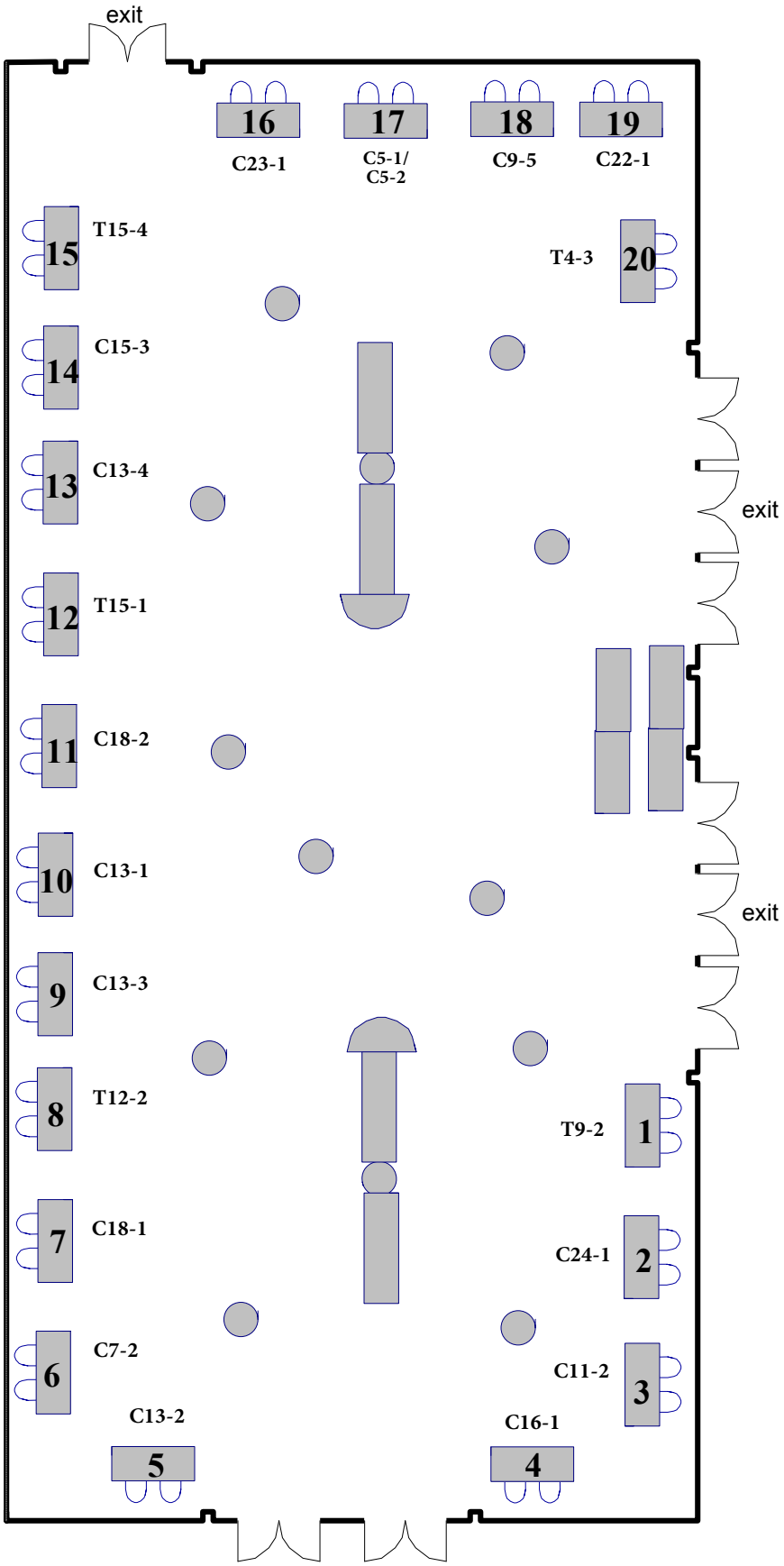
Organizers:

Technology
Kamel Benaissa, Texas Instruments
Noboyuki Sugii, Hitachi, Ltd.

Circuits
Dennis Sylvester, Michigan University
Sugako Otani, Renesas Electronics Corp.

Tapa I

IEEE VLSI
Demo Session
June 18, 2018



Booth: 1
T9-2
A Low-Power and High-Speed True Random Number Generator Using Generated RTN, *J. Brown, R. Gao, Z. Ji, J. Chen*, J. Wu*, J. Zhang, B. Zhou, Q. Shi, J. Crowford, W. Zhang, Liverpool John Moores University, *Shandong University*

The Internet of Things (IoT) is a fast-growing market where data encryption is required during the communication phase. Modern encryption algorithms rely on random numbers for cryptographic operations in almost all the security standards. Conventional random number generation requires harvesting noise from the environment as the seed. This can be slow for high-quality random number generation. A new technique is required to enhance the security of IoT devices for real-time protection. We developed one solution which injects individual defect into nano-scaled CMOS technology and from which we harvest true randomness with the random telegraph noise. By operating under AC condition, the high-quality random number can be generated with low power consumption and high speed, making it an ideal solution for future IoT appliances. In this demonstration, we will illustrate our technique and compare the speed and the amount of the generated random numbers with the conventional method.

Booth: 2
C24-1
A 4096-neuron 1M-synapse 3.8pJ/SOP Spiking Neural Network with On-chip STDP Learning and Sparse Weights in 10nm FinFET CMOS, *G. K. Chen, R. Kumar, H. E. Sumbul, P. Knag, R. K. Krishnamurthy, Intel Corporation*

A Spiking Neural Network (SNN) chip demonstrates neuromorphic workloads using on-die learning with Spike Timing Dependent Plasticity (STDP) in 10nm FinFET CMOS. The 4096-neuron 1M-synapse SNN achieves a peak throughput of 25.2GSOP/s at 0.9V and peak energy efficiency of 3.8pJ per synaptic operation at 525mV. Sparse spiking activity lowers energy by up to 9.4x and structured weight sparsity reduces memory requirements by up to 16x. The demonstration will display a visualization of key chip features including spiking activity, on-chip STDP training, and sparse weight compression. A video of the 10nm wafer probed experiment test-setup shows silicon measurements taken while running an MNIST classification workload. A live FPGA demonstration will give audience members an opportunity to interact with the SNN and experience its capabilities for themselves.

Booth: 3
C11-2
A 64µs Start-Up 26/40MHz Crystal Oscillator with Negative Resistance Boosting Technique Using Reconfigurable Multi-Stage Amplifier, *M. Miyahara, Y. Endo*, K. Okada**, A. Matsuzawa*., High Energy Accelerator Research Organization, *Tokyo Institute of Technology*

I will show crystal oscillator waveforms with and without proposed technique to compare the start-up time.

Booth: 4
C16-1
An All-Digital Unified Static/Dynamic Entropy Generator Featuring Self-Calibrating Hierarchical Von Neumann Extraction for Secure Privacy-Preserving Mutual Authentication in IoT Mote Platforms, *S. Satpathy, S. Mathew, V. Suresh, M. Anders, H. Kaul, A. Agarwal, S. Hsu, R. Krishnamurthy, V. De, Intel Corporation*

The demo will showcase unified PUF/TRNG entropy generation technique on the Sakura G FPGA kit. We will program the FPGA with the design rtl featuring proposed Von Neumann extraction and inline reconfiguration scheme. Measurement results collected (apriori) from 14nm Test-chip will be sent to the FPGA from a PC for processing in real-time. FPGA results demonstrating the impact of different self-calibrating loops and adaptive circuits will be displayed via visuals on the PC. Both PUF-ID and TRNG bit-streams will be generated from a common entropy source and their cryptographic quality will be analyzed before the audience. A video showcasing the wafer-probed measurement set-up and data collection from 14nm test-chip will also be displayed.

Booth: 5
C13-2
A 1920 × 1080 25fps, 2.4TOPS/W Unified Optical Flow and Depth 6D Vision Processor for Energy-Efficient, Low Power Autonomous Navigation, *Z. Li, J. Wang, D. Sylvester, D. Blaauw, and H.-S. Kim, University of Michigan*

This demo presents a unified 6D vision (3D coordinate + 3D motion) processor. The processor is integrated in a system with a motherboard and a camera to performs real-time dense optical flow and stereo depth computation. The system tracks the depth and moving objects of the scene.

Booth: 6
C7-2
A 220 m-Range Direct Time-of-Flight 688 × 384 CMOS Image Sensor with Sub-Photon Signal Extraction (SPSE) Pixels Using Vertical Avalanche Photo-Diodes and 6 kHz Light Pulse Counters, *S, Koyama, M. Ishii, S. Saito, M. Takemoto, Y. Nose, A. Inoue, Y. Sakata, Y. Sugiura, M. Usuda, T. Kabe, S. Kasuga, M. Mori, Y. Hirose, A. Odagawa, T. Tanaka, Panasonic Corporation*

With the use of a fabricated APD TOF CMOS image sensor, 0.25-mega 220-m-range depth-map video will demonstrate humans, cars, and obstacles at blind spot. For the demo, we will prepare a display, a PC to play the demo video, and a panel poster.

Booth: 7
C18-1
A Wireless Implantable Ultrasound Array Receiver for Thermoacoustic Imaging, *A. Sawaby, M. L. Wang, E. So, J.-C. Chien, H. Nan, B. T. Khuri-Yakub, A. Arbabian, Stanford University*
This demo is a real-time demonstration of a fully-wireless implantable thermoacoustic receiver that uses US for both power and data links through >6cm of tissue phantom. The receiver consists of 16 channels interfacing with a CMUT array, and has an integrated charge pump for biasing the CMUTs. The measured image is stored on an on-chip memory during capturing, then it is transmitted through an OOK US link. The imager achieves noise floor of 10 mPa/sqrt(Hz) over 13 MHz BW.

Booth: 8
T12-2
High-Density and Fault-Tolerant Cu Atom Switch Technology Toward 28 nm-node Nonvolatile Programmable Logic, *R. Nebashi, N. Banno, M. Miyamura, Y. Tsuji, A. Morioka, X. Bai, K. Okamoto, N. Iguchi, H. Numata, H. Hada, T. Sugibayashi, T. Sakamoto, M. Tada, NEC Corporation*

We have developed ultra-low power device/circuit technologies for realizing an atom switch programmable logic (AS-PL). The nonvolatile atom switch with a high ON/OFF resistance ratio is a key element to improve energy efficiency and soft error tolerance of FPGA. In this demo session, an image compression is demonstrated by using a 40nm-node 34k-LUT AS-PL in real time.

Booth: 9
C13-3
B-Face: 0.2 mW CNN-Based Face Recognition Processor with Face Alignment for Mobile User Identification, *S. Kang, J. Lee, C. Kim, H. Yoo, KAIST*

I will demonstrate a low power face recognition system "B-Face". The system accurately recognizes human faces using a binary weight convolutional neural network. Due to the nature of convolutional neural networks, the face recognition algorithms is highly vulnerable to rotational variances. For robust user identification with various head position, the system integrates the face alignment core to generate a frontalized face image. Integration of the face alignment core and the binary convolution core manages to accurately recognize faces with low power consumption.

Booth: 10
C13-1
Navion: A Fully Integrated Energy-Efficient Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones, *A. Suleiman, Z. Zhang, L. Carlone, S. Karman, V. Sze, Massachusetts Institute of Technology*
This demo presents Navion, A fully integrated energy-efficient Visual-Inertial Odometry (VIO) accelerator. Navion enables autonomous navigation of miniaturized robots (e.g., nano drones), and virtual/augmented reality on portable devices. The chip uses inertial measurements and mono/stereo images to estimate the camera's trajectory and a 3D map of the environment. Navion uses a state-of-the-art algorithm based on non-linear factor graph optimization, which requires large irregularly structured memories and heterogeneous computation flow. The chip can process 752x480 stereo frames at up to 171 fps, and IMU measurements at up to 52 kHz. We will show the chip processing videos and IMU measurements while visualizing the trajectory of the moving camera in real-time, without any external computation or storage, and consuming an average power of less than 24 mW. To the best of our knowledge, Navion is the first fully integrated VIO system in an ASIC."

Booth: 11
C18-2
A 0.04mm^3 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement, *X. Wu, I. Lee, Q. Dong, K. Yang, D. Kim, J. Wang, Y. Peng, Y. Zhang, M. Saligane, M. Yasuda*, K. Kumeno*, F. Ohno*, S. Miyoshi**, M. Kawaminami*, D. Sylvester & D. Blaauw 1University of Michigan, *Mie Fujitsu Semiconductor Limited, **Fujitsu Electronics America, Inc.*

This demo shows operation of a complete wireless sensor node for accurate cellular temperature measurement that includes a fully programmable Cortex-M0+ processor, custom SRAM, optical energy harvesting, 2-way communication, and a subthreshold temperature sensor. With the temperature resolution of 0.034°C RMS, the 0.04mm3 (~500× smaller than a grain of rice) fully assembled cellular temperature sensing system (CTS) is 24× smaller than prior programmable sensing systems, enabling implantation in a cluster of cells or large egg cells for biological studies.

Booth: 12
T15-1
Self-Organized Gate Stack of Ge Nanosphere/SiO_2/$Si_{1-x}Ge_x$ Enables Ge-Based Monolithically-Integrated Electronics and Photonics on Si Platform, *P. H. Liao*, M. H. Kuo*, C. W. Tien**, Y. L. Chang**, P. Y. Hong**, T. George*, H. C. Lin**, and P. W. Li*,**, *National Central University, **National Chiao Tung University*

We are going to have a poster and a carton movie to illustrate our experimental success in fabricating the first-of-its-kind, self-organized, gate-stacking heterostructires of Ge-nanosphere/SiO_2/$Si_{1-x}Ge_x$ shells over Si substrates in a standard CMOS-compatible approach at high temperature (800-900°C). Our unique MOS heterostructure of Ge-nanosphere/SiO_2/$Si_{1-x}Ge_x$-shell is analogous to the poly-Si/SiO_2/Si heterostructure, which is the quintessential basis for all CMOS devices. The primary advantages of our Ge-nanosphere/SiO_2/$Si_{1-x}Ge_x$-shell structure lie in (1) its inherent structural simplicity as well as the process elegance of being simultaneously produced within a single oxidation step

for lithographically patterned $Si_{1-y}Ge_y$ nano-pillars over a buffer Si_3N_4 layer on top of the single-crystalline Si substrate. Thus, no special surface treatments nor additional passivation processes are needed either prior to or following the formation of our Ge MOS gate-stacking heterostructures. It is important to note that such treatments and additional processes are required for the conventional, epitaxy-based fabrication processes. (2) the process-controlled capability to produce highly-stressed SiGe channels with a Ge content as high as x = 0.85 and a high degree of crystallinity, (3) size-tunable bandgap energy (0.8-3.5eV) for Ge nanospheres, and (4) strain engineering for the $Si_{0.15}Ge_{0.85}$ channels compressive strain as high as 3%. Armed with these salient features, high drive current in combination with low I_{OFF} ($I_{ON}/I_{OFF} > 10^8$ at 80K) are achievable for Ge JL n-FETs as well as high photoresponsivity (>3000A/W) and detectivity ($6\acute{}10^{12}$ cm×$Hz^{1/2}$/W) are measured on Ge NP/SiGe PTs, respectively, enabling feasibility of high-performance, functionally-diversified CMOS EPICs.

Booth: 13
C13-4
A 141 uW, 2.46 pJ/Neuron Binarized Convolutional Neural Network based Self-learning Speech Recognition Processor in 28nm CMOS, *S.Yin, P. Ouyang*, S. Zheng, D. Song, X. Li, L. Liu, S. Wei, Tsinghua University, *Beihang University*

In this demo, we will show an ultra-low power speech recognition processor fabricated in 28 nm CMOS technology, which is based on an optimized binary convolutional neural network (BCNN). This processor supports real time speech recognition with power consumption of 141 uW and energy efficiency of 2.46 pJ/Neuron when working at 2.5 MHz, while achieving at most 98.6% recognition accuracy.

Booth: 14
C15-3
A 181nW 970μg/√Hz Accelerometer Analog Front-End Employing Feedforward Noise Reduction Technique, *I. Akita, T. Okazawa, Y. Kurui*, A. Fujimoto*, T. Asano, Toyohashi University of Technology, *Toshiba Corporation*

We will demonstrate our ultra low power accelerometer analog front-end (AAFE) employing proposed noise reduction technique. In our demo system, the AAFE chip with an MCU is directly connected to PC, and its output acceleration waveform can be observed in real-time through GUI on PC, while the power consumption can be monitored at the same time.

Booth: 15
T15-4
Next-generation Fundus Camera with Full Color Image Acquisition in 0-lx Visible Light by 1.12-micron Square Pixel, 4K, 30-fps BSI CMOS Image Sensor with Advanced NIR Multi-spectral Imaging System

H.Sumi,**, T.Takehara**,S.Miyazaki**, D.Shirahige**, K.Sasagawa**, T.Tokuda**, Y.Watanabe*, N.Kishi*, J.Ohta**, M.Ishikawa*, * The University of Tokyo, **NAIST*
Using black out curtain box, we will show you the night vision color camera and reproduced realtime movie(complete 0 lux) and also demo of selfie Fundus camera I also show the Panel at the back board in Fundus camera(camera demo table)

Booth: 16
C23-1
A 5500fps 85GOPS/W 3D stacked BSI vision chip based on parallel in-focal-plane acquisition and processing, *L. Millet, S. Chevobbe, C. Andriamisaina, E. Beigne, F. Guellec, T. Dombek, L. Benaissa, E. Deschaseaux, M. Duranton, K. Benchehida, M. Darouich, M. Lepecq, CEA*

The showcased prototype called "RETINE" is inspired by the performance and flexibility of the human eye. It is the first smart sensor with in-focal-plane massively parallel pixel transfer to a programmable image processing circuit. The architecture uses dense 3D circuit integration technology and a flexible and scalable circuit architecture to reach over 1000 frames per second capture and in-sensor analysis. The concept overcomes multiple roadblocks of classical image sensors and processing systems: Classic systems use global parameters set by application that can only be adapted after a full capture and SW analysis (typically 100ms delay). RETINE can use differentiated acquisition parameters and analysis algorithms per image region and adapt the sensor settings depending on scene content in less than 1ms! State of the art smart sensors use serialized image readout that limits overall performance and costs transmission latency and power. RETINE leverages advanced 3D circuit connectivity to realize direct, parallel transmission of sensor information to co-located processing elements. This results in unequalled bandwidth and enables image analysis at ultra-low latency. The region and data dependent data processing and sensor configuration capacities allow for completely new algorithm paradigms.

The smart-sensor prototype has been realized in 130 nm CMOS technology on two stacked layers:
Layer 1 : Backside illuminated CMOS image sensor with parallel converter and direct transmission to the second, digital layer. The system can reach resolution of 192x256 @ 1000-5500 fps / 768x1024 @ 60 fps

Layer 2 : Digital processing architecture build of 192 processors, each carrying 16 parallel execution slots for SIMD execution. Up to 1000 instructions / pixel @ 1000 fps can be executed.

The demonstration will highlight some of RETINE's low-latency spatio-temporal Image Processing capabilities of and a region differentiated processing scenario"

Booth: 17
C5-1/C5-2
A 112-Gb/s PAM4 Transmitter in 16nm FinFET, *K. Tan, P.-C. Chiang, Y. Wang, H. Zhao, A. Roldan, H. Zhao, N. Narang, S. Lim, D. Carey, S. Ambatipudi, P. Upadhyaya, Y. Frans, K. Chang, Xilinx*

112Gb/s PAM4 Wireline Receiver using a 64-way Time-Interleaved SAR ADC in 16nm FinFET, *J. Hudner, D. Carey, R. Casey ,K. Hearne, P. Neto, I. Chlis, M. Erett, C. Poon, A. Laraba, H. Zhang, S. Ambatipudi, D. Mahashin, P. Upadhyaya, Y. Frans, K. Chang. Xilinx Incorporated*

Anticipating even more demand for speed and throughput, Xilinx is demonstrating 112G PAM4 transceiver fabricated in 16nm. The transceiver achieves <3e-9 pre-FEC BER over a channel with 23dB loss (BGA-to-BGA) at 28GHz. Industry experts regard 112Gb/s transceiver performance as necessary to address next-generation optical networking and line card densities. Customers can expect programmable devices with 112G transceivers in Xilinx's upcoming 7nm portfolio.

Booth: 18
C9-5
A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET, *B. Vaz, B. Verbruggen, C. Erdmann, D. Collins, J. Mcgrath, A. Boumaalif, E. Cullen, D. Walsh, A. Morgado, C. Mesadri, B. Long, R. Pathepuram, R. De La Torre, A. Manlapat, G. Karyotis, D. Tsaliagos, P. Lynch, P. Lim, D. Breathnach and B. Farley, Xilinx*

Demo board showcasing Xilinx RFSoC device including 8x RF DACs amd 8x RF ADCs. DACs provide various RF input signals to the ADCs in loop back configuration. The capabilities of the chopping interleaving calibration will be demonstrated for a few configurations and different signals. ADCs output data will be presented in a monitor in the form of FFTs.

Booth: 19
C22-1
A 1mW -101dB THD+N Class-AB High-Fidelity Headphone Driver in 65nm CMOS, *N. Mehta, J. Huijsing*, V. Stojanovic, University of California at Berkeley, *Delft University of Technology*

The paper C22-1 proposes a high-linearity low-power amplifier using new class-AB biasing and frequency compensation scheme. This demo presentation intends to capitalize on high-linearity and dynamic range of the amplifier by displaying an audiometer that records a person’s hearing sensitivity. The audiometry measures the hearing threshold by using a high-purity sinusoidal tone from 20Hz to 20kHz with dynamic range of approximately 90dB. The design presented in C22-1 is a good fit for this purpose, as it not only meets dynamic range and linearity requirements, but also unity-gain stable. Besides, amplifier’s low-power operation enables the audiometer to be battery powered and thus, fully portable.

During the demo a person is ask to wear a headphone and listen to the pure tones as the loudness-level and frequency of the tone are swept. Person flags an interrupt as soon as the sound is audible. This way the hearing threshold of a person is measured to a pre-calibrated normal hearing level of 0dB. The output is in the form of an audiogram that shows measured hearing level in decibels on Y-axis and frequency in Hertz on the X-axis. In the interest of time, the current the demo configuration will test both ears simultaneously.

Booth: 20
T4-3
High Performance High Density Gas-FET Array in Standard CMOS, *Q. Yu*, X. Zhong*, F. Boussaid**, A. Bermak*,***, C. Y. Tsui*, *Hong Kong University of Science and Technology, **University of Western Australia, ***Hamad Bin Khalifa University*

Standard CMOS integration of FET-type gas sensors with processing circuitry enables small sensing area, thus large sensor array, and fast response at room temperature operation. This enables low power, long lifetime, and wearable integrated systems for air quality monitoring. A Carbon monoxide (CO) monitoring is demonstrated due to the easy production of CO gas. CO is a very common toxic gas that may lead to a headache, dizziness, chest pain, and confusion. It’s produced during incomplete burning, which can come from motor vehicles, cooking, heating systems (stoves, furnaces, portable generators, etc.). However, it’s colorless, odorless, often confused with symptoms of flu. But it can cause unconsciousness in minutes or even death at high concentrations, extremely dangerous when people are sleeping. In the demonstration, a transparent box mimics indoor environment. A candle and the sensor chip is put inside the box. The burning of the candle turns oxygen into CO when the box is kept closed. The sensor chip detects CO and quantizes to digital output, which is transmitted to the laptop to show the CO concentration in real time. A fan is also put in the box to blow out the candle and introduce fresh air to reduce CO concentration. Then the sensor starts to recover from the CO reaction.