Technology / Circuits Short Courses June 18 - Monday				2018 Symposia on VLSI Technology and Circuits June 19th - Tuesday									
Time	Tapa 3	Tapa 2	Honolulu	Time	Tapa I		Tapa II		Tapa III				
8:20 AM	Tech SC	Circ. SC	Circ. SC		Joint Technology/Circuits Plenary and Welcome								
				8:10 AM		Welcome and Opening Remarks							
				8:40 AM	Micron Technology	Memory Technology: The Core to Enable Future Computing Systems							
				9:20 AM		EDS Presentation - IEEE Fellows Recognition							
				9:30 AM	The Univ. of Tokyo	Revolutionizing Cancer Genomic Medicine by AI and Supercomputer with Big Data							
				10:30 AM	Best Student Paper Awards and Circuits Plenary								
				10:40 AM	Nvidia	Hardware-Enabled Artificial Intelligence							
				11:20 AM		2019 Joint Announcement							
				11:30 AM	SECOM	Semiconductor Technologies Accelerate Our Future Vision: "ANSHIN Platform"							
					T2: TFS: Back-End Compatible Devices and Advanced Thermal		T3: Devices and Systems for AI		C2: SRAM Designs		C3: Wireless Systems		
				1:30 PM	STMicro	Shaping Circuit Environment to Face Thermal Challenges	IBM	Capacitor-based Cross-point Array for Analog Neural Network with Record Symmetry and Linearity	TSMC	A 290mV Ultra-Low Voltage One-Port SRAM Compiler Design Using a 12T Write Contention and Read Upset Free Bit-Cell in 7nm FinFET Technology	UC Berkeley	A Dual-Mode Configurable RF-to-Digital Receiver in 16nm FinFET	
				1:55 PM	Stanford Univ.	Thermal Management Research – From Power Electronics to Portables	The Univ. of Tokyo	Analog Spike Processing with High Scalability and Low Energy Consumption Using Thermal Degree of Freedom in Phase Transition Materials	Qualcomm	A 7nm Double-Pumped 6R6W Register File for Machine Learning Memory	Toshiba Elec. Dev. & Storage	An 113dB-Link-Budget Bluetooth-5 SoC with an 8dBm 22%-Efficiency TX	
				2:20 PM	Univ. of Minnesota	Electromigration Effects in Power Grids Characterized Using an On-Chip Test Structure with Poly Heaters and Voltage Tapping Points	Nat'l Chiao Tung Univ.	An Energy Efficient FinFET-based Field Programmable Synapse Array (FPSA) Feasible for One-shot Learning on EDGE AI	Korea Univ.	Half-and-Half Compare Content Addressable Memory with Charge-Sharing based Selective Match-Line Precharge Scheme	Keio Univ.	Fully integrated OOK-powered pad-less deep sub-wavelength-sized 5-GHz RFID with on-chip antenna using adiabatic logic in 0.18um CMOS	
				2:45 PM	Inst. of Electro-Optical Eng.	Low Thermal Budget Amorphous Indium Tungsten Oxide Nano-Sheet Junctionless Transistors with Near Ideal Subthreshold Swing	Tsinghua Univ.	Novel In-Memory Matrix-Matrix Multiplication with Resistive Cross-Point Arrays	Renesas	12-nm Fin-FET 3.0G-search/s 80-bit x 128-entry Dual-port Ternary CAM	Virginia Tech	A Fast Triple-Interferer Sensor (Detector and Digital Encoder) with In-Situ Reference Frequency Acquisition at 2.7-to-3.7GHz in 0.13um CMOS	
					T4: TFS: Sensors and Devices for IoT, Medicine and Smart Living		T5: Negative Capacitance FET		C4: Machine Learning Processors		C5: Extreme Wireline Transceivers		
				3:25 PM	CEA-LETI	Sensors & related devices for IoT, Medicine and Smart Living	NDL	A Numerical Study of Polymorphic Phase Distribution and Interfacial Layer Effects for Sub-5 nm Negative Capacitance FETs	Tsinghua Univ.	STICKER: A 0.41-62.1 TOPS/W 8bit Neural Network Processor with Multi-Sparsity Compatible Convolution Arrays and Online Tuning Acceleration for Fully Connected Layers	Xilinx	A 112-Gb/s PAM4 Transmitter in 16nm FinFET	
				3:50 PM	Nat'l Tsing Hua Univ.	Development of Multisite, Closed-loop Neuromodulator for Theranosis of Neural Degenerative Diseases	Nat'l Chiao Tung Univ.	First Experimental Demonstration of Negative Capacitance InGaAs MOSFETs With Hf0.5Zr0.5O2 Ferroelectric Gate Stack	IBM	A Scalable Multi-TeraOPS Deep Learning Processor Core for AI Training and Inference	Xilinx	112Gb/s PAM4 Wireline Receiver using a 64-way Time-Interleaved SAR ADC in 16nm FinFET	
				4:15 PM	HKUST	High Performance High Density Gas-FET Array in Standard CMOS	UC Berkeley	Response Speed of Negative Capacitance FinFETs	Tsinghua Univ.	An ultra-high energy-efficient reconfigurable processor for deep neural networks with binary/ternary weights in 28nm CMOS	Hitachi	An Active Copper-Cable Supporting 56-Gbit/s PAM4 and 28-Gbit/s NRZ with Continuous Time Linear Equalizer IC for 10-meters Reach Interconnection (Invited)	
				4:40 PM	Toshiba	High-sensitivity and low-power inertial MEMS-on-CMOS sensors using low-temperature-deposited poly SiGe film for the IoT era	Samsung	Ferroelectric Switching Delay as Cause of Negative Capacitance and the Implications to NCFETs	Intel	2.9TOPS/W Reconfigurable Dense/Sparse Matrix-Multiply Accelerator with Unified INT8/INT16/FP16 Datapath in 14nm Tri-gate CMOS	Seoul National Univ.	A 64 Gb/s 1.5 pJ/bit PAM-4 Transmitter with 3-Tap FFE and Gm-Regulated Active-Feedback Driver in 28 nm CMOS	
				5:05 PM			UC Berkeley	Negative Capacitance, n-Channel, Si FinFETs: Bi-directional Sub-60 mV/dec, Negative DIBL, Negative Differential Resistance and Improved Short Channel Effect	Renesas	New Generation Dynamically Reconfigurable Processor Technology for Accelerating Embedded AI Applications	IBM	A 0.3pJ/bit 112Gb/s PAM4 1+0.5D TX-DFE Precoder and 8-tap FFE in 14nm CMOS	
				5:30 PM									
5:30 PM	Demo Session/ Joint Reception			7:30 PM					Women in Engineering sponsored by SSCS and EDS 6:00 pm - 7:00 pm				
8:00 PM	Joint Technology/Circuits Panel Session Is the CPU Dying or Dead? Are Accelerators the Future of Computation?			8:00 PM	Technology Panel Storage Class Memories: Who cares? DRAM is Scaling Fine, NAND is Stacking Great		Circuit Panel What's the next big thing after smartphones?						

Color code
Technology (white)
Circuits (red)
Joint Technology / Circuits (green)

2018 Symposia on VLSI Technology and Circuits June 20 - Wednesday

Time	Tapa 3		Tapa 2		Tapa 1		Honolulu	
		T6 Technology Highlights			C6: Adaptive and Application Specific Digital Circuits		C7: Time-of-Flight and Advanced Image Sensors	
8:10 AM	Samsung	True 7nm Platform Technology featuring Smallest FinFET and Smallest SRAM Cell by EUV, Special Constructs and 3rd Generation Single Diffusion Break			Fujitsu	Memory Expansion Technology for Large-Scale Data Processing Using Software-Controlled SSD (Invited)	EPFL	A 252 × 144 SPAD pixel FLASH LiDAR with 1728 Dual-clock 48.8 ps TDCs, Integrated Histogramming and 14.9-to-1 Compression in 180nm CMOS Technology
8:35 AM	Global-foundries	Nanosecond Laser Anneal for BEOL Performance Boost in Advanced FinFETs			UC Berkeley	An Out-of-Order RISC-V Processor with Resilient Low-Voltage Operation in 28 nm CMOS	Panasonic	A 220 m-Range Direct Time-of-Flight 688 × 384 CMOS Image Sensor with Sub-Photon Signal Extraction (SPSE) Pixels Using Vertical Avalanche Photo-Diodes and 6 kHz
9:00 AM	Panasonic	From Memory to Sensor: ultra-Low Power and High Selectivity Hydrogen Sensor Based on ReRAM Technology			Univ. of Michigan	An Adaptive Body-Biasing SoC using in situ Slack Monitoring for Runtime Replica Calibration	TU Delft	Multipurpose, fully-integrated 128x128 event-driven MD-SiPM with 512 16-bit TDCs with 45 ps LSB and 20 ns gating
9:25 AM	TDK/ Headway Tech.	Demonstration of Ultra-Low Voltage pSTT-MRAM designed for compatibility with 0x node embedded LLC applications			Univ. of Washington	An All-Digital Unified Clock Frequency and Switched-Capacitor Voltage Regulator for Variation Tolerance in a Sub-Threshold ARM Cortex M0 Processor	Shizuoka Univ.	A Two-Tap NIR Lock-In Pixel CMOS Image Sensor with Background Light Cancelling Capability for Non-Contact Heart Rate Detection
	T7: Process and Material Technologies 1		T8: Advanced FinFET and GAA		C8: CJFS: Emerging Memory		C9: Nyquist ADC	
10:05 AM	imec	3D sequential stacked planar devices on 300mm wafers featuring replacement metal gate junction-less top devices processed at 525°C with improved reliability	Global-foundries	Multiple Workfunction High Performance FinFETs for Ultra-low Voltage Operation	TSMC	Logic Process Compatible 40nm 16Mb, Embedded Perpendicular-MRAM with Hybrid-Resistance Reference, sub-µA Sensing Resolution, and 17.5nS Read Access Time	Analog Devices	A 12-bit 31.1uW 1MS/s SAR ADC with On-Chip Input-Signal-Independent Calibration Achieving 100.4dB SFDR using 256fF Sampling Capacitance
10:30 AM	Panasonic	An over 120 dB wide-dynamic-range 3.0 µm pixel image sensor with in-pixel capacitor of 41.7 fF/um2 and high reliability enabled by BEOL 3D capacitor process	imec	An In-depth Study of High-Performing Strained Germanium Nanowire pFETs	IMEC	SOT-MRAM 300mm integration for low power and ultrafast embedded memories	Univ. of ECT of China	A 0.5-1.1V 10b Adaptive Bypassing SAR ADC Utilizing Oscillation Cycle Information of VCO-based Comparator
10:55 AM	KAIST	Selective Pore-Sealing of Highly Porous Ultralow-k dielectrics for ULSI Interconnects by Cyclic Initiated Chemical Vapor Deposition Process	imec	Si/SiGe superlattice I/O finFETs in a vertically-stacked Gate-All-Around horizontal Nanowire Technology	Toshiba	High-speed Voltage Control Spintronics Memory (VoCSM) Having Broad Design Windows	Kagoshima Univ.	A 2.3-mW, 950-MHz, 8-bit Fully-Time-Based Subranging ADC Using Highly-Linear Dynamic VTC
11:20 AM	CEA-LETI	Performance and Reliability of a Fully Integrated 3D Sequential Technology	IBM	Leakage aware Si/SiGe CMOS FinFET for low power applications	Univ. of Michigan	Energy Efficient Adiabatic FRAM with 0.99 pJ/bit Write for IoT Applications	Univ. of ECT of China	A >3GHz ERBW 1.1-GS/s 8-bit Two-Step SAR ADC with Recursive-Weight DAC
11:45 AM	National Univ. of Singapore	Metal/P-type GeSn Contacts with Specific Contact Resistivity down to 4.4×10^-10 Ohm-cm^2	Purdue Univ.	First Direct Experimental Studies of Hf0.5Zr0.5O2 Ferroelectric Polarization Switching Down to 100-picosecond in Sub-60mV/dec Germanium Ferroelectric Nanowire FETs	Global-foundries	14nm FinFET 1.5Mb Embedded High-K Charge Trap Transistor One Time Programmable Memory Using Dynamic Adaptive Programming	Xilinx	A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET
	T9: IoT Devices and Technology		T10: Resistive RAM		C10: CJFS: Power Devices and Circuits		C11: Frequency References	C12: Bio-Medical Interfaces
1:30 PM	Waseda Univ.	10µW/cm2-Class High Power Density Silicon Thermoelectric Energy Harvester Compatible with CMOS-VLSI Technology	Tsinghua Univ.	A Methodology to Improve Linearity of Analog RRAM for Neuromorphic Computing	KU Leuven	A Single-Topology Continuously-Scalable-Conversion-Ratio Fully Integrated Switched-Capacitor DC-DC Converter with 0-to-2.22V Output and 93% Peak-Efficiency	MIT	A CMOS Molecular Clock Probing 231.061-GHz Rotational Line of OCS with Sub-ppb Long-Term Stability and 66-mW DC Power	KAIST	A 0.8V 82.9µW In-ear BCI Controller System with 8.8 PEF EEG Instrumentational Amplifier and Wireless BAN Transceiver
1:55 PM	Liverpool John Moores Univ.	A low-power and high-speed True Random Number Generator using generated RTN	Zhejiang Univ.	Non-Volatile Ternary Content Addressable Memory(TCAM) with Two Ge/GeOx/Al2O3/HfO2 MOS Diodes	Tokyo Institute of Technology	New methodology for evaluating minority carrier lifetime for process assessment	High Energy Accelerator Research Org.	A 37.2nJ 64 (micro)s Start-Up 26/40MHz Crystal Oscillator with Negative Resistance Boosting Technique Using Reconfigurable Multi-Stage Amplifier	Univ. of Michigan	A Battery-Powered Opto-Electrophysiology Neural Interface with Artifact-Preventing Optical Pulse Shaping
2:20 PM	STMicroelectronics	Ultrahigh-Sensitive and CMOS Compatible ISFET Developed in BEOL of Industrial UTBB FDSOI	Stanford Univ.	Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM	KAIST	A Quasi-Digital Ultra-Fast Capacitor-less Low-Dropout Regulator Based on Comparator Control for x8 Current Spike of PCRAM systems	Univ. of Michigan	A 224 pW 260 ppm/°C Gate-Leakage-based Timer for Ultra-Low Power Sensor Nodes with Second-Order Temperature Dependency Cancellation	Univ. of Toronto	Artifact-Tolerant Opamp-less Delta-Modulated Bidirectional Neuro-Interface
2:45 PM	UC Santa Barbara	RX-PUF: Low Power, Dense, Reliable, and Resilient Physically Unclonable Functions Based on Analog Passive RRAM Crossbar Arrays	Chuo Univ.	5x Reliability Enhanced 40nm TaOx Approximate-ReRAM with Domain-Specific Computing for Real-time Image Recognition of IoT Edge Devices	Columbia Univ.	0.5V-VIN, 165-mA/mm2 Fully-Integrated Digital LDO based on Event-Driven Self-Triggering Control	National Univ. of Singapore	A Sub-Leakage pW-Power Hz-Range Relaxation Oscillator Operating with 0.3V-1.8V Unregulated Supply	imec	A 400GΩ input-impedance, 220mVpp linear-input-range, 2.8Vpp CM-interference-tolerant active electrode for non-contact capacitively coupled ECG acquisition
	T11: Process and Material Technologies 2		T12: Beyond CMOS		C13: Robotics and Machine Learning Applications		C14: Advanced Wireline and Memory Interfaces	C15: Capacitive Sensor Interfaces
3:25 PM	National Taiwan Univ.	Comprehensive Thermal SPICE Modeling of FinFETs and BEOL with Layout Flexibility Considering Frequency Dependent Thermal Time Constant, 3D Heat Flows, Boundary/Alloy Scattering, and Interfacial Thermal Resistance with	CEA-LETI	All-Electrical Control of a Hybrid Electron Spin/Valley Quantum Bit in SOI CMOS Technology	MIT	Navion: A Fully Integrated Energy-Efficient Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones	Xilinx	A 0.5-28Gb/s Wireline Tranceiver with 15-Tap DFE and Fast-Locking Digital CDR in 7nm FinFET	DGIST, Morse Micro	A 114-aFrms-Resolution 46-nF/10-MΩ-Range Digital-Intensive Reconfigurable RC-to-Digital Converter with Parasitic-Insensitive Femto-Farad Baseline Sensing
3:50 PM	IBM	Differentiated Performance and Reliability Enabled by Multi-Work Function Solution in RMG Silicon and SiGe MOSFETs	NEC	High-Density and Fault-Tolerant Cu Atom Switch Technology Toward 28nm-node Nonvolatile Programmable Logic	Univ. of Michigan	A 1920 × 1080 25fps, 2.4TOPS/W Unified Optical Flow and Depth 6D Vision Processor for Energy-Efficient, Low Power Autonomous Navigation	Samsung	A sub-0.85V, 6.4Gbp/s/pin TX-Interleaved Transceiver with Fast Wake-up Time using 2-Step Charging Control and VOH Calibration in 20nm DRAM Process	Delft Univ. of Tech.	A 117dB In-band CMRR 98.5dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing with an Electrically Floating Target
4:15 PM	Applied Materials, Inc.	Process Optimization of Perpendicular Magnetic Tunnel Junction Arrays for Last-Level Cache beyond 7 nm Node	Univ. of Notre Dame	A Threshold Switch Augmented Hybrid-FeFET (H-FeFET) with Enhanced Read Distinguishability and Reduced Programming Voltage for Non-Volatile Memory Applications	KAIST	B-Face: 0.2 mW CNN-Based Face Recognition Processor with Face Alignment for Mobile User Identification	Toshiba Memory Corporation	A 12.8 Gb/s Daisy Chain-Based Downlink I/F Employing Spectrally Compressed Multi-Band Multiplexing for High-Bandwidth and Large-Capacity Storage Systems	Toyohashi Univ. of Tech.	A 181nW 970µg/√Hz Accelerometer Analog Front-End Employing Feedforward Noise Reduction Technique
4:40 PM	National Tsing Hua Univ.	Dependence of Reliability of Ferroelectric HfZrOx on Epitaxial SiGe Film with Various Ge Content	Univ. of Notre Dame	A Circuit Compatible Accurate Compact Model for Ferroelectric-FETs	Tsinghua Univ.	A 141 uW, 2.46 pJ/Neuron Binarized Convolutional Neural Network based Self-learning Speech Recognition Processor in 28nm CMOS	Intel Corp	A Digital-Intensive 2-to-9.2 Gb/s/pin Memory Controller I/O with Fast-Response LDO in 10nm CMOS	KAIST	A 2.69uW Dual Quantization-based Capacitance-to-Digital Converter for Pressure, Humidity, and Acceleration Sensing in 0.18um CMOS
5:05 PM	Samsung	Modeling of FinFET Self-Heating Effects in multiple FinFET Technology Generations with implication for Transistor and Product Reliability	imec	Record 47 mV/dec top-down vertical nanowire InGaAs/GaAsSb tunnel FETs	Princeton Univ.	A Mixed-Signal Binarized Convolutional-Neural-Network Accelerator Integrating Dense Weight Storage and Multiplication for Reduced Data Movement	UC Berkeley	An Automated SerDes Frontend Generator Verified with a 16nm Instance Achieving 15 Gb/s at 1.96 pJ/bit	National Univ. of Singapore	An 8.2 µW 0.14 mm2 16-Channel CDMA-Like Period Modulation Capacitance-to-Digital Converter with Reduced Data Throughput
6:00 PM	Young Professionals Sponsored by SSCS/EDS									
7:00 PM	Banquet on the Great Lawn									

2018 Symposia on VLSI Technology and Circuits June 21 - Thursday

Time	Tapa 3		Tapa 2		Tapa 1		Honolulu 1		Honolulu 2	
	T13: FET Performance and Scaling		T14: TJFS: DTCO		C16: Hardware Security		C17: Advanced PLLs		C18: Wireless for Biomedical and IoT	
8:10 AM	Global-foundries	Improving Performance, Power, and Area by Optimizing Gear Ratio of Gate-Metal Pitches in Sub-10nm Node CMOS Designs	imec	Enabling CMOS Scaling Towards 3nm and Beyond	Intel	An All-Digital Unified Static/Dynamic Entropy Generator Featuring Self-Calibrating Hierarchical Von Neumann Extraction for Secure Privacy-Preserving Mutual Authentication in IoT Mote Platforms	TSMC	A Digital Bang-Bang Phase-Locked Loop with Background Injection Timing Calibration and Automatic Loop Gain Control in 7nm FinFET CMOS	Stanford Univ.	A Wireless Implantable Ultrasound Array Receiver for Thermoacoustic Imaging
8:35 AM	Nat'l Chiao Tung Univ.	Achieving High-Scalability Negative Capacitance FETs with Uniform Sub-35 mV/dec Switch Using Dopant-Free Hafnium Oxide and Gate Strain	Samsung	Smart Scaling Technology for Advanced FinFET Node	Rice Univ.	A 28nm Integrated True Random Number Generator Harvesting Entropy from MRAM	UC San Diego	AMASS PLL: An Active-Mixer-Adopted Sub-Sampling PLL Achieving an FOM of -255.5dB and a Reference Spur of -66.5dBc	Univ. of Michigan	A 0.04mm3 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement
9:00 AM	imec	The Complementary FET (CFET) for CMOS scaling beyond N3	Intel	Sub-550mV SRAM Design in 22nm FinFET Low Power (22FFL) Technology with Self-Induced Collapse Write Assist	Univ. of Washington	An All-Digital True-Random-Number Generator with Integrated De-correlation and Bias-Correction at 3.2-to-86 Mb/s, 2.58 pJ/bit in 65 nm CMOS	TSMC	A 0.2GHz to 4GHz Hybrid PLL (ADPLL/Charge-Pump-PLL) in 7nm FinFET CMOS Featuring 0.619ps Integrated Jitter and 0.6us Settling Time at 2.3mW	UC Los Angeles	Self-Regulated Wireless Power and Simultaneous 5 Mb/s Reverse Data over One Pair of Coils
9:25 AM	imec	Power-performance Trade-offs for Lateral NanoSheets on Ultra-Scaled Standard Cells	CEA-LETI	Design Technology Co-Optimization in advanced FDSOI CMOS around the Minimum Energy Point: body biasing and within-cell VT-mixing	Intel	220mV-900mV 794/584/754 Gbps/W Reconfigurable GF(24)2 AES/SMS4/Camellia Symmetric-Key Cipher Accelerator in 14nm Tri-gate CMOS	Ulsan Nat'l Institute of Science and Technology (UNIST)	153 fsRMS-Integrated-Jitter and 114-Multiplication Factor PVT-Robust 22.8 GHz Ring-LC-Hybrid Injection-Locked Clock Multiplier	Intel	A Single-Stage, Single-Inductor, 6-Input 9-Output Multi-Modal Energy Harvesting Power Management IC for 100µW-120mW Battery-Powered IoT Edge Nodes
	T15: Photonics and RF/Analog		T16: TJFS: In Memory and In Sensor Computing		C19: Oversampling Data Converters		C20: RF Circuits and Techniques		C21: Power Converters	
10:05 AM	Nat'l Central Univ.	Self-organized gate stack of Ge nanosphere/SiO2/Si1-xGex enables Ge-based monolithically-integrated electronics and photonics on Si platform	Seoul Nat'l Univ.	Neuromorphic Technology Based on Charge Storage Memory Devices	Yonsei Univ.	A 1.2V 68µW 98.2dB-DR Audio Continuous-Time Delta-Sigma Modulator	The Univ. Texas at Dallas	Terahertz RF Front-End Employing Even-Order Subharmonic MOS Symmetric Varactor Mixers in 65-nm CMOS for Hydration Measurements at 560 GHz	Analog Device	A 95.3% Peak Efficiency, 135nA Quiescent Current Buck-Boost DC-DC Converter with Current-Slope-Based Mode Control
10:30 AM	Nat'l Univ. Singapore	A Near- & Short-Wave IR Tunable InGaAs Nanomembrane PhotoFET on Flexible Substrate for Lightweight and Wide-Angle Imaging Applications	Nat'l Tsing Hua Univ.	Nonvolatile Circuit-Device Interaction for Memory, Logic and AI	Univ. of Electronic Science and Technology of China	A 0.029mm^2 17-fJ/Conv.-Step CT Delta-Sigma ADC With 2nd-Order Noise-Shaping SAR Quantizer	Univ. of Southern California	A Sub-Harmonic Switching Digital Power Amplifier with Hybrid Class-G Operation for Enhancing Power Back-off Efficiency	KAIST	A Hybrid Dual-Path Step-Down Converter with 96.2% Peak Efficiency using a 250mΩ of Large-DCR Inductor
10:55 AM	Nat'l Univ. Singapore	Integration of 2D Black Phosphorus Phototransistor and Silicon Photonics Waveguide System Towards Mid-Infrared On-Chip Sensing Applications	Columbia Univ.	XNOR-SRAM: In-Memory Computing SRAM Macro for Binary/Ternary Deep Neural Networks	Univ. of Macau	A 77dB SNDR 12.5MHz Bandwidth 0-1 MASH ΣΔ ADC Based on the Pipelined-SAR Structure	imec	A 5.5 GHz Background-Calibrated Subsampling Polar Transmitter with -41.3 dB EVM at 1024 QAM in 28nm CMOS	Shinshu Univ.	A 92.8% Efficiency Adaptive-On/Off-Time Control 3-Level Buck Converter for Wide Conversion Ratio with Shared Charge Pump Intermediate Voltage Regulator
11:20 AM	The Univ. of Tokyo	Next-generation Fundus Camera with Full Color Image Acquisition in 0-lx Visible Light by 1.12-micron Square Pixel, 4K, 30-fps BSI CMOS Image Sensor with Advanced NIR Multi-spectral Imaging	Panasonic	A 4M Synapses integrated Analog ReRAM based 66.5 TOPS/W Neural-Network Processor with Cell Current Controlled Writing and Flexible Network Architecture	Asahi Kasei Micro-devices	A 1.25MS/s Two-Step Incremental ADC with 100dB DR and 110dB SFDR	HKUST	A 16-Gb/s 0-dB Power Back-off 16-QAM Transmitter at 28 GHz in 65-nm CMOSX	Nat'l Chiao Tung Univ.	An Ultra-low Quiescent Current 250nA Low Dropout Regulator for No-load to 10mA Internet-of-Everything Applications
11:45 AM	IBM	InGaAs-on-Insulator MOSFETs Featuring Scaled Logic Devices and Record RF Performance	Macronix	A Novel 3D AND-type NVM Architecture Capable of High-density, Low-power In-Memory Sum-of-Product Computation for Artificial Intelligence Application	Univ. of Macau	A 550uW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental Converter with 256-cycles in 65nm CMOS	XILINX	A modular 16nm Direct-RF TX/RX embedding 9GS/s DAC and 4.5GS/s ADC with 90dB isolation and sub-80ps channel alignment for monolithic integration in 5G base-station SoC	Seoul Nat'l Univ.	A Fully Integrated 700mA Event-Driven Digital Low-Dropout Regulator with Residue-Tracking Loop for Fine-Grained Power Management Unit
12:10 PM	Luncheon Talk The Hardware of Mind, from Turing to Today, Grady Booch, IBM Coral 2 - Mid Pacific Convention Center, 12:15 PM - 1:30 PM									
	T17: STT MRAM		T18: Process and Material Technologies 3		C22: Advanced Amplifiers and Analog Front-Ends		C23: Next Generation Sensors			
1:50 PM	Samsung	Embedded STT-MRAM in 28-nm FDSOI Logic Process for Industrial MCU/IoT Application	AIST	Significant Performance Enhancement of UTB GeOI pMOSFETs by Advanced Channel Formation Technologies	UC Berkeley	A 1mW -101dB THD+N Class-AB High-Fidelity Headphone Driver in 65nm CMOS	CEA-LETI	A 5500fps 85GOPS/W 3D stacked BSI vision chip based on parallel in-focal-plane acquisition and processing		
2:15 PM	Global-foundries	22-nm FD-SOI Embedded MRAM with Full Solder Reflow Compatibility and Enhanced Magnetic Immunity	imec	First demonstration of vertically-stacked Gate-All-Around highly strained Germanium nanowire p-FETs	Univ. of Michigan	A 2.2 NEF Neural-Recording Amplifier Using Discrete-Time Parametric Amplification	HKUST	A 2pJ/pixel/direction MIMO Processing based CMOS Image Sensor for Omnidirectional Local Binary Pattern Extraction and Edge Detection		
2:40 PM	Qualcomm	Low RA Magnetic Tunnel Junction Arrays in Conjunction with Low Switching Current and High Breakdown Voltage for STT-MRAM at 10 nm and Beyond	The Univ. of Tokyo	Hole mobility enhancement in extremely-thin-body strained GOI and SGOI pMOSFETs by improved Ge condensation method	KAIST	A 6.5µW 92.3dB-DR Biopotential-Recording Front-End with 360mVpp Linear Input Range	MIT	Room-Temperature Quantum Sensing in CMOS: On-Chip Detection of Electronic Spin States in Diamond Color Centers for Magnetometry		
3:05 PM	Samsung	Rare-Failure Oriented STT-MRAM Technology Optimization	NUS	GeSn p-FinFETs with Sub-10 nm Fin Width Realized on a 200 mm GeSnOI Substrate:Lowest SS of 63 mV/decade, Highest Gm,int of 900 µS/µm, and High-field µeff of 275 cm2/V·s	KU Leuven	A 0.6V 54dB SNR Analog Frontend with 0.18% THD for Low Power Sensory Applications in 65nm CMOS	Univ. of Michigan	A 179-lux Energy-Autonomous Fully-Encapsulated 17-mm³ Sensor Node with Initial Charge Delay Circuit for Battery Protection		
	T19: 3D Vertical and Stackable NVM		T20: CMOS Platform and Technology		C24: Machine Learning for Health and Neuro Inspired Processing		C25: Wireline Building Blocks			
3:45 PM	Seoul Nat'l Univ.	Space Program Scheme for 3-D NAND Flash Memory Specialized for the TLC Design	Samsung	Highly Manufacturable Low Power and High Performance 11LPP Platform Technology for Mobile and GPU Applications	Intel	A 4096-neuron 1M-synapse 3.8pJ/SOP Spiking Neural Network with On-chip STDP Learning and Sparse Weights in 10nm FinFET CMOS	Toshiba	A 50Gb/s 1.6pJ/b RX Data-Path with Quarter-Rate 3-tap Speculative DFE		
4:10 PM	imec	First demonstration of monocrystalline silicon macaroni channel for 3-D NAND memory devices	Globalfoundries	A 12nm FinFET Technology Featuring 2nd Generation FinFET for Low Power and High Performance Applications	Mediatek Inc.	A 0.76mm² 0.22nJ/Pixel DL-assisted 4K Video Encoder LSI for Quality-of-Experience over Smart-Phones	IBM	An Inverter-based Analog Front End for a 56 Gb/s PAM4 Wireline Transceiver in 16nm CMOS		
4:35 PM	Macronix	High Endurance Self-Heating OTS-PCM Pillar Cell for 3D Stackable Memory	Samsung	8LPP Logic Platform Technology for Cost-Effective High Volume Manufacturing	Nat'l Taiwan Univ.	A 1.9mW SVM Processor with On-chip Active Learning for Epileptic Seizure Control	Stanford Univ.	A 14 µm × 26 µm 20-Gb/s 3-mW CDR Circuit with High Jitter Tolerance		
5:00 PM	POSTECH	Te-based binary OTS selectors with excellent selectivity (>1E5), endurance (>1E8) and thermal stability (>450°C)	Qualcomm	High Performance Mobile SoC Productization with 2nd Generation 10nm FinFET Technology and Extension to 8nm Scaling	Nat'l Taiwan Univ.	A 12.6mW 573-2,901KS/s Reconfigurable Processor for Reconstruction of Compressively-Sensed Physiological Signals	UC Los Angeles	A 40Gb/s Optical NRZ Transmitter Based on Monolithic Microring Modulators in 45nm SOI CMOS		
5:25 PM	imec	Half-bias Ioff reduction down to nA range of thermally and electrically stable high-performance integrated OTS selector, obtained by Se enrichment and N-doping of thin GeSe layers	imec	Hybrid 14nm FinFET - Silicon Photonics Technology for Low-Power Tb/s/mm2 Optical I/O	Toshiba	PhaseMAC: A 14 TOPS/W 8bit GRO based Phase Domain MAC Circuit for In-Sensor-Computed Deep Learning Accelerators	UC Berkeley	A 10-bit 20-40 GS/s ADC with 37 dB SNDR at 40 GHz Input using First Order Sampling Bandwidth Calibration		

2018 Symposia on VLSI Technology and Circuits June 22 - Friday

Machine Learning Today and Tomorrow: Technology, Circuits and System View

Time	Tapa I	
8:00 AM	Tech	Opening Remarks
8:15 AM	Massachusetts Inst. of Tech	Hardware for Machine Learning: Design Considerations, Vivienne Sze
8:50 AM	Harvard University / Facebook	Machine Learning at Scale, David Brooks
9:30 AM		Joint Q&A with Speakers
10:10 AM	CEA-Tech	What You Need to Develop your own Deep Learning system: Tools, Databases, Hardware, Ethics, or Soon use Self-generating Systems?, Marc Duranton
10:45 AM	Stanford	Mixed-signal Techniques for Embedded Machine Learning Systems, Boris Murmann
11:20 AM		Joint Q&A with Speakers
11:40 AM		Lunch Panel, Barbara de Salvo, CEA-LETI, J. Deguchi, Toshiba Memory, N. Shanbhag, UIUC
1:40 PM	UIUC	The Deep In-Memory Architecture for Energy Efficient Machine Learning, Naresh Shanbhag
2:15 PM	CEA-LETI	Emerging Technologies for Memory-centric Computing, Elisa Vianello
2:50 PM		Joint Q&A with Speakers
3:30 PM	Preferred Networks	Emerging Applications: Machine Learning in Real World: Automobile, Robotics, and Life Science, Daisuke Okanohara
4:05 PM	Waseda University / AIST	Emerging Applications: Humanoid Robotics for Multiple Tasks and Communication, Tetsuya Ogata
4:40 PM		Joint Q&A with Speakers
5:00 PM		Close