2018 Symposium on VLSI Circuits Acceptance List

4 A Hybrid Dual-Path Step-Down Converter with 96.2% Peak Efficiency using a 250mΩ of Large-DCR Inductor, Yeunhee Huh, KAIST

9 A 0.2GHz to 4GHz Hybrid PLL (ADPLL/Charge-Pump-PLL) in 7nm FinFET CMOS Featuring 0.619ps Integrated Jitter and 0.6us Settling Time at 2.3mW, Tsung-Hsien Tsai, TSMC

10 A sub-0.85V, 6.4Gbp/s/pin TX-Interleaved Transceiver with Fast Wake-up Time using 2-Step Charging Control and VOH Calibration in 20nm DRAM Process, Jin-Hyeok Baek, Samsung Electronics

12 220mV-900mV 794/584/754 Gbps/W Reconfigurable GF(24)2 AES/SMS4/Camellia Symmetric-Key Cipher Accelerator in 14nm Tri-gate CMOS, Sudhir Satpathy, Intel Corporation

13 A 12-bit 31.1uW 1MS/s SAR ADC with On-Chip Input-Signal-Independent Calibration Achieving 100.4dB SFDR using 256fF Sampling Capacitance, Junhua Shen, Analog Devices

18 PhaseMAC: A 14 TOPS/W 8bit GRO based Phase Domain MAC Circuit for In-Sensor-Computed Deep Learning Accelerators, Kentaro Yoshioka, Toshiba

27 A 4096-neuron 1M-synapse 3.8pJ/SOP Spiking Neural Network with On-chip STDP Learning and Sparse Weights in 10nm FinFET CMOS, Gregory K. Chen, Intel Corporation

43 A 2.3-mW, 950-MHz, 8-bit Fully-Time-Based Subranging ADC Using Highly-Linear Dynamic VTC, Kenichi Ohhata, Kagoshima University

44 A 2.69uW Dual Quantization-based Capacitance-to-Digital Converter for Pressure, Humidity, and Acceleration Sensing in 0.18um CMOS, Sujin Park, KAIST

46 153 fsRMS-Integrated-Jitter and 114-Multiplication Factor PVT-Robust 22.8 GHz Ring-LC-Hybrid Injection-Locked Clock Multiplier, Seojin Choi, Ulsan National Institute of Science and Technology (UNIST)

48 A 117dB In-band CMRR 98.5dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing with an Electrically Floating Target, Hui Jiang, Delft University of Technology

49 A 95.3% Peak Efficiency, 135nA Quiescent Current Buck-Boost DC-DC Converter with Current-Slope-Based Mode Control, Danzhu Lu, Analog Device Inc.

51 A Digital Bang-Bang Phase-Locked Loop with Background Injection Timing Calibration and Automatic Loop Gain Control in 7nm FinFET CMOS, Ting-Kuei Kuan, TSMC

53 A 550uW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental Converter with 256-cycles in 65nm CMOS, Biao Wang, University of Macau

59 A 16-Gb/s 0-dB Power Back-off 16-QAM Transmitter at 28 GHz in 65-nm CMOSX, Xiangyu Meng, The Hong Kong University of Science and Technology

65 A Sub-Leakage pW-Power Hz-Range Relaxation Oscillator Operating with 0.3V-1.8V Unregulated Supply, Orazio Aiello, National University of Singapore

68 An Ultra-low Quiescent Current 250nA Low Dropout Regulator for No-load to 10mA Internet-of-Everything Applications, Ke-Horng Chen, ECE, NCTU

69 A Quasi-Digital Ultra-Fast Capacitor-less Low-Dropout Regulator Based on Comparator Control for x8 Current Spike of PCRAM systems, Sung-Won Choi, KAIST

73 A 5.5 GHz Background-Calibrated Subsampling Polar Transmitter with -41.3 dB EVM at 1024 QAM in 28nm CMOS, Nereo Markulic, imec and Vrije Universiteit Brussel

74 An All-Digital Unified Static/Dynamic Entropy Generator Featuring Self-Calibrating Hierarchical Von Neumann Extraction for Secure Privacy-Preserving Mutual Authentication in IoT Mote Platforms, Sudhir Satpathy, Intel Corporation

78 A 181nW 970µg/√Hz Accelerometer Analog Front-End Employing Feedforward Noise Reduction Technique, Ippei Akita, Toyohashi University of Technology

80 A 14 µm × 26 µm 20-Gb/s 3-mW CDR Circuit with High Jitter Tolerance, Long Kong, University of California, Los Angeles

83 An 8.2 µW 0.14 mm2 16-Channel CDMA-Like Period Modulation Capacitance-to-Digital Converter with Reduced Data Throughput, Yuxuan Luo, National University of Singapore

87 A 0.76mm² 0.22nJ/Pixel DL-assisted 4K Video Encoder LSI for Quality-of-Experience over Smart-Phones, Tsu-Ming Liu, Mediatek Inc.

96 A 10-bit 20-40 GS/s ADC with 37 dB SNDR at 40 GHz Input using First Order Sampling Bandwidth Calibration, Lukas Kull, IBM Research – Zurich, Rueschlikon, Switzerland

97 14nm FinFET 1.5Mb Embedded High-K Charge Trap Transistor One Time Programmable Memory Using Dynamic Adaptive Programming, Eric Hunt-Schroeder, GLOBALFOUNDRIES

98 A 0.029mm^2 17-fJ/Conv.-Step CT Delta-Sigma ADC With 2nd-Order Noise-Shaping SAR Quantizer, Jiaxin Liu, University of Electronic Science and Technology of China

100 A Mixed-Signal Binarized Convolutional-Neural-Network Accelerator Integrating Dense Weight Storage and Multiplication for Reduced Data Movement, Hossein Valavi, Princeton University

101 XNOR-SRAM: In-Memory Computing SRAM Macro for Binary/Ternary Deep Neural Networks, Zhewei Jiang, Columbia University

109 Artifact-Tolerant Opamp-less Delta-Modulated Bidirectional Neuro-Interface, M. Reza Pazhouhandeh, University of Toronto

113 A 290mV Ultra-Low Voltage One-Port SRAM Compiler Design Using a 12T Write Contention and Read Upset Free Bit-Cell in 7nm FinFET Technology, Mahmut Sinangil, TSMC

117 A 1.2V 68µW 98.2dB-DR Audio Continuous-Time Delta-Sigma Modulator, Changwook Lee, Yonsei University

121 STICKER: A 0.41-62.1 TOPS/W 8bit Neural Network Processor with Multi-Sparsity Compatible Convolution Arrays and Online Tuning Acceleration for Fully Connected Layers, Zhe Yuan, Tsinghua University, Beijing

125 A 179-lux Energy-Autonomous Fully-Encapsulated 17-mm³ Sensor Node with Initial Charge Delay Circuit for Battery Protection, Inhee Lee, University of Michigan

130 A 77dB SNDR 12.5MHz Bandwidth 0-1 MASH ΣΔ ADC Based on the Pipelined-SAR Structure, Yan Song, State-Key Laboratory of Analog and Mixed Signal VLSI, DECE/FST, University of Macau, Macau, China

132 A Sub-Harmonic Switching Digital Power Amplifier with Hybrid Class-G Operation for Enhancing Power Back-off Efficiency, Aoyang Zhang, University of Southern California

142 A 0.3pJ/bit 112Gb/s PAM4 1+0.5D TX-DFE Precoder and 8-tap FFE in 14nm CMOS, Thomas Toifl, IBM Research

143 A 2pJ/pixel/direction MIMO Processing based CMOS Image Sensor for Omnidirectional Local Binary Pattern Extraction and Edge Detection, Xiaopeng Zhong, Hong Kong University of Science and Technology

149 0.5V-VIN, 165-mA/mm2 Fully-Integrated Digital LDO based on Event-Driven Self-Triggering Control, Doyun Kim, Columbia University

151 A 1920 × 1080 25fps, 2.4TOPS/W Unified Optical Flow and Depth 6D Vision Processor for Energy-Efficient, Low Power Autonomous Navigation, Ziyun Li, University of Michigan, Ann Arbor

152 A 224 pW 260 ppm/°C Gate-Leakage-based Timer for Ultra-Low Power Sensor Nodes with Second-Order Temperature Dependency Cancellation, Jongyup Lim, University of Michigan

154 2.9TOPS/W Reconfigurable Dense/Sparse Matrix-Multiply Accelerator with Unified INT8/INT16/FP16 Datapath in 14nm Tri-gate CMOS, Mark Anders, Intel Corporation

155 A Fast Triple-Interferer Sensor (Detector and Digital Encoder) with In-Situ Reference Frequency Acquisition at 2.7-to-3.7GHz in 0.13um CMOS, Dongseok Shin, Virginia Tech, Intel Corp.

159 A CMOS Molecular Clock Probing 231.061-GHz Rotational Line of OCS with Sub-ppb Long-Term Stability and 66-mW DC Power, Cheng Wang, Massachuetts Institute of Technology

163 A 40Gb/s Optical NRZ Transmitter Based on Monolithic Microring Modulators in 45nm SOI CMOS, Sen Lin, University of California, Berkeley

164 Navion: A Fully Integrated Energy-Efficient Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones, Amr Suleiman, MIT

166 An All-Digital Unified Clock Frequency and Switched-Capacitor Voltage Regulator for Variation Tolerance in a Sub-Threshold ARM Cortex M0 Processor, Fahim ur Rahman, University of Washington

168 Sub-550mV SRAM Design in 22nm FinFET Low Power (22FFL) Technology with Self-Induced Collapse Write Assist, Daeyeon Kim, Intel Corporation

171 Fully integrated OOK-powered pad-less deep sub-wavelength-sized 5-GHz RFID with on-chip antenna using adiabatic logic in 0.18um CMOS, Yuta Toeda, Keio University

173 A 12.8 Gb/s Daisy Chain-Based Downlink I/F Employing Spectrally Compressed Multi-Band Multiplexing for High-Bandwidth and Large-Capacity Storage Systems, Yuta Tsubouchi, Toshiba Memory Corporation

179 Self-Regulated Wireless Power and Simultaneous 5 Mb/s Reverse Data over One Pair of Coils, Jiacheng Pan, UCLA

180 A 112-Gb/s PAM4 Transmitter in 16nm FinFET, KeeHian Tan, Xilinx Singapore

184 Terahertz RF Front-End Employing Even-Order Subharmonic MOS Symmetric Varactor Mixers in 65-nm CMOS for Hydration Measurements at 560 GHz, Qian Zhong, The University of Texas at Dallas

186 12-nm Fin-FET 3.0G-search/s 80-bit x 128-entry Dual-port Ternary CAM, Makoto Yabuuchi, Renesas Electronics Corporation

187 A Single-Stage, Single-Inductor, 6-Input 9-Output Multi-Modal Energy Harvesting Power Management IC for 100µW-120mW Battery-Powered IoT Edge Nodes, Suhwan Kim, Intel Corporation

189 A 1.25MS/s Two-Step Incremental ADC with 100dB DR and 110dB SFDR, Takato Katayama, Asahi Kasei Microdevices

197 A 1.9mW SVM Processor with On-chip Active Learning for Epileptic Seizure Control, Shuo-An Huang, National Taiwan University

202 A 12.6mW 573-2,901KS/s Reconfigurable Processor for Reconstruction of Compressively-Sensed Physiological Signals, Yu-Zhe Wang, National Taiwan University

207 A 114-aFrms-Resolution 46-nF/10-MΩ-Range Digital-Intensive Reconfigurable RC-to-Digital Converter with Parasitic-Insensitive Femto-Farad Baseline Sensing, Arup K. George, DGIST, Morse Micro

208 A Two-Tap NIR Lock-In Pixel CMOS Image Sensor with Background Light Cancelling Capability for Non-Contact Heart Rate Detection, Chen Cao, Shizuoka University

210 An 113dB-Link-Budget Bluetooth-5 SoC with an 8dBm 22%-Efficiency TX, Tong Wang, Toshiba Electronic Devices & Storage Corporation

213 Multipurpose, fully-integrated 128x128 event-driven MD-SiPM with 512 16-bit TDCs with 45 ps LSB and 20 ns gating, AUGUSTO CARIMATTO, TU Delft

216 A 0.04mm3 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement, Xiao Wu, University of Michigan, Ann Arbor

222 A Fully Integrated 700mA Event-Driven Digital Low-Dropout Regulator with Residue-Tracking Loop for Fine-Grained Power Management Unit, Jun-Eun Park, Seoul National University

226 A 50Gb/s 1.6pJ/b RX Data-Path with Quarter-Rate 3-tap Speculative DFE, Pier Andrea Francese, IBM Research-Zurich, Rueschlikon, Switzerland

230 Logic Process Compatible 40nm 16Mb, Embedded Perpendicular-MRAM with Hybrid-Resistance Reference, sub-µA Sensing Resolution, and 17.5nS Read Access Time, Yi-Chun Shih, TSMC

231 A Single-Topology Continuously-Scalable-Conversion-Ratio Fully Integrated Switched-Capacitor DC-DC Converter with 0-to-2.22V Output and 93% Peak-Efficiency, Nicolas Butzen, KU Leuven

233 A 7nm Double-Pumped 6R6W Register File for Machine Learning Memory, Hoan Nguyen, Qualcomm Technologies, Inc.

250 A 6.5µW 92.3dB-DR Biopotential-Recording Front-End with 360mVpp Linear Input Range, Jun-Suk Bang, KAIST, Samsung Electronics

251 A 64 Gb/s 1.5 pJ/bit PAM-4 Transmitter with 3-Tap FFE and Gm-Regulated Active-Feedback Driver in 28 nm CMOS, Haram Ju, Seoul National University

263 112Gb/s PAM4 Wireline Receiver using a 64-way Time-Interleaved SAR ADC in 16nm FinFET, James Hudner, Xilinx, Incorporated

266 A 5500fps 85GOPS/W 3D stacked BSI vision chip based on parallel in-focal-plane acquisition and processing, Laurent Millet, CEA, LETI, Minatec Campus

268 Energy Efficient Adiabatic FRAM with 0.99 pJ/bit Write for IoT Applications, Supreet Jeloka, University of Michigan, Ann Arbor, MI

270 AMASS PLL: An Active-Mixer-Adopted Sub-Sampling PLL Achieving an FOM of -255.5dB and a Reference Spur of -66.5dBc, Dhon-Gue Lee, UCSD

271 A 0.6V 54dB SNR Analog Frontend with 0.18% THD for Low Power Sensory Applications in 65nm CMOS, Komail Badami, MICAS - ESAT - KU Leuven

272 An Out-of-Order RISC-V Processor with Resilient Low-Voltage Operation in 28 nm CMOS, Pi-Feng Chiu, University of California, Berkeley

273 A 400GΩ input-impedance, 220mVpp linear-input-range, 2.8Vpp CM-interference-tolerant active electrode for non-contact capacitively coupled ECG acquisition, Mingyi Chen, imec,Leuven; Shanghai Jiaotong University

274 A modular 16nm Direct-RF TX/RX embedding 9GS/s DAC and 4.5GS/s ADC with 90dB isolation and sub-80ps channel alignment for monolithic integration in 5G base-station SoC, Christophe Erdmann, XILINX

275 A 28nm Integrated True Random Number Generator Harvesting Entropy from MRAM, Kaiyuan Yang, Rice University

279 A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET, Bruno Vaz, Xilinx, Dublin, Ireland

282 An Adaptive Body-Biasing SoC using in situ Slack Monitoring for Runtime Replica Calibration, Mehdi Saligane, University of Michigan

286 A 37.2nJ 64 (micro)s Start-Up 26/40MHz Crystal Oscillator with Negative Resistance Boosting Technique Using Reconfigurable Multi-Stage Amplifier, Masaya Miyahara, High Energy Accelerator Research Organization

292 An Automated SerDes Frontend Generator Verified with a 16nm Instance Achieving 15 Gb/s at 1.96 pJ/bit, Eric Chang, UC Berkeley

294 A Dual-Mode Configurable RF-to-Digital Receiver in 16nm FinFET, Amy Whitcombe, UC Berkeley

295 B-Face: 0.2 mW CNN-Based Face Recognition Processor with Face Alignment for Mobile User Identification, Sanghoon Kang, KAIST

297 A 92.8% Efficiency Adaptive-On/Off-Time Control 3-Level Buck Converter for Wide Conversion Ratio with Shared Charge Pump Intermediate Voltage Regulator, Yuki Karasawa, Shinshu University

300 A 0.8V 82.9µW In-ear BCI Controller System with 8.8 PEF EEG Instrumentational Amplifier and Wireless BAN Transceiver, Jaehyuk Lee, KAIST

302 A 2.2 NEF Neural-Recording Amplifier Using Discrete-Time Parametric Amplification, Taekwang Jang, University of Michigan

313 A Digital-Intensive 2-to-9.2 Gb/s/pin Memory Controller I/O with Fast-Response LDO in 10nm CMOS, Rajesh Inti, Intel Corporation

314 A Battery-Powered Opto-Electrophysiology Neural Interface with Artifact-Preventing Optical Pulse Shaping, Adam E. Mendrela, University of Michigan

316 An Inverter-based Analog Front End for a 56 Gb/s PAM4 Wireline Transceiver in 16nm CMOS, Kevin Zheng, Stanford University

317 A Scalable Multi-TeraOPS Deep Learning Processor Core for AI Training and Inference, Bruce Fleischer, IBM TJ Watson Research Center, Yorktown Heights, NY

321 A 141 uW, 2.46 pJ/Neuron Binarized Convolutional Neural Network based Self-learning Speech Recognition Processor in 28nm CMOS, Shouyi Yin, Tsinghua University, Beijing, China

322 Room-Temperature Quantum Sensing in CMOS: On-Chip Detection of Electronic Spin States in Diamond Color Centers for Magnetometry, Mohamed Ibrahim, Massachusetts Institute of Technology

323 An ultra-high energy-efficient reconfigurable processor for deep neural networks with binary/ternary weights in 28nm CMOS, Shouyi Yin, Tsinghua University, Beijing, China

327 A 1mW -101dB THD+N Class-AB High-Fidelity Headphone Driver in 65nm CMOS, Nandish Mehta, University of California, Berkeley

328 Half-and-Half Compare Content Addressable Memory with Charge-Sharing based Selective Match-Line Precharge Scheme, Woong Choi, Korea University

329 An All-Digital True-Random-Number Generator with Integrated De-correlation and Bias-Correction at 3.2-to-86 Mb/s, 2.58 pJ/bit in 65 nm CMOS, Rajesh Pamula, University of Washington

336 A >3GHz ERBW 1.1-GS/s 8-bit Two-Step SAR ADC with Recursive-Weight DAC, Haiwen Chen, University of Electronic Science and Technology of China

340 A 0.5-1.1V 10b Adaptive Bypassing SAR ADC Utilizing Oscillation Cycle Information of VCO-based Comparator, Zhaoming Ding, University of Electronic Science and Technology of China

347 A 0.5-28Gb/s Wireline Tranceiver with 15-Tap DFE and Fast-Locking Digital CDR in 7nm FinFET, Jay Im, Xilinx Inc.

355 A Wireless Implantable Ultrasound Array Receiver for Thermoacoustic Imaging, Ahmed Sawaby, Stanford University

362 A 252 × 144 SPAD pixel FLASH LiDAR with 1728 Dual-clock 48.8 ps TDCs, Integrated Histogramming and 14.9-to-1 Compression in 180nm CMOS Technology, Scott Lindner, EPFL and University of Zurich

373 A 220 m-Range Direct Time-of-Flight 688 × 384 CMOS Image Sensor with Sub-Photon Signal Extraction (SPSE) Pixels Using Vertical Avalanche Photo-Diodes and 6 kHz Light Pulse Counters, Shinzo Koyama, Panasonic Corp.