High performance $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs fabricated on 300 mm Si substrate


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Abstract

$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs are fabricated on 300 mm Si substrate. High device performance with good uniformity across the wafer are demonstrated (SS=78 mV/dec., $I_{on}/I_{off}=10^5$, DIBL=48 mV/V, $g_m=1510 \mu S/\mu m$, and $I_{on}=301 \mu A/\mu m$ at $V_{ds}=0.5V$ with $L_d=120$ nm device). The extrinsic field effect mobility of 1731 cm$^2$/V-s with EOT=0.9nm is extracted by split-CV. Devices fabricated on 300mm Si have shown similar performances in SS and $I_{on}$ when benchmarked with device fabricated on lattice-matched InP substrate. In addition, an $I_{on}$ of 44.1 $\mu A$/per fin is observed on the fin-height of 70 nm and the fin-width of 25nm, which is among the highest values reported for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs to the best of our knowledge.

Introduction

High electron mobility III-Vs semiconductors are promising for high-performance and low-power logic applications beyond Si channel. Hetero-epitaxial of high quality III-V on large scale Si platform and reducing the trap density in HK/III-V interface are critical challenges for fabricating high performance devices. Besides, in order to increase transistor density and improve electrostatic control of the channel, 3D architecture such as fins and nanowire are becoming essential in future applications. In this work, high quality $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel is epitaxially grown on 300 mm Si substrate. The fin structures are further fabricated using the combinations of dry and wet etching processes. The transfer/output characteristics, $L_g$ scaling properties, and carrier transport of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFET at various fin-width are demonstrated.

Device Fabrication

The process flow of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFET devices is shown in Fig. 1. The InGaAs channel is directly grown on 300 mm Si(100) substrate via a metamorphic III-V buffer by MOCVD [1]. The fin is fabricated by dry and wet etching of InGaAs channel. Fig.2 shows the FinFET with fin height (FH) of 45 nm and fin width (FW) of ~15 nm. Those characteristics indicate a well-controlled fin-etching process. After dummy gate formation, the heavily doped InGaAs is epitaxially grown on the source/drain (S/D) regions by MOCVD to wrap around the fin. The dummy gate is then removed for gate stack deposition. The S/D contact metal and the top metal are then patterned and deposited on the wafer.

Results and Discussion

The transfer characteristics of InGaAs planar ultra-thin body (UTB, channel thickness=10nm) and Fin- (FH=45nm) FET with EOT=0.9nm and $L_g=120$nm at $V_{ds}=0.5V$ are compared. The subthreshold swing (SS), drain induced barrier lowering (DIBL), peak transconductance ($g_m$), and drain current ($I_{on}$) as function of FW at $V_{ds}=0.5$ V are shown in Fig. 3. By narrowing the FW from 50 to 20 nm, the gate control can be significantly improved. Once the FW < 30nm, FinFET exhibits better electrostatic control of the channel than the UTB-FET.

The typical transfer characteristics of $L_g=1$ μm and 120 nm devices (FW=25,FH=45 nm) demonstrate similar subthreshold behavior (Fig. 4 (a) and (b)) indicating the excellent electrostatic control of the FinFET. SS of 78 and 84 mV/dec. are obtained at $V_{ds}=0.05$V and 0.5V for $L_g=120$ nm. DIBL and $I_{on}/I_{off}$ are ~48 mV/V and of ~10, respectively. The device with $L_g=120$ nm exhibits $g_m=1510 \mu S/\mu m$ and InGaAs $I_{on}=301 \mu A/\mu m$, $I_{on}/I_{off}=10^5$ when benchmarked with device fabricated on lattice-matched InP substrate. In addition, an $I_{on}$ of 44.1 $\mu A$/per fin is observed on the fin-height of 70 nm and the fin-width of 25nm, which is among the highest values reported for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs to the best of our knowledge.

Conclusions

High performance $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs have been fabricated on 300 mm Si substrate. Systematic study of materials properties, dimensions effect, and devices characteristics exhibits that III-V FinFETs on 300 mm Si is a promising candidate for next generation high-performance and low-power device applications.

References

**Process flow**
- III-V epi. on 300nm Si
- Fin formation
- N+ S/D
- HK deposition
- MG deposition
- S/D contact metal dep.
- Metallization

Fig. 1 Process flow for the InGaAs FinFET fabrication. Fin dimension was controlled by InGaAs epi-layer thickness and dry/wet etch conditions.

**Fig. 2** (a) Top view SEM and (b) cross-sectional TEM images of the InGaAs FinFET.

Fig. 3 (a) $I_{ds}$-$V_{gs}$ plot of UTB-FET ($T=10$nm) and FinFET at $V_{ds}=0.5V$. (b) SS, (c) DIBL, (d) $g_m$, and (e) $I_{ds}$ vs. FW for FinFET and UTB-FET.

**Fig. 4** Transfer characteristics of (a) $L_g=1\mu$m and (b) $L_g=120$ nm devices with FW=25 and FH=45nm.

**Fig. 5** $g_m$-$I_{gs}$ and $I_{ds}$-$V_{gs}$ of $L_g=120$ nm device at $V_{ds}=0.5$ and 0.05V, respectively.

**Fig. 6** $I_{ds}$-$V_{ds}$ of $L_g=120$ nm device.

**Fig. 7** $I_{on}$ characteristics with FW=45 and 70 nm of $L_g=120$ nm device.

**Fig. 8** (a) SS, (b) DIBL, (c) $g_m$, and (d) $I_{on}$ vs. various $L_g$.

**Fig. 9** The (a) $g_m$ and (b) SS map across 300mm wafer, respectively. The good uniformity of $L_g=120$ nm devices with high $g_m$(mean) of $1514 \mu S/\mu m$ (STD=1.9%) and low SS(mean) of $87 \text{mV/dec}$. (STD=3.3 %), respectively.

**Fig. 10** $R_{on}$ vs. $L_g$ of InGaAs FinFET.

**Fig. 11** TLM of metal-S/D junction.

**Fig. 12** Split C-V characteristics of planar-(T=50nm), UTB- (T=10nm), and Fin- (FW=25 nm) FET.

**Fig. 13** Extracted field effect mobility ($\mu_{FE}$) vs. $N_s$ for UTB-, and Fin- FET.

**Fig. 14** Benchmarking of $g_m$ (a) and $I_{on}$ (b,c) vs. SS of In$_{0.53}$Ga$_{0.47}$As Fin- and nanowire- FET at $V_{ds}=0.5V$ and $V_{gs}=0.5V$ with $I_d=100\text{nA/um}$. The $g_m$ and $I_{on}$ data are selected from device FW=20-50 nm.