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4 White Spots Reduction by Ultimate Proximity Metal Gettering at Carbon Complexes Formed underneath Contact Area in CMOS Image Sensors, Yamaguchi, *Renesas Electronics Corporation*

7 Demonstration of Record SiGe Transconductance and Short-Channel Current Drive in High-Ge-Content SiGe PMOS FinFETs with Improved Junction and Scaled EOT, Hashemi, *IBM*

15 Ultralow-Resistivity CMOS Contact Scheme with Pre-Contact Amorphization Plus Ti (Germano-)Silicidation, Yu, *Katholieke Universiteit Leuven & imec*

19 Demonstration of a sub-0.03 um2 High Density 6-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node, Wu, *Taiwan Semiconductor Manufacturing Company*

23 First demonstration and performance improvement of ferroelectric HfO2-based resistive switch with low operation current and intrinsic diode property, Fujii, *Toshiba Corporation*

25 Replacement High-K/Metal-Gate High-Ge-Content Strained SiGe FinFETs with High Hole Mobility and Excellent SS and Reliability at Aggressive EOT ~7Å and Scaled Dimensions Down to Sub-4nm Fin Widths, Hashemi, *IBM*

26 Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory, Choi, *Kookmin University*

31 Reliability study of perpendicular STT-MRAM as emerging embedded memory qualified for reflow soldering at 260oC, Shih, *TSMC*

33 Sub-3 ns pulse with sub-100 uA switching of 1x-2x nm perpendicular MTJ for high-performance embedded STT-MRAM towards sub-20 nm CMOS, Saida, *Corporate R&D Center, Toshiba Corporation*

34 Enabling monolithic 3D image sensor using large-area monolayer transition metal dichalcogenide and logic/memory hybrid 3D+IC, Yang, *National Nano Device Laboratories*

36 InGaAs Nanowire MOSFETs with ION = 555 µA/µm at IOFF = 100 nA/µm and VDD = 0.5 V, Zota, *Lund University*

38 Design / technology co-optimization of strain-induced layout effects in 14nm UTBB-FDSOI CMOS: enablement and assessment of continuous-RX designs, Berthelon, *STMicroelectronics*

39 Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates, Mertens, *imec*

40 A Novel Low Power Phase Change Memory Using Inter-Granular Switching, Lung, *Macronix*

43 Ultra low p-type SiGe contact resistance FinFETs with Ti silicide liner using cryogenic contact implantation amorphization and Solid-Phase Epitaxial Regrowth (SPER), Yang, *United Microelectronics Corp.(UMC)*

44 A ReRAM-based Physically Unclonable Function with Bit Error Rate < 0.5% after 10 years at 125˚C for 40nm Embedded Application, Yoshimoto, *Panasonic Semiconductor Solutions Corporation*

49 Deep Insight into Process-induced Pre-existing Traps and PBTI Stress-induced Trap Generations in High-k Gate Dielectrics through Systematic RTN Characterizations and Ab initio Calculations, Chen, *Toshiba Corporation*

51 Enabling High-Performance Heterogeneous TFET/CMOS Logic with Novel Circuits Using TFET Unidirectionality and Low-VDD Operation, Morris, *Components Research, Technology and Manufacturing Group, Intel Corporation*

52 A Monte Carlo Simulation Method to Predict Large-density NAND Product Memory Window from Small-array Test Element Group (TEG) Verified on a 3D NAND Flash Test Chip, Hsieh, *Macronix International Co., LTD.*

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57 Understanding charge traps for optimizing Si-passivated Ge nMOSFETs, Ren, *Liverpool john Moores University*

59 A New Variation Plot to Examine the Interfacial-dipole Induced Work-function Variation in Advanced High-k Metal-gate CMOS Devices, Hsieh, *National Chiao Tung University*

61 RTN-based defect tracking technique: experimentally probing the spatial and energy profile of the critical filament region and its correlation with HfO2 RRAM switching operation and failure mechanism, Chai, *Dept. of Electronics & Electr. Eng., Liverpool John Moores University, Liverpool L3 3AF, UK*

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67 Four-Layer 3D Vertical RRAM Integrated with FinFET as a Versatile Computing Unit for Brain-Inspired Cognitive Information Processing, Li, *Stanford University, USA*

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73 One-Transistor Ferroelectric Versatile Memory:Strained-Gate Engineering for Realizing Energy-Efficient Switching and Fast Negative-Capacitance Operation, Chiu, *National Chiao-Tung University*

74 Application of CVS and VRS method for correlation of logic CMOS wear out to discrete device degradation based on Ring Oscillator circuits, Kerber, *GLOBALFOUNDRIES*

76 Versatile TLC NAND Flash Memory Control to Reduce Read Disturb Errors by 85% and Extend Read Cycles by 6.7-times of Read-Hot and Cold Data for Cloud Data Centers, Kobayashi, *Department of Electrical, Electronic, and Communication Engineering, Graduate school of Science and Engineering*

80 A sub-ns three-terminal spin-orbit torque induced switching device, Fukami, *Tohoku University*

81 Fully CMOS Compatible 3D Vertical RRAM with Self-aligned Self-selective Cell Enabling Sub-5nm Scaling, Xu, *Institute of Microelectronics of the Chinese Academy of Sciences*

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91 Gate Stack Solutions in Gate-First FDSOI Technology to meet High Performance, Low Leakage, VT centering and Reliability Criteria, Weber, *CEA-LETI*

93 Low-Power, High-Performance S-NDR Oscillators for Stereo (3D) Vision using Directly-Coupled Oscillator Networks, Sharma, *Carnegie Mellon Universisty*

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94 Junctionless Gate-All-Around Lateral and Vertical Nanowire FETs with Simplified Processing for Advanced Logic and Analog/RF Applications and Scaled SRAM Cells, Veloso, *Imec*

95 Smart Solutions for Efficient Dual Strain Integration for Future FDSOI Generations, BONNEVIALLE, *CEA LETI,STMicroelectronics, CEMES-CNRS*

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110 Extremely Low Power C-Axis Aligned Crystalline In-Ga-Zn-O 60 nm Transistor Integrated with Industry 65 nm Si MOSFET for IoT Normally-Off CPU Application, wu, *United Microelectronics Corporation, Singapore*

111 Robust Cu Atom Switch with over-400oC thermally tolerant Polymer-solid Electrolyte (TT-PSE) for Nonvolatile Programmable Logic, Okamoto, *NEC Corporation*

113 Variability-aware TCAD Based Design-Technology Co-Optimization Platform for 7nm Node Nanowire and Beyond, Wang, *Peking Univerasity*

114 Direct three-dimensional observation of the conduction in poly-Si and In1-xGaxAs 3D NAND vertical channels, Celano, *imec*

119 Top-down InGaAs Nanowire and Fin Vertical FETs with Record Performance, Ramesh, *KU Leuven, ESAT, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium, IMEC, Kapeldreef 75, B-3001 Leuven, Belgium*

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132 Retention, disturb and variability improvements enabled by local chemical-potential tuning and controlled Hour-Glass filament shape in a novel W\WO3\Al2O3\Cu CBRAM, Goux, *imec*

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145 Monolayer MoS2 FETs with Sub-10 nm Channel Formed by Directed Self-Assembly, Nourbakhsh, *Massachusetts Institute of Technology*

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148 RTN and Low Frequency Noise on Ultra-scaled Near-ballistic Ge Nanowire nMOSFETs, Wu, *Purdue University, USA, Nanjing University, China, Zhejiang University, China*

152 Performance improvement of InxGa1-xAs Tunnel FETs with Quantum Well and EOT scaling, Ahn, *The university of Tokyo, JST CREST*

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159 Sub-2x10-9 Ω-cm2 N- and P-Contact Resistivity with Si:P and Ge:Ga Metastable Alloys for FinFET CMOS Technology, Niimi, *GLOBALFOUNDRIES Inc.*

165 FINFET Technology Featuring High Mobility SiGe Channel for 10nm and Beyond, Guo, *IBM*

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167 High Performance CMOS FDSOI Devices activated at Low Temperature, Pasini, *CEA-LETI, STMicroelectronics, IMPE-LAHC*

175 High aspect ratio InGaAs FinFETs with sub-20 nm fin width, Vardi, *MIT*

177 Ti and NiPt/Ti Liner Silicide Contacts for Advanced Technologie, ADUSUMILLI, *IBM Research, Albany, NY*

179 A Highly Scalable Poly-Si Junctionless FETs Featuring a Novel Multi-Stacking Hybrid P/N Layer and Vertical Gate with Very High Ion/Ioff for 3D Stacked ICs, Cheng, *National Tsing Hua University,National Chiao Tung University*

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183 Back-illuminated voltage-domain global shutter CMOS image sensor with 3.75µm pixels and dual in-pixel storage nodes, Stark, *University of Edinburgh, UK*

185 GDOT: A Graphene-Based Nanofunction for Dot-Product Computation, Wang, *Stanford University*

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211 High performance In0.53Ga0.47As FinFETs fabricated on 300 mm Si substrate, Huang, *TSMC*

212 Achieving Sub-ns switching of STT-MRAM for future embedded LLC applications through improvement of nucleation and propagation switching mechanisms, jan, *Headway technologies*

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C073 Novel Pixel Structure with Stacked Deep Photodiode to Achieve High NIR Sensitivity and High MTF, takahashi.hiroki@tpsemico.com, *TowerJazz*