## 2016 Symposia on VLSI Technology and Circuits June 14th - Tuesday

<table>
<thead>
<tr>
<th>Time</th>
<th>Tapa I</th>
<th>Tapa II</th>
<th>Tapa III</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:00 AM</td>
<td>Technology Panel Session - Tapa I</td>
<td>How Moore’s Law, Industry Consolidation, and System Trends are Shaping the Memory Roadmap?</td>
<td>Joint Technology/Circuits Panel Session - Tapa II</td>
</tr>
<tr>
<td>8:30 AM</td>
<td>InvenSense</td>
<td>The Age of Sensors – How MEMS sensors will enable the next wave of new products (Invited)</td>
<td></td>
</tr>
<tr>
<td>9:00 AM</td>
<td>Nissan</td>
<td>Intelligent mobility realized through VLSI (Invited)</td>
<td></td>
</tr>
</tbody>
</table>

### T2: Technology Highlights Session

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
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</thead>
<tbody>
<tr>
<td>10:30 AM</td>
<td>Samsung Elect. Si FinFET based 10nm Technology with Multi-VG Gate Stack for Low Power and High Performance Applications</td>
</tr>
<tr>
<td>10:30 AM</td>
<td>IBM</td>
</tr>
<tr>
<td>11:15 AM</td>
<td>TSMC Joint Technology / Circuits (green)</td>
</tr>
<tr>
<td>11:45 AM</td>
<td>Headway Tech.</td>
</tr>
</tbody>
</table>

### T3: System and Embedded Memory

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
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</thead>
<tbody>
<tr>
<td>1:00 PM</td>
<td>Micron</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>Toshiba Corp.</td>
</tr>
<tr>
<td>2:00 PM</td>
<td>Hitachi, Ltd.</td>
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</table>

### T4: Ge and SiGe Channel Devices

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
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</thead>
<tbody>
<tr>
<td>1:30 PM</td>
<td>Liverpool John Moores U.</td>
</tr>
<tr>
<td>1:50 PM</td>
<td>imec</td>
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<tr>
<td>2:20 PM</td>
<td>imec</td>
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<tr>
<td>2:45 PM</td>
<td>imec</td>
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### T5: Device Reliability

<table>
<thead>
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<th>Time</th>
<th>Topic</th>
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<tbody>
<tr>
<td>3:25 PM</td>
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<td>3:50 PM</td>
<td>imec</td>
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<tr>
<td>4:15 PM</td>
<td>imec</td>
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<tr>
<td>4:40 PM</td>
<td>imec</td>
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### T6: Novel 2D Materials and Devices

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<thead>
<tr>
<th>Time</th>
<th>Topic</th>
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<tbody>
<tr>
<td>3:25 PM</td>
<td>imec</td>
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<tr>
<td>3:50 PM</td>
<td>imec</td>
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<tr>
<td>4:15 PM</td>
<td>imec</td>
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<tr>
<td>4:40 PM</td>
<td>imec</td>
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### T7: Contact Resistance Innovations for Sub-10nm Scaling

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<th>Time</th>
<th>Topic</th>
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<tbody>
<tr>
<td>3:25 PM</td>
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<td>3:50 PM</td>
<td>imec</td>
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<tr>
<td>4:15 PM</td>
<td>imec</td>
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### T8: High Density Non Volatile Memory

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
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<tbody>
<tr>
<td>3:25 PM</td>
<td>imec</td>
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<tr>
<td>3:50 PM</td>
<td>imec</td>
</tr>
<tr>
<td>4:15 PM</td>
<td>imec</td>
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<tr>
<td>4:40 PM</td>
<td>imec</td>
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### Joint Technology/Circuits Reception

<table>
<thead>
<tr>
<th>Time</th>
<th>Tapa Conference Center, Palace Lounge</th>
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<tbody>
<tr>
<td>8:00 PM</td>
<td>Joint Technology/Circuits Reception</td>
</tr>
</tbody>
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**Color Code**
- **Technology (blue)**
- **Circuits (red)**
- **Joint Technology / Circuits (green)**

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**Technology Panel Session - Tapa I**

- **Technology Reliability and Welcome**
- **Welcome and Opening Remarks**

**Joint Technology/Circuits Session - Tapa II**

- **Technology Highlights Session**
- **System and Embedded Memory**
- **Ge and SiGe Channel Devices**
- **Device Reliability**

**Joint Technology/Circuits Panel Session - Tapa III**

- **More Moore, More than Moore, or Mo(o)re Slowly?**

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**Technology Plenary and Welcome**

- **10:30 AM - 11:00 AM**
  - 10:45 AM: Introduction to the Symposium (Tapa Conference Center)
  - 11:00 AM: Welcome and Opening Remarks (Tapa Conference Center)

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**Technology Highlights Session**

- **10:30 AM - 11:00 AM**
  - 10:45 AM: Introduction to the Symposium (Tapa Conference Center)
  - 11:00 AM: Technology Highlights Session (Tapa Conference Center)

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**System and Embedded Memory**

- **1:30 PM - 2:00 PM**
  - 1:45 PM: Introduction to the Symposium (Tapa Conference Center)
  - 2:00 PM: System and Embedded Memory (Tapa Conference Center)

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**Ge and SiGe Channel Devices**

- **2:30 PM - 3:00 PM**
  - 2:45 PM: Introduction to the Symposium (Tapa Conference Center)
  - 3:00 PM: Ge and SiGe Channel Devices (Tapa Conference Center)

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**Device Reliability**

- **3:30 PM - 4:00 PM**
  - 3:45 PM: Introduction to the Symposium (Tapa Conference Center)
  - 4:00 PM: Device Reliability (Tapa Conference Center)

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**More Moore, More than Moore, or Mo(o)re Slowly?**

- **4:30 PM - 5:00 PM**
  - 4:45 PM: Introduction to the Symposium (Tapa Conference Center)
  - 5:00 PM: More Moore, More than Moore, or Mo(o)re Slowly? (Tapa Conference Center)
<table>
<thead>
<tr>
<th>Time</th>
<th>Tapa I</th>
<th>Tapa II</th>
<th>Tapa III</th>
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<tbody>
<tr>
<td>8:00 AM</td>
<td>Google Inc.</td>
<td>Enabling Progress in Machine Learning</td>
<td>Instantaneous Power Management</td>
</tr>
<tr>
<td>9:30 AM</td>
<td>SONY</td>
<td>Accelerating the Sensing World through Imaging Evolution</td>
<td></td>
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</tbody>
</table>

### Tech Focus Sessions

#### 10:15 AM
- **TSMC**
  - **Title**: A 15.6 nm Dual-Port SRAM with Partial Suppressed Write Inhibit, Dummy Read Recovery and Negative Bit-line Circui
  - **Abstract**: Demonstration of a sub-0.5 um High Density 5-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node
  - **Institution**: Texas Inst.
  - **Speaker**: Smart Power Technologies

#### 10:40 AM
- **Renesas Elec. Corp.**
  - **Title**: A 0.05 μm2 FinFET Double Pumping 35W CMOS
  - **Abstract**: First Demonstration of InGaAs CMOS Inverters and Dense SRAM Arrays on Si Using
  - **Institution**: Renesas Electronics

#### 11:05 AM
- **NEC Corp.**
  - **Title**: A 2x Logic Density Programmable Logic Array using 60nm Switch Full Implemented with Logic Transistors at 40nm and beyond
  - **Abstract**: Replacement High-K/Metal-Gate High-Current Strained SiGe HFO2 with High Hole Mobility and Excellent SS and Reliability at
  - **Institution**: IMEC

### Biomedical SOCs

#### 13:30 PM
- **GLOBAL FOUNDRIES, INDIA**
  - **Title**: 180nm 128 Mbit Read Cycle Logic Embedded High-K Charge Trap Multi-Programmable Memory Scalable to 14nm Fin with no Added Process
  - **Abstract**: Zero-thick Multi Work Function Solutions for N7 bulk FinFETs
  - **Institution**: KAUST

### Low Power RF-Transceivers

#### 2:30 PM
- **U. of Texas at Austin**
  - **Title**: A Front-end ASIC with Receiver Sub-Array Transforming Integrated with a 32x32 PZT Matrix Transducer for 3D Transesophageal Imaging
  - **Abstract**: Broadband THz Spectroscopic Imaging based on a Fully Integrated 4×2 Digital-to-Impulse Radiating Array with a Full-Spectrum of
  - **Institution**: Macromix

### Voltage Regulator

#### 4:30 PM
- **IIT Madras**
  - **Title**: A 128-Channel Spike Sorting Processor Featuring 0.175 μW and 0.0033 mm2 per Channel
  - **Abstract**: Overcoming Scaling Barriers through Design Technology Co-optimization (Invited)
  - **Institution**: Liverpool John Moores

### Emerging Memory Technology (RRAM and PCM)

#### 8:00 AM
- **TSMC**
  - **Title**: A 50nm 5V 5W 50% Efficiency 3-Level Buck Converter with Real-Time Calibration and Wide Output Range for Fast DVS in 55nm CMOS
  - **Abstract**: Smart Solutions for Efficient Dual Stage Integration for Future FDSCII Generations
  - **Institution**: CEIA LETI

### Voltage Regulation

#### 2:55 PM
- **NSC, Taiwan**
  - **Title**: A 120 MHz Dual-Power SRAM with Partial Suppressed Write Inhibit, Dummy Read Recovery and Negative Bit-line Circuits for Low VMIN Applications
  - **Abstract**: Demonstration of a sub-0.05 um2 High Density 5-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node
  - **Institution**: SMART Power Technologies Enabling Power SOC and SIP

### Technology Circuits Joint Focus Session

#### 3:00 PM
- **Toshiba**
  - **Title**: A 16nm Dual-Port SRAM with Partial Suppressed Write Inhibit, Dummy Read Recovery and Negative Bit-line Circuits for Low VMIN Applications
  - **Abstract**: Demonstration of a sub-0.5 um High Density 5-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node
  - **Institution**: Panasonic Corp.

### Power Management and Energy Harvesting

#### 3:10 PM
- **NEC Corp.**
  - **Title**: A Fully-Adaptive Wideband 0.5-32.75Gb/s Data Recovery Transceiver using a 23-way Time-Interleaved FIP Feedback
  - **Abstract**: A 5Gb/s PAM4 Wireline Transceiver using a 23-way Time-Interleaved SARR ADC in 15nm FinFET

### Emerging Memory Technology (RRAM and PCM)

#### 3:15 PM
- **Toshiba**
  - **Title**: A 128-Channel Spike Sorting Processor Featuring 0.175 μW and 0.0033 mm2 per Channel
  - **Abstract**: Overcoming Scaling Barriers through Design Technology Co-optimization (Invited)
  - **Institution**: Liverpool John Moores

### Voltage Regulation

#### 5:30 PM
- **NEC Corp.**
  - **Title**: A 16nm Dual-Port SRAM with Partial Suppressed Write Inhibit, Dummy Read Recovery and Negative Bit-line Circuits for Low VMIN Applications
  - **Abstract**: Demonstration of a sub-0.05 um2 High Density 5-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node
  - **Institution**: SMART Power Technologies Enabling Power SOC and SIP

### Low Power RF-Transceivers

#### 5:30 PM
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### Voltage Regulation

#### 5:50 PM
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### Low Power RF-Transceivers

#### 6:00 PM
- **NEC Corp.**
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  - **Institution**: Liverpool John Moores

### Voltage Regulation

#### 6:15 PM
- **NEC Corp.**
  - **Title**: A 128-Channel Spike Sorting Processor Featuring 0.175 μW and 0.0033 mm2 per Channel
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  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers

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  - **Institution**: Liverpool John Moores

### Voltage Regulation

#### 6:45 PM
- **NEC Corp.**
  - **Title**: A 128-Channel Spike Sorting Processor Featuring 0.175 μW and 0.0033 mm2 per Channel
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  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers

#### 7:00 PM
- **NEC Corp.**
  - **Title**: A 128-Channel Spike Sorting Processor Featuring 0.175 μW and 0.0033 mm2 per Channel
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  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers

#### 7:15 PM
- **NEC Corp.**
  - **Title**: A 128-Channel Spike Sorting Processor Featuring 0.175 μW and 0.0033 mm2 per Channel
  - **Abstract**: Overcoming Scaling Barriers through Design Technology Co-optimization (Invited)
  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers

#### 7:30 PM
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  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers

#### 7:45 PM
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  - **Abstract**: Overcoming Scaling Barriers through Design Technology Co-optimization (Invited)
  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers

#### 8:00 PM
- **NEC Corp.**
  - **Title**: A 128-Channel Spike Sorting Processor Featuring 0.175 μW and 0.0033 mm2 per Channel
  - **Abstract**: Overcoming Scaling Barriers through Design Technology Co-optimization (Invited)
  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers

#### 8:15 PM
- **NEC Corp.**
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  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers

#### 8:30 PM
- **NEC Corp.**
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  - **Abstract**: Overcoming Scaling Barriers through Design Technology Co-optimization (Invited)
  - **Institution**: Liverpool John Moores

### Low Power RF-Transceivers
<table>
<thead>
<tr>
<th>Time</th>
<th>Tapa I</th>
<th>Tapa II</th>
<th>Tapa III</th>
<th>Honolulu</th>
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</thead>
<tbody>
<tr>
<td>8:05 AM</td>
<td>Intel Corp.</td>
<td>An FPGA On-chip Interconnect Trends, Challenges and Solutions: How to Keep</td>
<td>U. of Michigan, Ann Arbor</td>
<td>A 669W Discontinuous Switch Capacitor Energy Harvester for Self-Sustaining Sensor Applications</td>
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<tr>
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<td></td>
<td>Reconfigurable Interconnects Based on a Near-Threshold Voltage 1A-32 Microcomms in 14nm</td>
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<tr>
<td>8:55 AM</td>
<td>IMEC</td>
<td>Novel Nanowire MOSFETs with 12-15 nm Diameter</td>
<td>Stanford U.</td>
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<td>Statistical Limits of Contact Resistivity Due to Atomic Variation in Nanoscale Contacts</td>
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<tr>
<td>9:20 AM</td>
<td>Texas Inst.</td>
<td>Top-down InGaAs Nanowire and Fin Vertical FETs with Record Performance</td>
<td>Intel Corp.</td>
<td>A 144 MHz Wireless Power-Receiver-on-Chip</td>
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<tr>
<td></td>
<td></td>
<td>Random Telegraph Noise (RTN) in 14nm Logic Technology: High Volume</td>
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<td>IMEC</td>
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<td>Scalability of InGaAs Gate-All-Around FET integrated on 300nm Si platform</td>
<td>U. of Michigan, Ann Arbor</td>
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<td>Demonstration of channel with DVS/Time-division/delay</td>
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<td>10:25 AM</td>
<td>Texas Inst.</td>
<td>On-chip Interconnects, Challenges and Solutions: How to Keep</td>
<td>U.C Berkeley</td>
<td>A 669W CMOS Transceiver with Integrated Active Cancellation Supporting FDD from 1GHz</td>
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<td>Direct three-dimensional observation of the conduction in poly-Si and InGaAs 3D NAND vertical channels</td>
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<tr>
<td>10:50 AM</td>
<td>Panasonic Corp.</td>
<td>Seattle’s First 3D IC Design Technology Scalable in U.S. and Beyond 200k</td>
<td>UCLA</td>
<td>Digital PLL for Phase Noise Cancellation in Ring Oscillator-Based IQ Receivers</td>
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<td>Production-Worthy 3D Integration Technology using Bumped Interconnects and Ultra-Thinning Processes (Invited Paper)</td>
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<tr>
<td>11:15 AM</td>
<td>Analog Devices Inc.</td>
<td>First demonstration of a CMOS over CMOS 3D VLSI CoaxCable integration on 300mm</td>
<td>Pol. di Milano</td>
<td>A Chopping Switched-Capacitor RF Receiver with Integrated</td>
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<td>Novel CMOS-enabled 1T1R synapse capable of low-power STDP via burst</td>
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<tr>
<td>11:40 AM</td>
<td>STMicroelectronics</td>
<td>A Highly Scalable Poly-Si Junctionless FETs Featuring a Novel Multi-Stacking Hybrid PIN Layer and Vertical Gate with Very</td>
<td>Broadcom</td>
<td>A 180 mW Multistandard TV Tuner in 28 nm CMOS</td>
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<td>STMicroelectronics</td>
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<td>National Tsing Hua U.</td>
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<td>High-yield CMOS-512 × 576 CMOS Sensor for Food Safety Screening with</td>
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<td>Sensing to 0.01 pH Resolution</td>
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<td>Intel Corp.</td>
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<td>Random Telegraph Noise (RTN) in 14nm Logic Technology: High Volume</td>
<td>Intel Corp.</td>
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<td>Intel Corp.</td>
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<tr>
<td>1:30 PM</td>
<td>POSTECH</td>
<td>Gate Stack Solutions in Gate-First FDSOI Technology to meet High Performance, Low Leakage, VT Optimisation and Reliability Criteria</td>
<td>Carnegie Mellon U.</td>
<td>A 5.86mW 33mC 4th-Order Low-Pass Filter with +29dBm IP3 Using Self-Coupled Source Follower</td>
</tr>
<tr>
<td>1:55 PM</td>
<td>M. Semi. Lab</td>
<td>A New Variation Plot to Examine the Interface-Induced Work-Function Variation in Advanced High-K Metal-gate CMOS Devices</td>
<td>U. of Name Dame</td>
<td>3.6mW 35kHz AM Detector and Digitally-Controlled Tuner in a 1GHz TFFT for</td>
</tr>
<tr>
<td>2:45 PM</td>
<td>Intel Corp.</td>
<td>Complete Extraction of Defect Bands Responsible for Instabilities in n-channel and p-channel TFETs</td>
<td>National Tsing Hua U.</td>
<td>A Field-Programmable Mixed-Signal IC with Time-Domain Configurable Analog Blocks</td>
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<td>National Tsing Hua U.</td>
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<td>Intel Corp.</td>
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<td>Intel Corp.</td>
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<tr>
<td>3:25 PM</td>
<td>UC Davis</td>
<td>A 5.9 μJ/pOp 155 Billion Ops, to 1.78 Tillion Ops/sec 10mm 1000-Processor Array</td>
<td>Renesas Electronics Corp.</td>
<td>A 12-bit 1.6 Gbps Interlaced SAR ADC with Dual Reference Shifting and Interpolation</td>
</tr>
<tr>
<td>3:50 PM</td>
<td>STMicroelectronics</td>
<td>3D FDSOI Technology Sub-0.6V SRAM Vmem Assessment for Ultra Low Voltage Applications</td>
<td>National Nanotech Lab.</td>
<td>A 14.6mW 12b 800MHz 4×Time-Interleaved Pipelined SAR ADC achieving 60.8dB SNDR</td>
</tr>
<tr>
<td>4:15 PM</td>
<td>IBM Research Zurich</td>
<td>Performance improvement of InGaAs xAOS Tunnel FETs with Quantum Well and EOT scaling</td>
<td>National U. of Singapore</td>
<td>An Oscillator-Based Combined Comparator with Application in a 74.1dB SNDR, 20kHz/15dB</td>
</tr>
<tr>
<td>4:40 PM</td>
<td>Intel Corp.</td>
<td>Complementary III-V Heterojunction Lateral NW Tunnel FET Technology on Si</td>
<td>National Tsing Hua U.</td>
<td>A 5.43-Conversion step 11b 600Ks/s SAR ADC with Semi-Resting DAC</td>
</tr>
<tr>
<td>5:05 PM</td>
<td>Qualcomm</td>
<td>Monolithic Phase-transition FET Exhibiting Steep Switching Slope of 9mV/decade and 36% Enhanced ON Current</td>
<td>TowerJazz</td>
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<td>Novel Pixel Structure with Stacked Deep Photodiode to Achieve High Efficiency</td>
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<td>Back-illuminated voltage-domain global shatter CMOS image sensor with</td>
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<td>3.75mμA picoamps and dual-in-pixel storage nodes</td>
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**IEEE Solid-State Circuits Society Young Professionals and**
Grad Students Mentoring and Career coaching event
Hokkaido Hotels Nana - Thursday, June 16, 5:45 PM - 6:45 PM
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<th>Time</th>
<th>Topic II</th>
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<th>C24: Advanced Sensor Circuits</th>
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<td>8:05 AM</td>
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**Topic II: High-Speed Data Converters**

- **U. of Texas at Dallas**: A 23mW 24GS/s 6b Time-Interleaved Hybrid Two-Step ADC in 28nm CMOS
  - Kühn Inc.
  - Intel Corp.

- **MediaTek Inc.**: A 8.2-mW 10-b 1.6-GS/s 4x TI SAR ADC with Fast Reference Change Neutralization and Background Timing Slow Calibration in 10-nm CMOS
  - U. of Texas at Dallas
  - TI

- **Analog Devices**: A 14-bit 2.5GS/s and 5GS/s RF Sampling ADC with Background Calibration and Dither
  - Oracle Labs
  - Stanford U.

- **Texas Inst.**: A 14-bit 8.9GS/s RF DAC in 40m CMOS achieving >71dBc LTE ACPR at 2.9GHz
  - Huazhi Ltd.

**Topic III: VCOs and Optical Building Blocks**

- **KU Leuven**: A 0.3-2.6 TOPS/W Precision-Scalable Processor for Real-Time Large-Scale ConvNets
  - Stanford U.
  - Intel Corp.

- **Korea Inc.**: A 7.1-18.3GHz Compact Transformer-based VCO in 16nm FinFET
  - Sony

- **U. of Texas at Dallas**: 10GHz LO FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS
  - Toshiba U.

- **Oracle Labs**: A 10GHz, 32x12bit Micro-Ring Modulator Transmitter with Switched-Capacitor Pre-Emphasis and Monolithic Temperature Sensor in 65nm CMOS
  - Stanford U.

- **Intel Corp.**: A 50.6-Gb/s 7.8-mW/Gb/s –7.4-dBm Sensitivity Optical Receiver based on 0.18-um SiGe BiCMOS Technology
  - Intel Corp.

**Topic IV: Advanced Architecture and Processors**

- **Intel Corp.**: A 28nm CMOS Ultra-Compact Thermal Sensor in Current-Mode Technique

**IEEE Solid-State Circuits Society Luncheon**

- **Intel Corp.**: An 8.3piexl 480ps Global-Shutter CMOS Image Sensor with Gain-Adaptive Column ADCs and 2-1 Stacked Device Structure

- **Toboku U.**: A Dead-time Free Global Shutter CMOS Image Sensor with 15-pixel LDIC and ADC using Paul-wise Connections

- **Stanford U.**: A Dead-time Free Global Shutter CMOS Image Sensor with Partial Settling Readout Architecture

- **30th Symposium on VLSI Circuits**
  - **12:15 PM - 1:30 PM, Topic Conference Center, Honolulu Suite**

**C22: Clock and Frequency Synthesis**

- **KU Leuven**: A Inductor-less Fractional-N Injection-Locked PLL with a Spur-and-Phase-Noise Filtering Technique
  - Intel Corp.

- **U. of Michigan**: A Compact 446 Gbps/W AES accelerator for Mobile SoC and IoT in 40nm CMOS
  - RIKEN

- **Intel Corp.**: A 450mV Timing-Margin-Free Waveform Sorter based on a Standard 6T SRAM Array

- **Aarhus U.**: A Wearable Ear-EEG Recording System Based on Dry-Contact Active Electrodes

- **Tokyo Inst. of Tech.**: An 8.865-GHz -244dB-FOM High-Frequency Piezoelectric Resonator-Based Cascaded Fractional-N PLL with Sub-psy/Order Channel Adjusting Technique

- **U. of Michigan**: A Machine-learning Classifier Implemented in a Standard 8T SRAM Array

- **Usan Natl Inst. of Science and Tech.**: A PVT-Robust –59-dBC Reference Spur and 450-fdBMS Jitter Injection-Locked Clock Multiplier Using a Voltage-Dependent Period-Calibrating Loop

- **Princeton U.**: A Machine-learning Classifier Implemented in a Standard 8T SRAM Array

- **Columbia U.**: A 400mV Timing-Margin-Free Waveform Sorter based on Body Swapping Error Correction

**C23: Hardware Security and Application Specific Digital Design**

- **Caltech**: A 16-Channel 1.1mm2 Implantable Security Control SoC with Sub-μW/Channel Consumption and Closed-Loop Stimulation in 0.18μm CMOS

- **RIKEN**: A Macromodel Array with 8.640 Electrodes Enabling Simultaneous Full-frame Readout at 6.5 kHz and 112-Channel Switch-Matrix Readout at 20 kHz

- **Aarhus U.**: A Wearable Ear-EEG Recording System Based on Dry-Contact Active Electrodes