

2016 Circuits Symposium Accepted Papers

- 8** Digital PLL for Phase Noise Cancellation in Ring Oscillator-Based I/Q Receivers, Chen, *University of California, Los Angeles*
- 9** A Microcontroller with 96% Power-Conversion Efficiency using Stacked Voltage Domains, Blutman, *NXP Semiconductors*
- 11** A Bluetooth Low-Energy (BLE) Transceiver with TX/RX Switchable On-Chip Matching Network, 2.75mW High-IF Discrete-Time Receiver, and 3.6mW All-Digital Transmitter, Kuo, *TSMC*
- 13** A 8.2-mW 10-b 1.6-GS/s 4× TI SAR ADC with Fast Reference Charge Neutralization and Background Timing-Skew Calibration in 16-nm CMOS, Lin, *MediaTek Inc.*
- 14** An Energy Harvesting Wireless Sensor Node for IoT Systems Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14nm Tri-Gate CMOS, Paul, *Intel Corporation*
- 17** A 35μW 96.8dB SNDR 1 kHz BW Multi-Step Incremental ADC Using Multi-Slope Extended Counting with a Single Integrator, Zhang, *Oregon State University*
- 19** SleepTalker: a 28nm FDSOI ULV 802.15.4a IR-UWB Transmitter SoC achieving 14pJ/bit at 27Mb/s with Adaptive-FBB-based Channel Selection and Programmable Pulse Shape, de Streef, *ICTEAM Institute, Université catholique de Louvain, Louvain-la-Neuve, Belgium*
- 27** A 0.3-2.6 TOPS/W Precision-Scalable Processor for Real-Time Large-Scale ConvNets, Moons, *KU Leuven*
- 28** A 350mV-900mV 2.1GHz 0.011mm² Regular Expression Matching Accelerator with Aging-Tolerant Low-VMIN Circuits in 14nm Tri-Gate CMOS, Agarwal, *Intel Corporation*
- 31** A 14-bit 2.5GS/s and 5GS/s RF Sampling ADC with Background Calibration and Dither, Ali, *Analog Devices*
- 34** A Wireless Power Transfer System with Enhanced Response and Efficiency by Fully-Integrated Fast-Tracking Wireless Constant-Idle-Time Control for Implants, Huang, *Keio University*
- 36** A Field-Programmable Mixed-Signal IC with Time-Domain Configurable Analog Blocks, Choi, *Seoul National University*
- 39** A 0.58mm² 2.76Gb/s 79.8pJ/b 256-QAM Massive MIMO Message-Passing Detector, Tang, *University of Michigan*
- 41** A Transformer-based Digital Isolator With 20kVpk Surge Capability and > 200kV/μs Common Mode Transient Immunity, Yun, *Analog Devices Inc*
- 47** A PVT-Robust -59-dBc Reference Spur and 450-fsRMS Jitter Injection-Locked Clock Multiplier Using a Voltage-Domain Period-Calibrating Loop, Lee, *Ulsan National Institute of Science and Technology*
- 49** A 58.6mW Real-Time Programmable Object Detector with Multi-Scale Multi-Object Support Using Deformable Parts Model on 1920x1080 Video at 30fps, Suleiman, *MIT*
- 50** A 16-Channel 1.1mm² Implantable Seizure Control SoC with Sub-μW/Channel Consumption and Closed-Loop Stimulation in 0.18μm CMOS, Shoaran, *Caltech*
- 51** 250mV-950mV 1.1Tbps/W Double Affine Mapped Sbox based Composite-Field SMS4 Encrypt/Decrypt Accelerator in 14nm Tri-gate CMOS, Satpathy, *Intel Corporation*

2016 Circuits Symposium Accepted Papers

- 56** A Microelectrode Array with 8,640 Electrodes Enabling Simultaneous Full-frame Readout at 6.5 kfps and 112-Channel Switch-Matrix Readout at 20 kS/s, Yuan, *RIKEN, Japan*
- 60** A 50.6-Gb/s 7.8-mW/Gb/s -7.4-dBm Sensitivity Optical Receiver based on 0.18-um SiGe BiCMOS Technology, Takemoto, *Hitachi Ltd.*
- 62** A 4fJ/bit Delay-Hardened Physically Unclonable Function Circuit with Selective Bit Destabilization in 14nm Tri-gate CMOS, Mathew, *Intel Corporation*
- 63** A 220pJ/Pixel/Frame CMOS Image Sensor with Partial Settling Readout Architecture, Ji, *Stanford University*
- 67** A 13.3mW 60MHz Bandwidth, 76dB DR 6GS/s CTDSM with Time Interleaved FIR Feedback, Jain, *IIT Madras, India*
- 69** A 128-Channel Spike Sorting Processor Featuring 0.175 μ W and 0.0033 mm² per Channel in 65-nm CMOS, Zeinolabedin, *Nanyang Technological University, Singapore*
- 74** A 0.034mm² , 725fs RMS Jitter, 1.8%/V Frequency-Pushing, 10.8-19.3GHz Transformer-Based Fractional-N All-Digital PLL in 10nm FinFET CMOS, Li, *TSMC, Hsinchu, Taiwan*
- 77** A 2.4GHz Ternary Sequence Spread Spectrum OOK Transceiver with Harmonic Spur Suppression and Dual-Mode Detection Architecture for ULP Wearable Devices, Kim, *KAIST*
- 81** A Chopping Switched-Capacitor RF Receiver with Integrated Blocker Detection, +31dBm OB-IIP3, and +15dBm OB-B1dB, Xu, *Columbia University*
- 88** A 1.40mm² 141mW 898GOPS Sparse Neuromorphic Processor in 40nm CMOS, Knag, *University of Michigan*
- 95** An 8.3M-pixel 480fps Global-Shutter CMOS Image Sensor with Gain-Adaptive Column ADCs and 2-on-1 Stacked Device Structure, Oike, *Sony*
- 96** 3.5mW 1MHz AM Detector and Digitally-Controlled Tuner in a-IGZO TFT for Wireless Communications in a Fully Integrated Flexible System for Audio Bag, Meister, *Technische Universität Dresden*
- 97** A 50MHz 5V 3W 90% Efficiency 3-Level Buck Converter with Real-Time Calibration and Wide Output Range for Fast-DVS in 65nm CMOS, Liu, *Hong Kong University of Science and Technology*
- 100** 80Kb 10ns Read Cycle Logic Embedded High-K Charge Trap Multi-Time-Programmable Memory Scalable to 14nm FIN with no Added Process Complexity, Viraraghavan, *GLOBALFOUNDRIES INDIA*
- 102** A 35fJ/Step Differential Successive Approximation Capacitive Sensor Readout Circuit with Quasi-Dynamic Operation, Omran, *King Abdullah University of Science and Technology (KAUST)*
- 105** A 65nm CMOS Transceiver with Integrated Active Cancellation Supporting FDD from 1GHz to 1.8GHz at +12.6dBm TX Power Leakage, Ramakrishnan, *UC Berkeley*
- 108** A 125 mW 8.5-11.5 Gb/s Serial Link Transceiver with a Dual Path 6-bit ADC/5-tap DFE Receiver and a 4-tap FFE Transmitter in 28 nm CMOS, Raghavan, *Broadcom Corp*
- 112** A 12-bit 1.6 GS/s Interleaved SAR ADC with Dual Reference Shifting and Interpolation Achieving 17.8 fJ/conv-step in 65nm CMOS, Nam, *University of Southern California*
- 114** A 18.5-fJ/step VCO-Based 0-1 MASH Delta-Sigma ADC with Digital Background Calibration, Sanyal, *The University of Texas at Austin*

2016 Circuits Symposium Accepted Papers

- 120** A 16Gb/s 14.7mW Tri-Band Cognitive Serial Link Transmitter with Forwarded Clock to Enable PAM-16/256-QAM and Channel Response Detection in 28 nm CMOS, Du, *University of California, Los Angeles*
- 122** 95% Light-load Efficiency Single-Inductor Dual-Output DC-DC Buck Converter with Synthesized Waveform Control Technique for USB Type-C, Yang, *ECE, National Chiao Tung University*
- 123** A 16nm Dual-Port SRAM with Partial Suppressed Word-line, Dummy Read Recovery and Negative Bit-line Circuitries for Low VMIN Applications, Chen, *TSMC*
- 124** A Low-EMI Four-Bit Four-Wire Single-Ended DRAM Interface by Using a Three-Level Balanced Coding Scheme, Yi, *POSTECH*
- 125** A $\pm 36\text{A}$ Integrated Current-Sensing System with 0.3% Gain Error and $400\mu\text{A}$ Offset from -55°C to $+85^\circ\text{C}$, Heidary Shalmany, *Delft University of Technology*
- 128** A 14.6mW 12b 800MS/s 4×Time-Interleaved Pipelined SAR ADC achieving 60.8dB SNDR with Nyquist input and sampling timing skew of 60fsrms without calibration, Lien, *MediaTek Inc.*
- 134** A 190GFLOPS/W DSP for Energy-Efficient Sparse-BLAS in Embedded IoT, Dorrance, *University of California, Los Angeles*
- 136** A 28nm CMOS Ultra-Compact Thermal Sensor in Current-Mode Technique, Eberlein, *Intel Germany*
- 138** A 114-pW PMOS-Only, Trim-Free Voltage Reference with 0.26% within-Wafer Inaccuracy for nW Systems, Dong, *University of Michigan, Ann Arbor*
- 139** A 450mV Timing-Margin-Free Waveform Sorter based on Body Swapping Error Correction, Kim, *Columbia University*
- 141** A 2.4-GHz 6.4-mW Fractional-N Inductorless RF Synthesizer, Kong, *University of California, Los Angeles*
- 145** A Multiple-String Hybrid LED Driver with 97% Power Efficiency and 0.996 Power Factor, Li, *The Hong Kong University of Science and Technology*
- 149** A BJT-based Temperature-to-Digital Converter with $\pm 60\text{mK}$ (3σ) Inaccuracy from -70°C to 125°C in 160nm CMOS, Yousefzadeh, *Delft University of Technology*
- 150** A Sine-Reference Band (SRB)-Controlled Average Current Technique for a Phase-Cut Dimmable AC-DC Buck LED Driver without an Electrolytic Capacitor, Shin, *KAIST, Daejeon, Korea*
- 157** A 0.44fJ/conversion-step 11b 600KS/s SAR ADC with Semi-Resting DAC, Hsieh, *National Tsing Hua University*
- 160** An Oscillator Collapse-Based Comparator with Application in a 74.1dB SNDR, 20kS/s 15b SAR ADC, Shim, *Korea University*
- 165** A 10Gb/s, 342fJ/bit Micro-Ring Modulator Transmitter with Switched-Capacitor Pre-Emphasis and Monolithic Temperature Sensor in 65nm CMOS, Saeedi, *Oracle Labs, Redwood Shores, CA*
- 167** A 56Gb/s PAM4 Wireline Transceiver using a 32-way Time-Interleaved SAR ADC in 16nm FinFET, Frans, *Xilinx Inc*
- 168** A Fully Integrated 144 MHz Wireless-Power-Receiver-on-Chip with an Adaptive Buck-Boost Regulating Rectifier and Low-Loss H-Tree Signal Distribution, Kim, *University of California, San Diego*

2016 Circuits Symposium Accepted Papers

- 182** An 18 μ W Spur Canceled Clock Generator for Recovering Receiver Sensitivity in Wireless SoCs, Ogasawara, *Toshiba Corporation*
- 185** A Wearable Ear-EEG Recording System Based on Dry-Contact Active Electrodes, Zhou, *Department of Engineering, Aarhus University*
- 190** A 97.99 dB SNDR, 2 kHz BW, 37.1 μ W Noise-Shaping SAR ADC with Dynamic Element Matching and Modulation Dither Effect, Obata, *Panasonic Corporation*
- 192** A 7-to-18.3GHz Compact Transformer based VCO in 16nm FinFET, Raj, *Xilinx Inc.*
- 196** A Machine-learning Classifier Implemented in a Standard 6T SRAM Array, Zhang, *Princeton University*
- 200** A Compact 446 Gbps/W AES accelerator for Mobile SoC and IoT in 40nm, Zhang, *University of Michigan*
- 205** A 2.048 Mb/s Full-Duplex Free-Space Optical Transceiver IC for a Real-Time In Vivo Neurofeedback Mouse Experiment Under Social Interaction, Hwang, *KAIST*
- 206** A 32 Gb/s Rx Only Equalization Transceiver with 1-tap Speculative FIR and 2-tap Direct IIR DFE, Hwang, *Korea University*
- 207** A 0.6mW 31MHz 4th-Order Low-Pass Filter with +29dBm IIP3 Using Self-Coupled Source Follower Based Biquads in 0.18 μ m CMOS, Xu, *Oregon State University*
- 209** A 35 mW 10 Gb/s ADC-DSP less Direct Digital Sequence Detector and Equalizer in 65nm CMOS, Hossain, *University of Alberta*
- 215** Embedded Memory and ARM Cortex-M0 Core Using 60 nm C-Axis Aligned Crystalline Indium–Gallium–Zinc Oxide FET Integrated with 65 nm Si CMOS, Onuki, *Semiconductor Energy Laboratory Co., Ltd.*
- 216** An 8.865-GHz -244dB-FOM High-Frequency Piezoelectric Resonator-Based Cascaded Fractional-N PLL with Sub-ppb-Order Channel Adjusting Technique, Ikeda, *Tokyo Institute of Technology*
- 228** An Inductor-less Fractional-N Injection-Locked PLL with a Spur-and-Phase-Noise Filtering Technique, Li, *The Hong Kong University of Science and Technology*
- 232** A 28.3 Gb/s 7.3 pJ/bit 35 dB Backplane Transceiver with Eye Sampling Phase Adaptation in 28 nm CMOS, Miyaoka, *Socionext Inc.*
- 233** A 0.23 micro-g Bias Instability and 1.6 micro-g/rt(Hz) Resolution Silicon Oscillating Accelerometer with Build-in Sigma-Delta Frequency-to-Digital Converter, zhao, *Nanjing University of Science and Technology*
- 242** A Dead-time Free Global Shutter CMOS Image Sensor with in-pixel LOFIC and ADC using Pixel-wise Direct Connections, Sugo, *Tohoku Univ.*
- 247** A Reconfigurable SIMO System with 10-Output Dual-Bus DC-DC Converter using the Load Balancing Function in Group Allocator for Diversified Load Condition, Shin, *KAIST*
- 261** 1.74- μ W/ch, 95.3%-Accurate Spike-Sorting Hardware based on Bayesian Decision, Jiang, *Columbia University*
- 262** A 2x Logic Density Programmable Logic Array using Atom Switch Fully Implemented with Logic Transistors at 40nm-node and beyond, Tsuji, *NEC Corporation*

2016 Circuits Symposium Accepted Papers

- 263** A 9.84–73.2 nJ, 0.048 mm² Time-Domain Impedance Sensor that Provides Values of Resistance and Capacitance, Hong, *Nanyang Technological University, Singapore, 2Institute of Microelectronics, A*STAR, Singapore.*
- 268** A 14-bit 8.9GS/s RF DAC in 40nm CMOS achieving >71dBc LTE ACPR at 2.9GHz, Ravinuthula, *Texas Instruments Inc*
- 273** A 180 mW Multistandard TV Tuner in 28 nm CMOS, Xiao, *Broadcom*
- 277** A Fully-Adaptive Wideband 0.5-32.75Gb/s FPGA Transceiver in 16nm FinFET CMOS Technology, Upadhyaya, *Xilinx*
- 278** Adaptive Clocking with Dynamic Power Gating for Energy Efficiency Improvement in a 22nm Graphics Execution Core under Fast Voltage Droop, Cho, *Intel Corp.*
- 286** A 260μW Infrared Gesture Recognition System-on-Chip for Smart Devices, Oh, *University of Michigan*
- 288** -197dBc/Hz FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS, Jha, *The University of Texas, Dallas*
- 291** An High-Density CMOS Multi-Modality Joint Sensor/Stimulator Array with 1024 Pixels for Holistic Real-Time Cellular Characterization, Park, *Georgia Institute of Technology*
- 297** A 0.9um² 1T1R Bit Cell in 14nm SoC Process for Metal-Fuse OTP Array with Hierarchical Bitline, Bit Level Redundancy, and Power Gating, Chen, *Intel Corporation*
- 302** Multi-modal Smart Bio-sensing SoC Platform with >80dB SNR 35μA PPG RX Chain, Sharma, *Texas Instruments Inc.*
- 313** A 16-channel Noise-Shaping Machine Learning Analog-Digital Interface, Buhler, *University of Michigan, Ann Arbor, MI*
- 314** A 380pW Dual Mode Optical Wake-up Receiver with Ambient Noise Cancellation, Lim, *University of Michigan*
- 317** A 66pW Discontinuous Switch-Capacitor Energy Harvester for Self-Sustaining Sensor Applications, Wu, *University of Michigan, Ann Arbor*
- 319** A 0.003 mm² 5.2 mW/tap 20 GBd Inductor-less 5-Tap Analog RX-FFE, Boesch, *Stanford University*
- 327** A 23mW 24GS/s 6b Time-Interleaved Hybrid Two-Step ADC in 28nm CMOS, Xu, *University of Texas at Dallas*
- 329** 200-280GHz CMOS RF Front-End of Transmitter for Rotational Spectroscopy, Sharma, *University of Texas at Dallas*
- 332** A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography, Chen, *Electronic Instrumentation Lab., Delft University of Technology, Delft, The Netherlands*
- 337** A 6.05-Mb/mm² 16-nm FinFET Double Pumping 1W1R 2-port SRAM with 313 ps Read Access Time, Yabuuchi, *Renesas Electronics Corp.*
- 339** A 400mV Active VMIN, 200mV Retention VMIN, 2.8 GHz 64Kb SRAM with a 0.09 um² 6T bitcell in a 16nm FinFET CMOS Process, Bhavnagarwala, *ARM Research*

2016 Circuits Symposium Accepted Papers

- 342** A Fast, Flexible, Positive and Negative Adaptive Body-Bias Generator in 28nm FDSOI, Blagojević, *STMicroelectronics, Crolles; Dept. of EECS, University of California, Berkeley; Institut Supérieur d'Électronique de Paris*
- 350** A 5.8 pJ/Op 115 Billion Ops/sec, to 1.78 Trillion Ops/sec 32nm 1000-Processor Array, Bohnenstiehl, *University of California, Davis*
- 388** Broadband THz Spectroscopic Imaging based on a Fully Integrated 4×2 Digital-to-Impulse Radiating Array with a Full-Spectrum of 0.03-1.03THz in Silicon, Assefzadeh, *Rice University*