Inflections in VLSI Technologies – Cloud and Beyond

Organizers: Chorng-Ping Chang, Applied Materials
Shinya Yamakawa, Sony Corporation

8:30 a.m. - Brief outline - Chorng-Ping Chang

Cloud Computing

8:35 a.m. The Future of HP Computing – Technology Scaling and Hardware Accelerators: Terence Hook, IBM

9:10 a.m. Silicon Photonics Technology Enabling Both Low Power Consumption and High Aggregated Bandwidth: Ken Morito, PETRA

9:45 a.m. Confluence of Memory and Storage Technologies: Craig Hampel, Rambus

10:20 a.m. Break

10:35 a.m. 5G: From Data Center to Mobile Phone, System Architecture Influences on Semiconductor Technology Requirements: Ted Letavic, GlobalFoundries

11:00 a.m. Cloud Computing: Everything Close with 3D System Integration: Denis Dutoit, CEA-LETI

11:45 a.m. Performances and Application of Power Devices in Si, SiC and GaN: Salvo Coffa, STMicroelectronics

12:20 p.m. Lunch

The Beyond: Edge Computing and Emerging Horizons

1:30 p.m. The Road to Ultra-Low Energy Computation: Jan Rabaey, UC Berkeley

2:10 p.m. Challenge of MOS/MTJ-Hybrid Nonvolatile VLSI Processor for IoE Applications: Takahiro Hanyu, Tohoku U.

2:50 p.m. Recent Progress in Neuromorphic Computing: Geoffrey Burr, IBM

3:30 p.m. Break

3:45 p.m. Flexible Sensors for Health-Monitoring Applications: Takao Someya, U. Tokyo

4:25 p.m. Battery Life Considerations for Mobile PCs: Kamal Shah, Intel

5:05 p.m. Adjourn
Session 1 – TAPA I & II

Plenary Session

Tuesday, June 14, 8:05 a.m.
Chairpersons: M. Khare, IBM Research
M. Masahara, AIST

8:05 a.m. Welcome and Opening Remarks
R. Jammy, Carl Zeiss
S. Inaba, Toshiba Corporation Storage & Electronic Devices Solutions Company

1.1 – 8:35 a.m.
The Age of Sensors – How MEMS sensors will enable the next wave of new products (Invited), Stephen Lloyd, VP of Engineering and New Product Development, InvenSense, Inc.

1.2 – 9:20 a.m.
Intelligent Mobility realized through VLSI (Invited), Takao Asami, Senior Vice President, Nissan

Session 2 - TAPA I & II

Technology Highlights Session

Tuesday, June 14
Chairpersons: G. Yeap, Qualcomm
K. Endo, AIST

2.1 - 10:25 a.m.

2.2 - 10:50 a.m.

2.3 - 11:15 a.m.

Session 3 – Tapa I
Technology Focus Session:
System and Embedded Memory

Tuesday, June 14
Chairpersons: N. Ramaswamy, Micron Technology, Inc.
S. Chung, National Chiao Tung University

3.1 – 1:30 p.m.
Memory: Welcome to the Era of Innovative Architectures (Invited), D. Klein, Micron Technology, Inc.

3.2 – 1:55 p.m.
High-Density User-Programmable Logic Array Based on Adjacent Integration of Pure-CMOS Crossbar Antifuse into Logic CMOS Circuits, S. Yasuda, M. Oda, M. Matsumoto, K. Tatsumura, K. Zaitsu, Y.-H. Ho, M. Ono, Toshiba Corporation

3.3 – 2:20 p.m.
Advanced Non-volatile Embedded Memories for a Wide Range of Applications (Invited), S. Kimura, Hitachi, Ltd.

3.4 – 2:45 p.m.

Session 4 – Tapa II
Ge and SiGe Channel Devices

Tuesday, June 14
Chairpersons: L. Selmi, University of Udine
K. Tateiwa, Tower Panasonic Semiconductor, Ltd.

4.1 - 1:30 p.m.
4.2 - 1:55 p.m.

4.3 - 2:20 p.m.

4.4 - 2:45 p.m.

Session 5 – Tapa III
Device Reliability

Tuesday, June 14
Chairpersons: C.-P. Chang, Applied Materials
T. Yamashita, Renesas Electronics Corporation

5.1 - 1:30 p.m.

5.2 - 1:55 p.m.
Application of CVS and VRS Method for Correlation of Logic CMOS Wear Out to Discrete Device Degradation Based on Ring Oscillator Circuits, A. Kerber, T. Nigam, GLOBALFOUNDRIES Inc.

5.3 - 2:20 p.m.
Deep Insight into Process-induced Pre-existing Traps and PBTI Stress-induced Trap Generations in High-k Gate Dielectrics through Systematic RTN Characterizations and Ab-initio Calculations, J. Chen, Y. Nakasaki, Y. Mitani, Toshiba Corporation

5.4 - 2:45 p.m.
Session 6 – Tapa I

**Novel 2D Materials and Devices**

Tuesday, June 14
Chairpersons: P. Ye, Purdue University
M. Kobayashi, The University of Tokyo

6.1 - 3:25 p.m.
MoS2 U‐shape pMOSFET with 10 nm Channel Length and Poly‐Si MoS2 Source/Drain Serving as Seed for Full Wafer CVD MoS2 Availability,

6.2 - 3:50 p.m.
Serially Connected Monolayer MoS2 FETs with Channel Patterned by a 7.5 nm Resolution Directed Self‐Assembly Lithography
A. Nourbakhsh, A. Zubair, A. Tavakkoli, R. Sajjad, X. Ling, M. Dresselhaus, J. Kong, K. K. Berggren, D. Antoniadis and T. Palacios, Massachusetts Institute of Technology

6.3 - 4:15 p.m.

6.4 - 4:40 p.m.
Extremely Low Power C‐Axis Aligned Crystalline In‐Ga‐Zn‐O 60 nm Transistor Integrated with Industry 65 nm Si MOSFET for IoT Normally‐Off CPU Application,

6.5 - 5:05 p.m.
A Sub‐ns Three‐terminal Spin‐orbit Torque Induced Switching Device,
S. Fukami, T. Anekawa, A. Ohkawara, C. Zhang, H. Ohno, Tohoku University

Session 7 - Tapa II

**Contact Resistance Innovations for Sub-10nm Scaling**

Tuesday, June 14
Chairpersons: R. Arghavani, LAM Research
T.‐R. Yew, United Microelectronics Corp.

7.1 - 3:25 p.m.
Ultralow‐Resistivity CMOS Contact Scheme with Pre‐Contact Amorphization Plus Ti (Germano‐) Silicidation,

7.2 - 3:50 p.m.

7.3 - 4:15 p.m.

7.4 - 4:40 p.m.

7.5 - 5:05 p.m.

Session 8 – Tapa III
High Density Non Volatile Memory

Tuesday, June 14
Chairpersons: G. Hemink, SanDisk
H. Miyake, Micron Memory Japan, Inc.
8.1 - 3:25 p.m.

8.2 - 3:50 p.m.

8.3 - 4:15 p.m.

8.4 - 4:40 p.m.

8.5 - 5:05 p.m.
Te-Based Amorphous Binary OTS Device with Excellent Selector Characteristics for X-point Memory Applications, Y. Koo, K. Baek, H. Hwang, POSTECH

Technology Panel Sessions
Tuesday, June 14, 8:00 p.m. – 10:00 p.m.

Joint Technology / Circuits Panel Session
Organizers:
Technology: M. Jurczak, ASM
W. Rachmady, Intel
T. Tsunomura, TEL
Circuits: P. Kumar Hanumolu, University of Illinois
R. Navid, Rambus
M. Ito, Renesas

PJ-1: “More Moore, More than Moore, or Mo(o)re Slowly”
Moderator: Subramanian Iyer, University of California, Los Angeles

Over the past 50 years, rapid advancement of fabrication technology has allowed doubling the number of transistors in VLSI components every two years. This trend has continuously enabled new system features that had been previously impractical if not impossible. As a result of this, the growth of the global semiconductor market has been predominantly fueled by technology scaling in what can sometimes be referred to as a “more of the same is good enough” paradigm. As technology scaling slows down, this dynamic is changing and it is unclear what will drive future growth. Is the industry going to continue a
similar path through introduction of new devices and 3D integration? Or is the end of silicon scaling the end of brute force large-scale integration? If that is the case, what is the value of sensor and system integration? Can they generate enough demand to drive growth at a rate comparable to silicon integration? And what is the role of circuit innovation in this environment? One might argue that the “more of the same is good enough” attitude of the past few decades has been a major hindrance for emergence and adoption of many promising ideas at the circuit level? Is the end of scaling a blessing in disguise for the talented circuit designer who would love to tackle a more constrained problem? Renowned experts will attempt to answer these very important questions in this panel.

Panelists:

Fari Assadaraghi, NXP Semiconductors
Vivek De, Intel
Nicky Lu, Etron
Gary Patton, GLOBALFOUNDRIES
Thomas Skotnicki, STMicroelectronics
Jan Vardhaman, TechSearch International

Technology Panel Session

P-2: “How Moore’s Law, Industry Consolidation, and System Trends are Shaping the Memory Roadmap?”

Organizers: M. Jurczak, ASM
W. Rachmady, Intel
T. Tsunomura, Tokyo Electron Ltd.

Moderators: Gary Bronner, Rambus and Fred Chen, Winbond

The roadmap for memory, both DRAM and Flash, has historically been driven by a self-fulfilling prophecy – memory cost must drop 35% / year on a cost per bit basis. Moore’s law drove this exponential decrease in cost and increase in memory density for over 3 decades. But the last decade has seen interesting modifications to this historical trend. The emergence of NAND Flash memory led to even faster drops in price, with NAND now 16x cheaper than DRAM on a cost/bit basis. DRAM scaling limits are causing DRAM density improvement to slow and the price gap to widen. NAND Flash continues on a classical price/density roadmap but its performance is not sufficient to replace DRAM. Current systems and applications are facing a “Memory Wall” – cheap Flash bits don’t meet CPU performance needs while DRAM bits are no longer cheap enough to meet the capacity needs of multicore CPUs. This has triggered a burst of innovation at all levels – technology, system, and software, creating a myriad of possibilities to be considered.

This panel will debate the technology roadmaps for DRAM, FLASH, SCM (storage class memory) and eNVM (embedded Non Volatile Memory) in light of the fundamental problems around memory cost, performance, and power. Can any of the emerging NVM technologies provide compelling solutions to current computer system and application needs? Which industry will drive the new memory technology - data centers or mobile chip vendors? What memory (or combination of memories) gives the lowest total cost of ownership? How will computer systems handle new levels of memory hierarchy? How does industry consolidation and the emergence of new players in the memory industry affect the roadmap?
These and other questions raised from the audience will be addressed by a distinguished panel of experts from industry. It is a most interesting time to be involved in the memory world!

Panelists:

Shekhar Borker, Intel
Takashi Kono, Renesas
Jae-Jin Lee, SK Hynix
Junhee Lim, Samsung
Gurtej Sandhu, Micron
Rob Sprinkle, Google

Session 9 – Tapa II

Technology Scaling Beyond 10 nm

Wednesday, June 15
Chairpersons: E. Pop, Stanford University
K. Miyashita, Toshiba Corporation

9.1 - 10:15 a.m.

9.2 - 10:40 a.m.
First Demonstration of InGaAs/SiGe CMOS Inverters and Dense SRAM Arrays on Si Using Selective Epitaxy and Standard FEOL Processes, L. Czornomaz, V. Djara, V. Deshpande, E. O’Connor, M. Sousa, D. Caimi, K. Cheng*, J. Fompeyrine, IBM Research Zurich, *IBM Research Albany

9.3 - 11:05 a.m.

9.4 - 11:30 a.m.

Session 10 - Tapa III

Technology/Circuits Joint Focus Session:
Smart Power

Wednesday, June 15
Chairpersons: T. Palacios, Massachusetts Institute of Technology
               H. Morioka, Socionext, Inc.

10.1 – 10:15 a.m.
Smart Power Technologies Enabling Power SOC and SIP (Invited), S. Pendharkar, Texas Instruments

10.2 – 10:40 a.m.
A Dynamic/Static SRAM Power Management Schemes for DVFS and AVS in Automotive Infotainment SoCs (Invited), K. Nii, M. Yabuuchi, Y. Ishii, M. Tanaka†, M. Igarashi, K. Fukuoka†, and S. Tanaka, Renesas Electronics Corporation, †Renesas System Design Corporation

10.3 - 11:05 a.m.
A Multiple-String Hybrid LED Driver with 97% Power Efficiency and 0.996 Power Factor, L. Li, Y. Gao, P. Mok, HKUST

10.4 – 11:30 a.m.

Session 11 – Tapa II
Technology/Circuits Joint Focus Session:
Analog / RF Integration and DTCO in CMOS

Wednesday, June 15
Chairpersons: G. Yeric, ARM
               Y.-C. Yeo, TSMC

11.1 – 1:15 p.m.
Overcoming Scaling Barriers through Design Technology CoOptimization (Invited), L. Liebmann, J. Zeng, X. Zhu, L. Yuan, G. Bouche, J. Kye, GLOBALFOUNDRIES

11.2 – 1:40 p.m.

11.3 - 2:05 p.m.
11.4 - 2:30 p.m.
Broadband THz Spectroscopic Imaging based on a Fully Integrated 4×2 Digital-to-Impulse Radiating Array with a Full-Spectrum of 0.03-1.03THz in Silicon, M. Mahdi Assefzadeh, A. Babakhani, Rice University

Session 12 – Tapa III
Emerging Memory Technology (RRAM and PCM)

Wednesday, June 15
Chairpersons: M. Jurczak, ASM
B.-H. Lee, Gwangju Institute of Science and Technology

12.1 - 1:15 p.m.

12.2 - 1:40 p.m.

12.3 - 2:05 p.m.
Retention, Disturb and Variability improvements enabled by local Chemical-potential Tuning and controlled Hour-Glass filament shape in a novel W\WO₃\Al₂O₃\Cu CBRAM, L. Goux*, A. Belmonte***, U. Celano***, J. Woo*, S. Folkersma*, C. Y. Chen***, A. Redolfi*, A. Fantini*, R. Degraeve*, S. Clima*, W. Vandervorst***, M. Jurczak*, *IMEC, **KU Leuven

12.4 - 2:30 p.m.

Session 13 – Tapa II
FDSOI and III-V Devices

Wednesday, June 15
Chairpersons: C. Mazure, Soitec Group
S. Takagi, The University of Tokyo

13.1 - 2:55 p.m.

13.2 - 3:20 p.m.

13.3 - 3:45 p.m.
High Aspect Ratio InGaAs FinFETs with Sub-20 nm Fin Width, A. Vardi, J. Lin, W. Lu, X. Zhao and J. A. del Alamo, Massachusetts Institute of Technology

13.4 - 4:10 p.m.

13.5 - 4:35 p.m.
Record Mobility (\(\mu_{\text{eff}}\sim3100\ \text{cm}^2/\text{V-s}\)) and Reliability Performance (\(V_{\text{ov}}\sim0.5\text{V}\) for 10yr Operation) of \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As}\) MOS Devices Using Improved Surface Preparation and a Novel Interfacial Layer, A. Vais***, A. Alian*, L. Nyns*, J. Franco*, S. Sioncke*, V. Putcha***, H. Yu***, Y. Mols*, R. Rooyackers**, D. Lin*, J.W. Maes***, Q. Xie***, M. Givens*, F. Tang**, X. Jiang**, A. Mocuta*, N. Collaert*, K. De Meyer***, A. Thean*, *IMEC, **KULeuven, ***ASM Belgium, *ASM, AZ, USA

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Session 14 – Tapa III

STT-MRAM and Ferroelectric Memories

Wednesday, June 15

Chairpersons: K. Baker, Freescale NXP
S.-W. Chung, SK Hynix Semiconductors, Inc.

14.1 - 2:55 p.m.
14.2 - 3:20 p.m.

14.3 - 3:45 p.m.
First Demonstration and Performance Improvement of Ferroelectric HfO2-based Resistive Switch with Low Operation Current and Intrinsic Diode Property, S. Fujii, Y. Kamimuta, T. Ino, Y. Nakasaki, R. Takaishi, M. Saitoh, Toshiba Corporation

14.4 - 4:10 p.m.

14.5 - 4:35 p.m.
Study of Wake-up and Fatigue Properties in Doped and Undoped Ferroelectric HfO2 in Conjunction with Piezo-Response Force Microscopy Analysis, S. Shibayama*, **, L. Xu*, S. Migita***, A. Toriumi*, *The University of Tokyo, **JSPS research fellow PD, ***AIST

Executive Panel Discussion

Wednesday, June 15, 6:00 p.m. – 7:00 p.m.

Chairs: Raj Jammy, Carl Zeiss
Satoshi Inaba, Toshiba Electronics Korea Corporation

Semiconductor Business: Inflections Beyond Scaling
Moderator: Dan Hutcheson, CEO and Chairman of VLSI Research Inc and author of The Chip Insider

As semiconductor industry approaches seemingly finite limits of physical scaling, a number of inflections are unfolding around us that may require us to rethink how we design, develop and manufacture semiconductor devices. Sensing, positioning, energy-aware and predictive systems are becoming the norm, opening up wider applications and enormous growth potential for semiconductor industry. Yet, implementation of such technologies from research to reality also poses technical and business challenges. Such systems require ultra-low power, always-on sensing, connectivity, vast embedded and discrete memory, smart energy sources and management - all wrapped in to ever smaller form factors. IoT, self-driving automobiles, next generation 5G networks, machine learning, brain-inspired computing, virtual/immersive reality and many other emerging trends will also need large investments for successful deployment and business models for ROI. The cost of developing such technologies, acceptable standards,
security protocols, inter-platform operability, etc., will need unprecedented collaboration in the industry. The panel will deliberate on these topics and discuss trends, applications that are shaping around us, industry needs, infrastructural/manufacturing gaps and economic challenges.

Panelists:

Mike Cadigan, Senior Vice President, Global Sales and Business Development, GLOBALFOUNDRIES
Tze-Chiang Chen, IBM Fellow, IBM TJ Watson Research Center, IBM
SungJoo Hong, EVP and Head of R&D, SK Hynix
Steve Lloyd, Vice President, Engineering and New Product Development, InvenSense
Marie-Noelle Semaria, CEO, CEA LETI

Session 15 – Tapa II
Gate All Around and III-V Devices

Thursday, June 16
Chairpersons:  W. Maszara, GLOBALFOUNDRIES
                 K. Endo, AIST

15.1 - 8:05 a.m.

15.2 - 8:30 a.m.

15.3 - 8:55 a.m.
InGaAs Nanowire MOSFETs with $I_{ON} = 555 \mu A/\mu m$ at $I_{OFF} = 100 nA/\mu m$ and $V_{DD} = 0.5 V$, C. B. Zota, F. Lindelöw, L.-E. Wernersson, E. Lind, Lund University

15.4 - 9:20 a.m.

15.5 - 9:45 a.m.

Session 16 – Tapa III
Variability and Design Technology Co-Optimization

Thursday, June 16
Chairpersons: L. Bair, AMD
N. Sugii, Hitachi, Ltd.

16.1 - 8:05 a.m.
RTN and Low Frequency Noise on Ultra-scaled Near-ballistic Ge Nanowire nMOSFETs, W. Wu*., **, ***, H. Wu*, M. Si*, N. Conrad*, Y. Zhao**, ***, P. D. Ye*, *Purdue University, **Nanjing University, ***Zhejiang University

16.2 - 8:30 a.m.
Statistical Limits of Contact Resistivity Due to Atomic Variation in Nanoscale Contacts, G. Shine, C. E. Weber*, K. C. Saraswat, Stanford University, *Intel Corporation

16.3 - 8:55 a.m.

16.4 - 9:20 a.m.

16.5 - 9:45 a.m.

Session 17 – Tapa II
Technology Focus Session:
Interconnect and 3D Integration
Thursday, June 16
Chairpersons: W. Rachmady, Intel Corporation
M. Tada, NEC Corporation

17.1 – 10:25 a.m.
On-chip Interconnect Trends, Challenges and Solutions: How to Keep RC and Reliability Under Control (Invited), Z. Tőkei, I. Ciofi, Ph. Roussel, P. Debacker, P. Raghavan, M. van der Veen, N. Jourdan, C. Wilson, V.V. Gonzalez, C. Adelmann, L. Wen, K. Croes, K. Moors, M. Krishtab, S. Armini, J. Boemmelms, IMEC

17.2 – 10:50 a.m.
Production-Worthy WOW 3D Integration Technology using Bumpless Interconnects and Ultra-Thinning Processes (Invited), T. Ohba, Tokyo Institute of Technology

17.3 – 11:15 a.m.

17.4 – 11:40 a.m.
A Highly Scalable Poly-Si Junctionless FETs Featuring a Novel Multi-Stacking Hybrid P/N Layer and Vertical Gate with Very High Ion/Ioff for 3D Stacked ICs, Y.-C. Cheng*,**, H.-B. Chen**, C.-Y. Chang**.*, C.-H. Cheng***, Y.-J. Shih**, Y.-C. Wu*, *National Tsing Hua University, **National Chiao-Tung University, ***National Taiwan Normal University, *Academia Scientia

Session 18 – Tapa III
Non Volatile Memories and Applications

Thursday, June 16
Chairpersons: M. Vinet, CEA-LETI, MINATEC
H.-T. Lue, Macronix International Co., Ltd.

18.1 – 10:25 a.m.

18.2 - 10:50 a.m.

18.3 - 11:15 a.m.

18.4 - 11:40 a.m.
A ReRAM-based Physically Unclonable Function with Bit Error Rate < 0.5% after 10 years at 125˚C for 40nm Embedded Application, Y. Yoshimoto, Y. Katoh, S. Ogasahara, Z. Wei, K. Kouno, Panasonic Semiconductor Solutions Corporation

Luncheon Talk

Thursday, June 16, 12:15 p.m. – 1:30 p.m.

Cyborg insects and other things: building interfaces between the synthetic and the multicellular

As the computation and communication circuits we build radically miniaturize (i.e. become so low power that 1 pJ is sufficient to bang out a bit of information over a wireless transceiver; become so small that 500 µm^2 of thinned CMOS can hold a reasonable sensor front-end and digital engine), the barrier to introducing these types of interfaces into organisms will get pretty low. Put another way, the rapid pace of computation and communication miniaturization is swiftly blurring the line between the technological base that created us and the technological based we've created. In this talk, I'll give an overview of recent work in my lab that touches on this concern. Most of the talk will cover our ongoing exploration of the remote control of insects in free flight via implantable radio-equipped miniature neural stimulating systems.; recent results with pupally-implanted neural interfaces and extreme miniaturization directions will be discussed. If time permits, I will show recent results building extremely small neural interfaces we call "neural dust," work done in collaboration with the Carmena, Alon and Rabaey labs.

Biography: Michel M. Maharbiz is an Associate Professor with the Department of Electrical Engineering and Computer Science at the University of California, Berkeley.

He received his Ph.D. from the University of California at Berkeley under Professor Roger T. Howe (EECS) and Professor Jay D. Keasling (ChemE); his work led to the foundation of Microreactor Technologies, Inc. which was acquired in 2009 by Pall Corporation. From 2003 to 2007, Michel Maharbiz was an Assistant Professor at the University of Michigan, Ann Arbor. He is the co-founder of Tweedle Technologies, Cortera Neurotech and served as vice-president for product development at Quswami, Inc. from July 2010 to June 2011.

Prof. Maharbiz is a Bakar Fellow and was the recipient of a 2009 NSF Career Award for research into developing microfabricated interfaces for synthetic biology. His group is also known for developing the
world’s first remotely radio-controlled cyborg beetles. This was named one of the top ten emerging technologies of 2009 by MIT’s Technology Review (TR10) and was in Time Magazine’s Top 50 Inventions of 2009. Dr. Maharbiz has been a GE Scholar and an Intel IMAP Fellow. Professor Maharbiz’s current research interests include building micro/nano interfaces to cells and organisms and exploring bio-derived fabrication methods. Michel’s long term goal is understanding developmental mechanisms as a way to engineer and fabricate machines.”

Session 19 – Tapa II
High-K Metal Gate Variability and Scaling

Thursday, June 16
Chairpersons: A. Ionescu, Swiss Federal Institute of Technology
T. Tsunomura, Tokyo Electron Ltd.

19.1 - 1:30 p.m.

19.2 - 1:55 p.m.

19.3 - 2:20 p.m.

19.4 - 2:45 p.m.

Session 20 – Tapa III
Sensor Technology and Microsystems for IoT

Thursday, June 16
Chairpersons: B.K. Liew, nVidia
S. Yamakawa, Sony Corporation

20.1 - 1:30 p.m.

20.2 - 1:55 p.m.

20.3 - 2:20 p.m.

20.4 - 2:45 p.m.

Session 21 – Tap II
Steep Sub-Threshold Devices

Thursday, June 16
Chairpersons: S. Salahuddin, University of California, Berkeley
M. Kobayashi, The University of Tokyo

21.1 - 3:25 p.m.

21.2 - 3:50 p.m.
Performance improvement of In_{x}Ga_{1-x}As Tunnel FETs with Quantum Well and EOT scaling, D. H. Ahn, S. M. Ji, M. Takenaka, S. Takagi, The university of Tokyo, JST CREST

21.3 - 4:15 p.m.
Complementary III-V Heterojunction Lateral NW Tunnel FET Technology on Si, D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, H. Riel, IBM Research Zurich

21.4 - 4:40 p.m.

21.5 - 5:05 p.m.
Circuit Performance Analysis of Negative Capacitance FinFETs, S. Khandelwal, A. I. Khan, J. P. Duarte, A. B. Sachid, S. Salahuddin, C. Hu, University of California, Berkeley

Session 22 – Tapa III
CMOS Image Sensors

Thursday, June 16
Chairpersons: K. Benaissa, Texas Instruments
T. Tanaka, Tohoku University

22.1 – 3:25 p.m.

22.2 – 3:50 p.m.

22.3 – 4:15 p.m.

22.4 – 4:40 p.m.

22.5 – 5:05 p.m.